austriamicrosystems AG

is now

ams AG

The technical content of this austriamicrosystems datasheet is still valid.

Contact information:

Headquarters:
ams AG
Tobelbaderstrasse 30
8141 Unterpremstaetten, Austria
Tel: +43 (0) 3136 500 0
e-Mail: ams_sales@ams.com

Please visit our website at **www.ams.com**

General Description

The AS3510 combines high flexibility and outstanding performance for analog audio front-end solutions.

This codec-chip contains a high performance 18 bit digital to analog converter. The dynamic range exceeds 95dB for best audio quality, for multi media applications (audio playback) within battery or line operated equipment.

An additional audio power amplifier can directly drive external headphones or small 4Ω speakers with a power of up to half a watt. The power-up is click- and pop-less due to a smooth start-up circuitry. The overall distortion level is always below 0.02%.

The microphone input amplifier contains an automatic gain control (AGC) with a dynamic range of 40dB to generate an amplified and compressed signal for the ADC, which provides 14 Bit resolution at 8kHz sampling-rate.

Furthermore all necessary power management is included such as bandgap reference and four voltage regulators. The two 2.9V regulators are used internally (analog and digital supply), but can also be used for external purposes as well. The third output is designed to supply the peripheral cells and an external digital core, and is programmable from 1.5V to 2.5V in 5 steps (default is 2.5V). They are all powered through a DCDC-Converter, which can work down to a voltage of 1V. So the whole chip can work from a single battery cell.

The fourth regulator is only used for generating the supply voltage for the analog USB 1.1 interface circuit. It is supplied via the USB connector. The performance of the regulators is excellent (noise, line- and load-regulation) and allows the direct supply of sensitive analog circuits.

Because of the internal supply and signal filtering only few small external capacitors are required for de-coupling and stabilising and lead to very low output noise.

The current consumption is very low and makes the chip ideally for battery powered devices.

Key Features

<u>On chip DCDC Converter</u>

- 1.0 to 5.5V input voltage range

<u>4 On-chip high performance voltage regulators</u>

- Digital Supply, 2.9V
- Analog Supply, 2.9V
- Core Supply, 1.5 to 2.5V
- USB Transceiver Supply, 3.2V

<u>18 Bit stereo DAC</u>

- Dynamic range >95 dB
- THD < -85dB
- De-emphasis for 32 kHz, 44.1 kHz and 48 kHz

<u>Stereo power audio amplifier</u>

- Max. 2x 0.5W @ 4Ω
- Analog volume control –39dB to +3dB, 3dB steps including mute)
- Click- and pop-less startup and power down
- Auxiliary inputs for additional audio sources

<u>Microphone input</u>

- 14 Bit ΣΔ–ADC , 8kHz sampling rate
- Automatic gain control (AGC)

- Low power consumption
- Wide battery supply range 1.0V – 5.5V
- Standard I2S interface
- Audio sampling rates: 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, and 48 kHz
- I2C control interface
- USB 1.1 front-end
- 49 Pin BGA Package

Applications

- Audio frontend for cellular phones
- Stand alone MP3 player
- CD and DVD player
- PDAs

Block Diagram

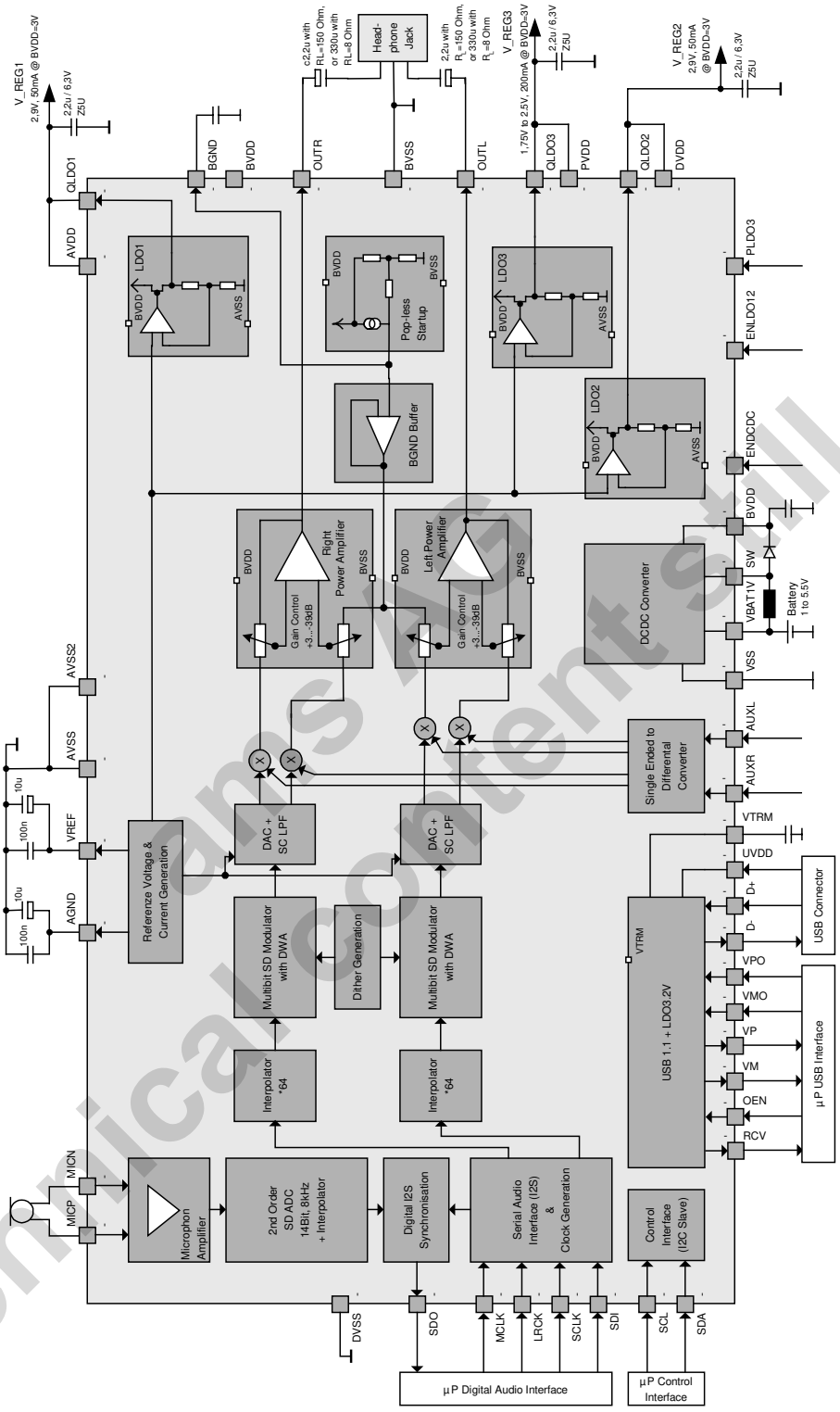

Figure 1 Block Diagram of AS3510

Modes of Operation

LDO-Modes	Inputs ENLDO12	Inputs ENLDO3	Outputs DVDD, AVDD	Outputs PVDD
OFF	L	L	LDO1, LDO2 are OFF 2.8–3.6V supply fr. Ext.	LDO3 is OFF 1.75-3.6V supply fr. Ext.
ON_12	H	L	LDO1, LDO2 are ON Output is 2.9Vtyp	LDO3 is OFF 1.75-3.6V supply fr. Ext. or connected to DVDD
ON_123	H	H	LDO1, LDO2 are ON Output is 2.9Vtyp	LDO3 is ON Output 2.5Vtyp

Table 1 LDO Operating Modes

Nodes:

- 1. BVDD as input to the LDO regulators has to be >=3.0V.
- 2. DVDD - AVDD max. difference of 100mV.
- 3. PVDD has to be lower or equal to DVDD.
- 4. LDO1 is to be used for regulating AVDD (connect pin 25 to pin 26)
- 5. LDO2 output is internaly connected to DVDD (pos. digital supply)
- 6. LDO3 output is internaly connected to PVDD (pos. peripheral supply)

DAC-Modes	Inputs DACPD	Inputs I2S	Inputs Gain3:0	Outputs OUTR, OUTL
OFF	H	X	LLLL	TriState
DAC_ON	L	LRCK up to 50kHz MCLK ... 128*F(LRCK) SCLK L=>H strobes SDI SCLK ... >=38*F(LRCK) SDI left justified with MSB first at 2nd SCLK edge	LLLL	TriState
AUDIO_ON	L	LRCK up to 50kHz MCLK ... 128*F(LRCK) SCLK L=>H strobes SDI SCLK ... >=38*F(LRCK) SDI left justified with MSB first at 2nd SCLK edge	LLLH . . HHHH	Stereo audio output with PowerAmp gain adjusted in 3dB steps by GAIN(3:0)

Table 2 DAC Operating Modes

Nodes:

- During supply voltages settling at system start-up GAIN(3:0) should be held “L”.
- The MCLK frequency ratio to LRCK is permanently checked. If the ratio is different to 128, the DAC goes in Reset-Mode (no audio will betransferred).
- MCLK rising edge should not be within +/-10ns of LRCK edges.
- Capacitors at VREF, AGND and BGND are needed for the DAC operation.
- The SCLK has to have at least 34 or 38 cycles within one LRCK cycle
  2*(16bit data + the leading empty bit) or 2*(18bit data + the leading empty bit)
- There can be more SDI bits presented but just the first 18 bits are transferred.

ADC-Modes	Inputs ENADC	I2S-Clocks LRCK, SCLK,MCLK	MICP/MICN	Output SDO
OFF	L	X	X	static L
ADC_ON	H	LRCK up to 50kHz MCLK ... 128*F(LRCK) SCLK ... >=34*F(LRCK)	Differential analog input to be converted to digital output	SDI serial data output left justified to LRCK with MSB first at 2nd SCLK edge

Table 3 ADC Operating Modes

Nodes:

- There are 16bit presented at SDO at each cycle but just the first 14 do have relevalt data.
- The ADC is a single channel (mono) path. The same SDO bitstream is presented for left and right channel of one cycle.
- The ADC sampling rate is equal to LRCK/4. This means that the SDO bitstream gets updated at each 4th cycle of LRCK.
- SCLK has to have at least 34 cycles within one LRCK cycle
  2*(16bit data + the leading empty bit)

Functional Description

Audio DAC

Block Description

This block is the complete audio DAC delivering 93dB dynamic range. It is comprised of a multibit sigma-delta modulator with dither option and a switched-capacitor analog filter. This architecture provides a high insensitivity to clock jitter. A digital interpolation filter increases the sample rate by a factor of 8 using 3 linear phase, half-band filters cascaded, followed by a first order SINC interpolator with a factor of 8. This filter eliminates the images of baseband audio remaining only the image at 64* the input sample rate. Optionally, a dither signal can be added that may reduce eventual noise tones at the output. However, the use of a multibit delta-sigma modulator already provides extremely low noise tone energy.

Signal Description

Setting DACPD to ´1´ forces the analog section to power-down. For Normal-Operation the I2S signals have to be applied as shown below:

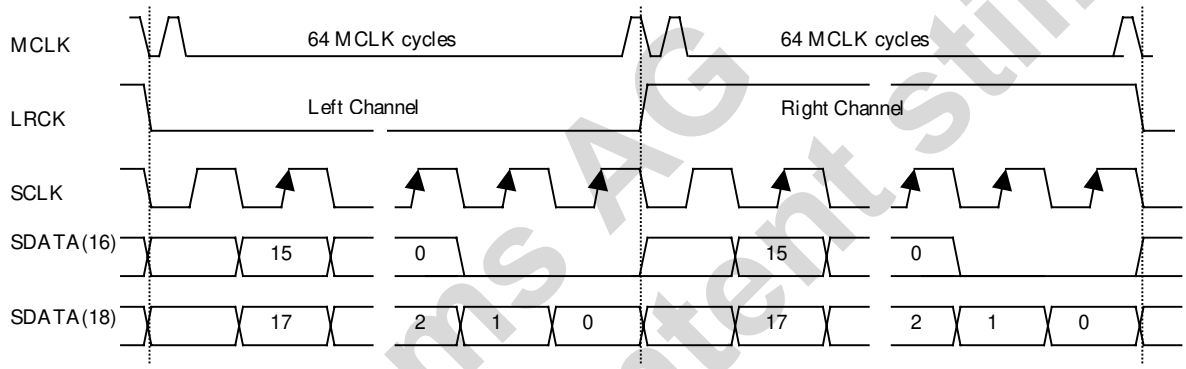

Figure 2 I2S Waveforms

The LRCK defines if the transferred data is for the left or right channel (L=left).

With the rising edge of the serial clock SCLK, the inputdata gets strobed.

The data word at SDATA is max. 18 bit with MSB first and 2nd complement coded. All I2S signals change state with falling edge of SCLK.

code	hex value
Max. positive code	1FFFF (hex)
+1	00001 (hex)
0	00000 (hex)
-1	3FFFF (hex)
Max. negative code:	20000 (hex)

Table 4 I2S Code Values

If the dataword length is less than 18 bit, zeros have to be added to avoid any offset value.

The frequency of master clock MCLK has to be 128 times the input sample rate (F(LRCK)*128) with low jitter. The rising edge of MCLK should be separated by >10ns from LRCK edges.

There are 2 pins needed for the generation and decoupling of reference-voltages for the DAC. AGND is AVDD/2 and VREF is equal to AVDD. Both pins have high output resistance which provides a suitable lowpass filter for these reference voltages with external capacitors of 10uF in parallel with 100nF.

The supply lines are separate for digital DVSS / DVDD and analog AVSS / AVDD to minimise coupling influences.

The analog output is differential stereo signal at nodes OUTRN, OUTRP and OUTLN, OUTLP respectively.

Control Interface

The interface is a standard I2C slave interface (write only). The system uses address group 8 address 41h for audio-processors. The following table shows the various control options.

Byte 0 (default value: 0x80h)

Bit	Name	Description
7	DITH	dither enable 1: enable (default) 0: disable
6..5	DacON	11: Audio DAC is switched on 10: Audio DAC is switched on 01: Audio DAC is switched off 00: automatic mode, DAC is on only when I2S interface is active
4	LP4/16	audio amplifier load switch 1: low power mode for speakers with more than 16 Ohm. 0: normal mode, 4 Ohm loads possible
3..0	Gain	gain settings for audio amplifier from –39dB to +3dB in steps of 3dB 1111: full output swing: +3dB 1110: 0dB . 0010: -36dB 0001: minimum output swing: -39dB 0000: mute

Table 5 – Software I2C Byte 0

Byte 1 (default value: 0x10h)

Bit	Name	Description
7	-	not used
6	Fadc2	1: doubles the sampling ADC freq. 0: normal ADC sampling frequnecy
5	USBspN	1: normal USB operation 0: suspend USB
4	PwUphld	0: switch off
3	AUXen	1: enable AUX inputs 0: disable AUX inputs
2	ADCen	1: ADC enable for microphone input 0: ADC disable
1..0	MicGain	gain settings for microphone amplifier 11: 40dB 10: 40dB 01: 34dB 00: 28dB

Table 6 – Software I2C Byte 1

The PowerUp hold (PwUphld; Bit 4) is when an high pulse on the PowerUp pin occures. To switch of the AS3520 the PwUphld bit must be cleared.

Byte 2 (default value: 0x01h)

Bit	Name	Description
7..6	Iaudio	audio amplifier supply current 11: 50% 10: 66% 01: 83% 00: 100% (default)
5..4	Idac	audio DAC supply current 11: 50% 10: 60% 01: 75% 00: 100% (default)
3..1	-	not used, must be set to 000
0	MCLK#	1: DAC uses inverted MCLK 0: DAC uses normal MCLK

Table 7 – Software I2C Byte 2

Byte 3 (default value: 0x11h)

Bit	Name	Description
7..4	Version	not used
3	-	not used
1..2	-	not used, must be set to 000
0	I2Sdir	1: only 18bit data are accepted 0: also less than 18 bit can be sent to the I2S interface and are shifted internal

Table 8 – Software I2C Byte 3

Power Amplifier

Block Description

The Power Amplifier Block converts the differential output signals from the AudioDAC into single ended signals with the drive capability for impedances ≥4 ohms.

With the conversion from differential to single ended, the transformation of DC level from AGND (=AVDD/2) to BGND (=BVDD/2) is done. The gain of this driver stage can be set by 4 digital input signals in the range from –39dB to +3dB in steps of 3dB. With the maximum gain of +3dB, full scale gives 4.95Vpp at the single ended output.

With I2S data giving full-scale swing, clipping will occur with the max. gain-step. With min. BVDD of 3.0V the same is true for the two highest gain-steps.

When the control signals Gain(3:0) are all set to "L", the block is set to power-down.

There is a BGND generation, which needs an external capacitor of 100nF for blocking of low frequency components at BVDD. With this external capacitor, a so called "Klickless On" is performed so that at power-up, the output terminals have a smooth startup to avoid any transient noise in the headphone.

Gain (3:0)				Gain dif→se	FS Swing		Gain (3:0)				Gain dif→se	FS Swing
H	H	H	H	+3dB	4.95Vpp		L	H	H	H	-21dB	309mVpp
H	H	H	L	0dB	3.50Vpp		L	H	H	L	-24dB	219mVpp
H	H	L	H	-3dB	2.47Vpp		L	H	L	H	-27dB	155mVpp
H	H	L	L	-6dB	1.75Vpp		L	H	L	L	-30dB	109mVpp
H	L	H	H	-9dB	1.24Vpp		L	L	H	H	-33dB	77mVpp
H	L	H	L	-12dB	0.87Vpp		L	L	H	L	-36dB	55mVpp
H	L	L	H	-15dB	0.62Vpp		L	L	L	H	-39dB	39mVpp
H	L	L	L	-18dB	0.44Vpp		L	L	L	L	OFF	-

Table 9 Table of Gain Steps

Supply Regulator

Block Description

This block can be used to provide three regulated supply voltages for the

- on_chip digital section
- on_chip analog section
- external circuit (uP, DSP...)

from the battery supply BVDD which is directly used by the power_amplifier.

The LDO1 and LDO2 do have the capability to drive 50mA with a voltage drop of <=50mV (1Ohm). Since the nominal output voltage for these LDOs is 2.9V (+/-50mV), a regulation can be done with BVDD as low as 3.0V.

The LDO3 is used to generate a supply voltage PVDD for the peripheral cells and external digital circuits, which are controlling the inputs of the AS3510. The drive capability is ≥200mA with a BVDD≥3V.

The maximum output currents for these LDOs can be calculated using the following equation:

$$I_{max} = \frac{(BVDD - (Vout + 50mV)}{1Ohm}$$

Vout is 2.9V for LDO1 and LDO2. The output Voltage for LDO3 can be programmed via the PLDO3 pin.

PLD3 pin	QLDO3 voltage
VSS	2.25V
150k to VSS	2.0V
open	2.5
150k to DVDD	1.5
DVDD	1.75

Table 10 LDO3 Programming

There are two pads at each LDO, one is the LDO output pad and the second is the corresponding chip supply pad, which are bonded to the same pin (LDO1 only), and have external blocking caps (Cblock with low ESR).

If supply should not be generated from the on_chip LDOs, these blocks can be disabled with control pin PowerUP. AVDD, DVDD and PVDD can then be forced from external regulators.

Microphone Path

Block Description

This block converts a differential microphone signal into digital and does a synchronisation to the DAC I2S input clocks. The SigmaDelta converter clock gets derived from MCLK. For LRCK=32kHz ➔ MCLK=4.096MHz, the SD_CLK is 1.024MHz which gives with decimation to 14 bit a sampling rate of 8kHz. Since the I2S signals for the DAC-path is 4 times higher, each ADC-output-code will be presented 4 times in both channels (left, right) the same.

For LRCK=48kHz ➔ MCLK=6.144MHz, the ADC conversion rate will be 12kHz. Due to this synchronisation the transfer of the ADC data is possible with just one extra digital output pin which makes the digital interface very efficient.

The microphone amplifier can be programmed to three different gain values 28dB/ 34dB/ 40dB to adjust the circuit to the used microphone. The microphone amplifier includes a softclip function that reduces the gain when the input voltage range of the ADC is violated.

The fullscale ADC input range is 1.157Vp differential with AVDD=2.9V.

The softclip references are +/-0.434V which gives a useable ADC-range of 0.868Vp differential. This gives a nominal mic input voltage range of 34.72 / 17.36 / 8.68mVp or 24 /12 / 6mVrms for the three micamp gain settings.

SoftClip is done with 15 steps of –1dB.

Specifications

Electrical Characteristics

Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNIT	Note
DCDC Input Supply Voltage	VBAT1.0	-0.5	5.0	V	
Battery Input Supply Voltage	BVDD	-0.5	7.0	V	
USB Input Supply Voltage	UVDD	-0.5	7.0	V	
AVDD Input Supply Voltage	AVDD	-0.5	5.0	V	
PVDD Input Supply Voltage	PVDD	-0.5	5.0	V	
DVDD Input Supply Voltage	DVDD	-0.5	5.0	V	
Voltage between VSS-Terminals VSS_DCDC, BVSS, AVSS, DVSS	xVSS	-0.5	0.5	V	
Voltage at pins: PowerUp, PLDO3, MICP, MICN, VREF, AGND, BGND, QLDO3, QLDO2, SW	Vin	-0.5	AVDD+0.5	V	
Voltage at pins: CSCL, CSDA	Vin	-0.5	5.0	V	no diode to DVDD
Voltage at pins: AUXL, AUXR, OUTL, OUTR	Vin	-0.5	BVDD+0.5	V	
Voltage at pins: VTREM, DP, DM	Vin	-0.5	5.0	V	
All other digital input pins	V_i	-0.5	DVDD+0.5	V	
Input Current (latchup immunity)	Iscr	-100	100	mA	
Electrostatic Discharge			1	kV	HBM, IEC61000-4-2
Storage Temperature	Tstrg	-55	125	^{O}C	
Soldering conditions	T_{lead}		240	^{O}C	IEC61760-1
Humidity non-condensing		5	85	%	

Table 11 Table of Absolute Maximum Ratings

Operating Conditions

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Analog Input Supply Voltage	AVDD	2.8	2.9	3.6	V
Digital Input Supply Voltage	DVDD	2.8	2.9	3.6	V
Digital Core Input Supply Voltage	PVDD	1.5		2.5	V
Battery Input Supply Voltage	BVDD	3.0	3.2	5.5	V
DCDC Input Supply Voltage	VBAT1.0	1.0	1.5	3.6	V
USB Input Supply Voltage	UVDD	4.0	5.0	5.5	V
Ambient Temperature		-20	25	85	C

Table 12 Table of Operating Conditions

Block Characteristics

Overall

SUPPLY	MIN	TYP	MAX	UNIT
AVDD (AVDD = 2.9 V)		2.6	9	mA
DVDD analog (DVDD = 2.9V)		4.5	8.5	mA
IDD in Power Down		< 1	10	uA

Table 13 Table of Overall Block Characteristics

AudioDAC

PARAMETER	MIN	TYP	MAX	UNIT
ANALOG PERFORMANCE				
THD+Noise at –1dB_FS		-85	-75	dB
Dynamic Range (20Hz-20kHz, -60dBFS)	90	93		dB
Interchannel Mismatch			0.25	dB

Table 14 Table of AudioDAC Block Characteristics

Power Amplifier

PARAMETER	MIN	TYP	MAX	UNIT
ANALOG PERFORMANCE				
R_Load at AOUTR and AOUTL differential	8			Ohm
R_Load at AOUTR and AOUTL single ended	4			Ohm
Gain Step Precision (RLmin-max,20Hz-20kHz)		±0.5	±	dB
THD @ 1kHz, BVDD=3-5V, Gain=8, no Load	-	-	0.03%	%
PSRR (200Hz-20kHz)	60	-	-	dB
IOUT_powerdown	-20		20	uA
Tpower_up (Cbgnd=100nF)		200		ms

Table 15 Table of Power Amplifier Block Characteristics

Supply Regulator

PARAMETER	MIN	TYP	MAX	UNIT
POR PERFORMANCE				
DVDD_POR_OFF	-	2.15		V
DVDD_POR_ON		2.0	-	V
POR_ON/OFF_HYST		100		mV
LRCK WATCHDOG with DVDD=2.9V				
F(LRCK)_WD_OFF	-	4.1		kHz
F(LRCK)_WD_ON		3.91	-	kHz
ON_Delay		50		us

Table 16 Table of Supply Regulator Block Characteristics

Microphone Path

PARAMETER	MIN	TYP	MAX	UNIT
ANALOG PERFORMANCE				
Rinp_dif (MICP, MICN)		30		kohm
Gain_MicAmp_0		28		dB
Gain_MicAmp_1		34		dB
Gain_MicAmp_2		40		dB
SoftClip_AGC_Range		15*1.0		dB
Attack_Time		39		us/st
Release_Time		80		ms/st
MIC vin full scale_0 (AVDD=2.9V)		24		mVrms
MIC vin full scale_1 (AVDD=2.9V)		12		mVrms
MIC vin full scale_2 (AVDD=2.9V)		6		mVrms
Decimation Rate		128		
ENOB		14		bit
SNR		71		dB
PSRR		tbd		dB

Table 17 Table of Microphone Path Block Characteristics

Measurements

The following measurement curves are the results from noise measurements on the AS3510 DAC.

TA.: 25C, Vdd: 2.9V, Signal: 1kHz, 0dBFS, Clk:128*48kHz

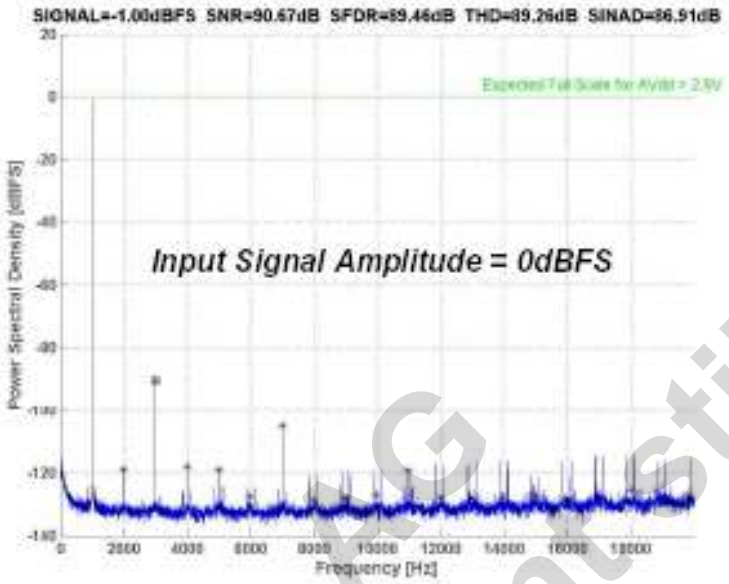

Figure 3 SINAD Measurement at 0dBFS

TA.: 25C, Vdd: 2.9V, Signal: 1kHz, -20dBFS, Clk:128*48kHz

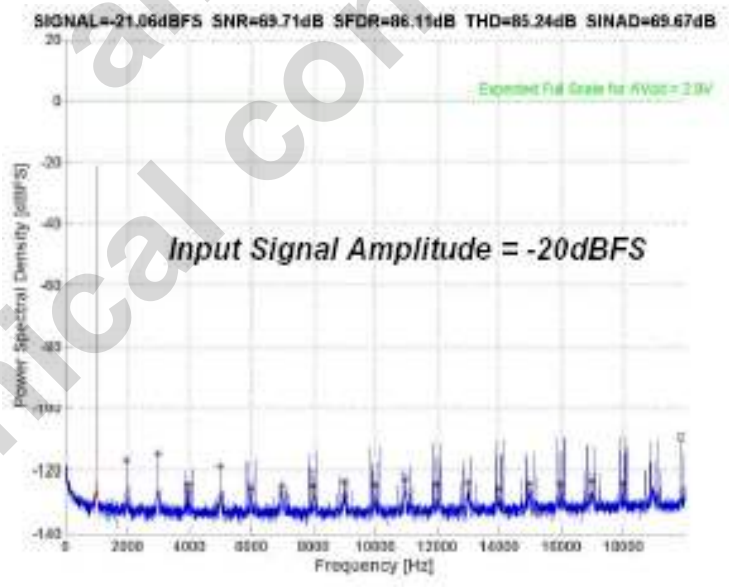

Figure 4 SINAD Measurement at -20dBFS

Package and Pinning

Pin Configuration for TQFP80

Pin#	PinName	Type	Function
25	DVSS	Supply	Neg. supply of digital circuit
27	PVDD	Supply	Supply of peripheral levelshifter of digital inputs
28	DVDD	Supply	Pos. supply of digital circuits
29	MCLK	Din with pull down	Master clock 128*FS / left open - enables PLL
31	LRCK	Din with pull down	I2S_Left/Right FrameClock = FS
32	SCLK	Din with pull down	I2S_Serial data clock >=38*FS
33	SDI	Din with pull down	I2S_Serial data 18bit left oriented, first bit fix L
36	CSCL	Din stt + spike supr	I2Ccomp_Serial clock to access control register
37	CSDA	Di/od stt + spike supr	I2Ccomp_Serial data to access control register
38	SDO	Dout_2mA	I2S_Serial data 14bit left orieted, first bit fix L
39	USBon	Dout_2mA	USB_indication of usb supply present
40	RCV	Dout_2mA	USB_differential receiver output
41	VP	Dout_2mA	USB_signle ended pos. receiver output
42	VM	Dout_2mA	USB_signle ended neg. receiver output
43	VPO	Din with pull down	USB_transmitter pos. input
44	VMO	Din with pull down	USB_transmitter neg. input
45	OEN	Din with pull up	USB_transmitter output enable (low active)
46	DVSS	Supply	Neg. supply of digital circuit
47	DP	Di/o with 1uA pd	USB_pos. I/O terminal
48	DM	Di/o with 1uA pd	USB_neg. I/O terminal
49	VTRM	Aout/Supply	USB_3.2V termination voltage regulator output
50	UVDD	Supply	USB_external supply 4-5.5V
51	AUX_R	Ain 40/200k to BGND	Analog aux input to audio amp Right channel
52	AUX_L	Ain 40/200k to BGND	Analog aux input to audio amp Left channel
53	PWRUP	Din 360k pull down	Enable LDO1 and 2 and DCDC
54	PLDO3	Din_5state	Selects one of 5 LDO3 states (L, 150kpd open, 150kpu, H)
55	MICP	Ain 15k to agnd	Microphone pos. input (MIC-ADC path)
56	MICN	Ain 15k to agnd	Microphone neg. input (MIC-ADC path)
57	VREF	Ai/o 10uF decpl	Reference voltage of DAC (AVDD)
58	AGND	Ai/o 10uF decpl	Reference voltage of DAC (AVDD/2)
59	AVSS	Supply	Neg. supply terminal of analog circuit
60	AVSS2	Supply	2nd Neg. supply terminal of analog circuit
64	AVDD	Aout/Supply	Pos. supply of analog circuits, LDO1 output – 2.9V
65	BGND	Ai/o 100nF decp	Reference voltage of power-amp (BVDD/2)
66	BVDD	Supply	Battery supply 3-5.5V
67	OUTR	Aout	Speaker/Headphone output (4 ohm min.)
68	BVSS	Supply	Neg. supply terminal of Power Amp.
69	OUTL	Aout	Speaker/Headphone output (4 ohm min.)
70	BVDD	Supply	Battery supply 3-5.5V
71	QLDO2	Aout	LDO2 output – 2.9V to be connected to DVDD
72	QLDO3	Aout	LDO3 output – 1.5...2.5V to be connected to PVDD
73	VSSDCDC	Supply	Power Ground for DCDC Converter
74	VSSDCDC	Supply	Power Ground for DCDC Converter
75	SWDCDC	Aout	Switch Output for DCDC Converter
76	SWDCDC	Aout	Switch Output for DCDC Converter
77	VB1V	Supply	Battery Supply Input (1V-3V)

Table 18 Table of Pin Configuration for TQFP80

Pin Configuration for CABGA 49

Ball#	BallName	Type	Function
F1	DVSS	Supply	Neg. supply of digital circuit
B2	PVDD	Supply	Supply of peripheral levelshifter of digital inputs
A2	DVDD	Supply	Pos. supply of digital circuits
G1	MCLK	Din with pull down	Master clock 128*FS / left open - enables PLL
D2	LRCK	Din with pull down	I2S_Left/Right FrameClock = FS
E2	SCLK	Din with pull down	I2S_Serial data clock >=38*FS
F2	SDI	Din with pull down	I2S_Serial data 18bit left oriented, first bit fix L
G2	CSCL	Din stt + spike supr	I2Ccomp_Serial clock to access control register
G3	CSDA	Di/od stt + spike supr	I2Ccomp_Serial data to access control register
F3	SDO	Dout_2mA	I2S_Serial data 14bit left orieted, first bit fix L
E3	USBon	Dout_2mA	USB_indication of usb supply present
G4	RCV	Dout_2mA	USB_differential receiver output
F4	VP	Dout_2mA	USB_signle ended pos. receiver output
E4	VM	Dout_2mA	USB_signle ended neg. receiver output
E5	VPO	Din with pull down	USB_transmitter pos. input
F5	VMO	Din with pull down	USB_transmitter neg. input
D5	OEN	Din with pull up	USB_transmitter output enable (low active)
G5	DVSS	Supply	Neg. supply of digital circuit
G6	DP	Di/o with 1uA pd	USB_pos. I/O terminal
G7	DM	Di/o with 1uA pd	USB_neg. I/O terminal
F6	VTRM	Aout/Supply	USB_3.2V termination voltage regulator output
F7	UVDD	Supply	USB_external supply 4-5.5V
D7	AUX_R	Ain 40/200k to BGND	Analog aux input to audio amp Right channel
D6	AUX_L	Ain 40/200k to BGND	Analog aux input to audio amp Left channel
E7	PWRUP	Din 360k pull down	Enable LDO1 and 2 and DCDC
E6	PLDO3	Din_5state	Selects one of 5 LDO3 states (L, 150kpd open, 150kpu, H)
C7	MICP	Ain 15k to agnd	Microphone pos. input (MIC-ADC path)
C6	MICN	Ain 15k to agnd	Microphone neg. input (MIC-ADC path)
C5	VREF	Ai/o 10uF decpl	Reference voltage of DAC (AVDD)
B6	AGND	Ai/o 10uF decpl	Reference voltage of DAC (AVDD/2)
B7	AVSS	Supply	Neg. supply terminal of analog circuit
A7	AVDD	Aout/Supply	Pos. supply of analog circuits, LDO1 output – 2.9V
A6	BGND	Ai/o 100nF decp	Reference voltage of power-amp (BVDD/2)
B5	BVDD	Supply	Battery supply 3-5.5V
A5	OUTR	Aout	Speaker/Headphone output (4 ohm min.)
A4, B4	BVSS	Supply	Neg. supply terminal of Power Amp.
A3	OUTL	Aout	Speaker/Headphone output (4 ohm min.)
B3	BVDD	Supply	Battery supply 3-5.5V
A1	VSSDCDC	Supply	Power Ground for DCDC Converter
B1	VSSDCDC	Supply	Power Ground for DCDC Converter
C1	SWDCDC	Aout	Switch Output for DCDC Converter
D1	SWDCDC	Aout	Switch Output for DCDC Converter
E1	VB1V	Supply	Battery Supply Input (1V-3V)
C2	n.c.		not connected
C3	n.c.		not connected
C4	n.c.		not connected
D4	n.c.		not connected

Table 19 Table of Pin Configuration for CABGA 49

	1	2	3	4	5	6	7
A	VSSDCDC	DVDD	OUTL	BVSS	OUTR	BGND	AVDD
B	VSSDCDC	PVDD	BVDD	BVSS	BVDD	AGND	AVSS
C	SWDCDC	n.c. (QPLL)	n.c. (RESET)	n.c.	VREF	MICN	MICP
D	SWDCDC	LRCLK	DACPD	n.c.	OEN	AUXL	AUXR
E	VB1V	SCLK	USB_ON	VM	VPO	PLDO3	PWRUP
F	DVSDS	SDI	SDO	VP	VMO	VTRM	UVDD
G	MCLK	CSCL	CSDA	RCV	DVSS	DP	DM

Figure 5 Figure of Pin Configuration

Mechanical Dimensions for CABGA 49

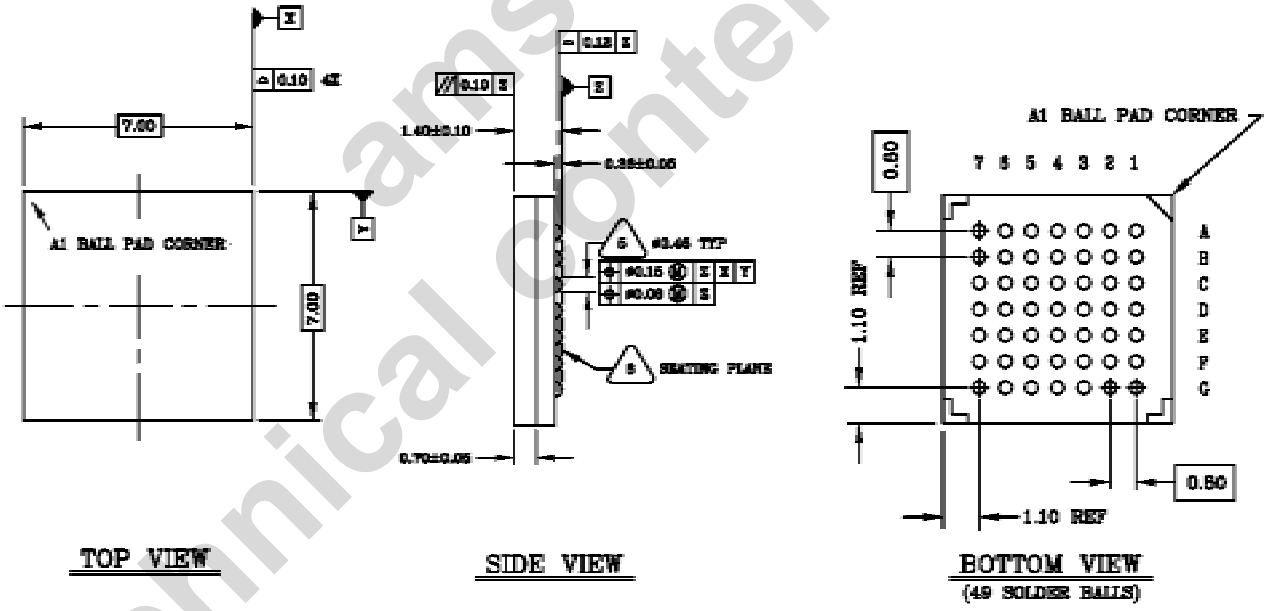

Figure 6 Mechanical Dimensions

Abbreviations

ADC	analog to digital converter
AGC	automatic gain control
DAC	digital to analog converter
dBFS	dB full scale
DSP	digital signalling processor
ENOB	effective number of bits
ESD	electrostatic discharge
I2S	inter IC sound
LDO	low drop regulator
PDA	personal digital assistance
PSRR	power supply rejection ratio
SFDR	spurious free dynamic range
SD	sigma delta
SNR	signal to noise ratio
SINAD	signal to noise and distortion (=THD+N)
TA	ambient temperature
THD	total harmonic distortion
uP	microprocessor
ΣΔ	sigma delta

Ordering Information

Number	Package	Description
AS3510	LQFP 80	Thin Quad Flat Pack - 80 leads (evaluation only)
	CABGA 49	ChipArray Ball Grid Array – 49 balls, 0.8mm pitch

Devices sold by austriamicrosystems AG are covered by the warranty and patent identification provisions appearing in its Term of Sale. austriamicrosystems AG makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. austriamicrosystems AG reserves the right to change specifications and prices at any time and without notice. Therefore, prior to designing this product into a system, it is necessary to check with austriamicrosystems AG for current information. This product is intended for use in normal commercial applications. Applications requiring extended temperature range, unusual environmental requirements, or high reliability applications, such as military, medical life-support or life-sustaining equipment are specifically not recommended without additional processing by austriamicrosystems AG for each application.

Copyright

The information furnished here by austriamicrosystems AG is believed to be correct and accurate. However, austriamicrosystems AG shall not be liable to recipient or any third party for any damages, including but not limited to personal injury, property damage, loss of profits, loss of use, interruption of business or indirect, special, incidental or consequential damages, of any kind, in connection with or arising out of the furnishing, performance or use of the technical data herein. No obligation or liability to recipient or any third party shall arise or flow out of austriamicrosystems AG rendering of technical or other services.

Contact

Headquarter

austriamicrosystems AG
Business Unit Communications
A 8141 Schloss Premstätten, Austria
T. +43 (0) 3136 5440
F. +43 (0) 3136 5692
accento@austriamicrosystems.com
www.austriamicrosystems.com

Sales Offices

austriamicrosystems Germany GmbH
Tegernseer Landstrasse 85
D-81539 München, Germany
Phone: +49/89/693643-0
Fax: +49/89/693643-66

austriamicrosystems France S.a.r.l.
124, Avenue de Paris
F-94300 Vincennes, France
Phone: +33/1/43 74 00 90
Fax: +33/1/43 74 20 98

austriamicrosystems Italy S.r.l.
Via Leone Tolstoi, 64
I-20146 Milano, Italy
Phone: +39/0242/36713
Fax: +39/0242/290889

austriamicrosystems Switzerland AG
Rietstrasse 4
CH-8640 Rapperswil, Switzerland
Phone: +41/55/220 9000
Fax: +41/55/220 9001

austriamicrosystems UK, Ltd.
Coliseum Business Centre, Watchmoor Park
Camberley, Surrey, GU15 3YL, United Kindom
Phone: +44/1276/23 3 99
Fax: +44/1276/29 3 53

austriamicrosystems USA, Inc.
Suite 116, 4030 Moorpark Ave,
San Jose, CA 95117, USA
Phone: +1/408/345 1790
Fax: +1/408/345 1795

austriamicrosystems USA, Inc.
Suite 400, 8601 Six Forks Road
Raleigh, NC 27615, USA
Phone: +1/919/676 5292
Fax: +1/919/676 5305

austriamicrosystems AG
AIOS Gotanda Annex 5th Fl.,
1-7-11,
Higashi-Gotanda, Shinagawa-ku,
Tokyo 141-0022 Japan
Phone: +81/3/5792 4975
Fax: +81/3/5792 4976

austriamicrosystems AG
Suite 811, Tsimshatsui Centre,
East Wing, 66 Mody Road,
Tsim Sha Tsui East,
Kowloon, Hong Kong
Phone: +852/2268 6899
Fax: +852/2268 6799

austriamicrosystems AG
Singapore Representative Office
83 Clemenceau Avenue
#02-01 UE Square
Singapore 239920
Phone: +65 68 30 83 05
Fax: +65 62 34 31 20

austriamicrosystems AG
#805, Dong Kyung Bldg., 824-19,
Yeok Sam Dong,
Kang Nam Gu, Seoul
Korea 135-080
Phone: +82/2/557 8776
Fax: +82/2/569 9823