

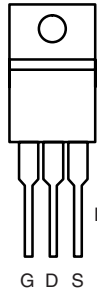
N-Channel 30-V (D-S), 175 °C MOSFET

| PRODUCT SUMMARY | | |
|-------------------|---------------------------|-----------------|
| $V_{(BR)DSS}$ (V) | $r_{DS(on)}$ (Ω) | I_D (A) |
| 30 | 0.004 | 75 ^a |

FEATURES

- TrenchFET[®] Power MOSFETs
- 175 °C Rated Maximum Junction Temperature

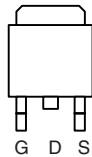

 Available
RoHS*
 COMPLIANT

TO-220AB


DRAIN connected to TAB

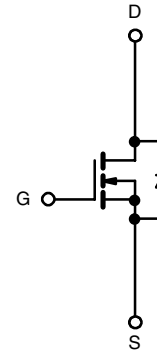
G D S

 Top View
 SUP75N03-04

TO-263


DRAIN connected to TAB

G D S

 Top View
 SUB75N03-04


N-Channel MOSFET

Ordering Information: SUP75N03-04
 SUP75N03-04-E3 (Lead (Pb)-free)
 SUB75N03-04
 SUB75N03-04-E3 (Lead (Pb)-free)

| ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted | | | | |
|--|--|----------------|------------------|------------------|
| Parameter | | Symbol | Limit | Unit |
| Gate-Source Voltage | | V_{GS} | ± 20 | V |
| Continuous Drain Current ($T_J = 175\text{ }^\circ\text{C}$) | $T_C = 25\text{ }^\circ\text{C}$ | I_D | 75 ^a | A |
| | $T_C = 125\text{ }^\circ\text{C}$ | | 75 ^a | |
| Pulsed Drain Current | | I_{DM} | 250 | |
| Pulse Diode Forward Current | | I_{SM} | 250 | |
| Continuous Source Current (Diode Conduction) | | I_S | 75 | |
| Avalanche Current | | I_{AR} | 75 | |
| Avalanche Energy | L = 0.1 mH | E_{AS} | 280 | |
| Repetitive Avalanche Energy ^b | L = 0.05 mH | E_{AR} | 140 | |
| Maximum Power Dissipation | $T_C = 25\text{ }^\circ\text{C}$ (TO-220AB and TO-263) | P_D | 187 ^c | W |
| | $T_A = 25\text{ }^\circ\text{C}$ (TO-263) ^d | | 3.7 | |
| Operating Junction and Storage Temperature Range | | T_J, T_{stg} | - 55 to 175 | $^\circ\text{C}$ |
| Lead Temperature ($1/16$ " from case for 10 sec.) | TO-220AB | T_L | 300 | |

| THERMAL RESISTANCE RATINGS | | | | |
|----------------------------|---------------------------------|------------|-------|--------------------|
| Parameter | | Symbol | Limit | Unit |
| Junction-to-Ambient | PCB Mount (TO-263) ^d | R_{thJA} | 40 | $^\circ\text{C/W}$ |
| | Free Air (TO-220AB) | | 62.5 | |
| Junction-to-Case | | R_{thJC} | 0.6 | |

Notes:

- Package limited.
- Duty cycle $\leq 1\%$.
- See SOA curve for voltage derating.
- When Mounted on 1" square PCB (FR-4 material).

 For SPICE model information via the Worldwide Web: <http://www.vishay.com/www/product/spice.htm>.

* Pb containing terminations are not RoHS compliant, exemptions may apply

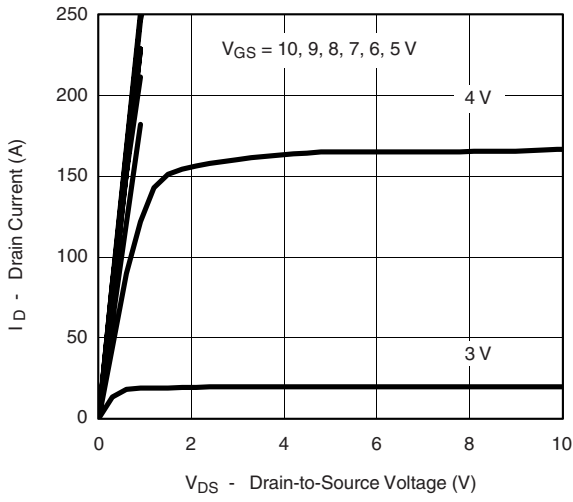
| SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted | | | | | | |
|---|---------------|--|-----|------------------|-----------|---------------|
| Parameter | Symbol | Test Conditions | Min | Typ ^a | Max | Unit |
| Static | | | | | | |
| Drain-Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$ | 30 | | | V |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$ | 1 | | 3 | |
| Gate-Body Leakage | I_{GSS} | $V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$ | | | ± 500 | nA |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$ | | | 1 | μA |
| | | $V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$ | | | 50 | |
| | | $V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 175\text{ }^\circ\text{C}$ | | | 200 | |
| On-State Drain Current ^b | $I_{D(on)}$ | $V_{DS} = 5\text{ V}, V_{GS} = 10\text{ V}$ | 120 | | | A |
| Drain-Source On-State Resistance ^b | $r_{DS(on)}$ | $V_{GS} = 10\text{ V}, I_D = 75\text{ A}$ | | 0.0034 | 0.004 | Ω |
| | | $V_{GS} = 4.5\text{ V}, I_D = 75\text{ A}$ | | 0.005 | 0.006 | |
| | | $V_{GS} = 10\text{ V}, I_D = 25\text{ A}, T_J = 125\text{ }^\circ\text{C}$ | | | 0.006 | |
| | | $V_{GS} = 10\text{ V}, I_D = 25\text{ A}, T_J = 175\text{ }^\circ\text{C}$ | | | 0.008 | |
| Forward Transconductance ^b | g_{fs} | $V_{DS} = 15\text{ V}, I_D = 25\text{ A}$ | 30 | | | S |
| Dynamic | | | | | | |
| Input Capacitance | C_{iss} | $V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1\text{ MHz}$ | | 10742 | | μF |
| Output Capacitance | C_{oss} | | | 1811 | | |
| Reverse Transfer Capacitance | C_{rss} | | | 775 | | |
| Total Gate Charge | Q_g | $V_{DS} = 30\text{ V}, V_{GS} = 10\text{ V}, I_D = 75\text{ A}$ | | 200 | 250 | nC |
| Gate-Source Charge | Q_{gs} | | | 40 | | |
| Gate-Drain Charge | Q_{gd} | | | 40 | | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD} = 30\text{ V}, R_L = 0.6\text{ }\Omega$ $I_D \cong 50\text{ A}, V_{GEN} = 10\text{ V}, R_G = 2.5\text{ }\Omega$ | | 20 | 40 | ns |
| Rise Time | t_r | | | 40 | | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | 190 | | |
| Fall Time | t_f | | | 95 | | |
| | | | | | | |
| Source-Drain Diode Ratings and Characteristics | | | | | | |
| Diode Forward Voltage ^b | V_{SD} | $I_F = 75\text{ A}, V_{GS} = 0\text{ V}$ | | | 1.3 | V |
| Reverse Recovery Time | t_{rr} | $I_F = 50\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$ | | 70 | 120 | ns |
| Peak Reverse Recovery Current | $I_{RM(rec)}$ | | | 2.8 | 6 | A |
| Reverse Recovery Charge | Q_{rr} | | | 0.1 | 0.36 | μC |

Notes:

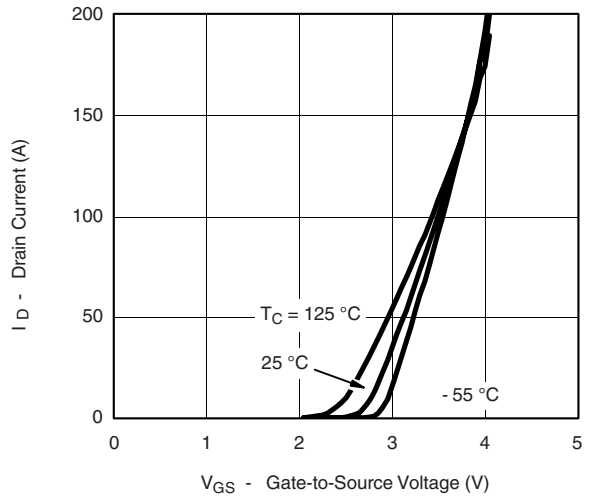
- a. For design aid only; not subject to production testing.
- b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

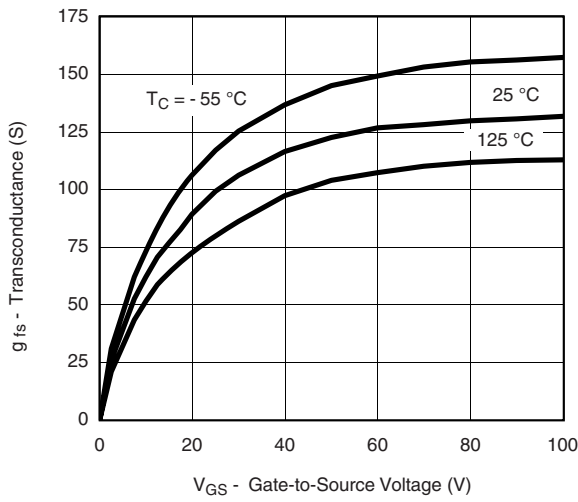
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



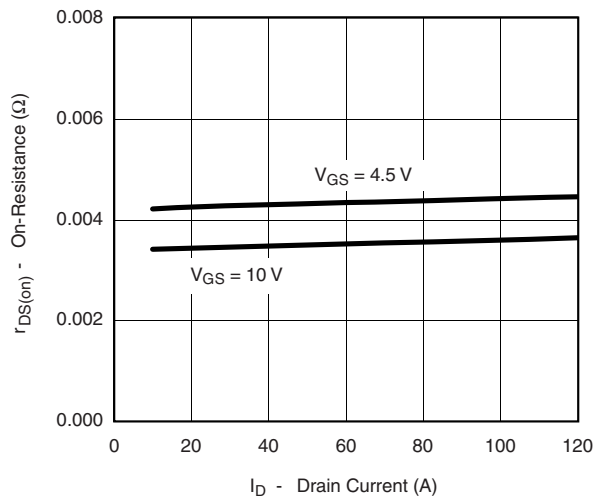
Output Characteristics



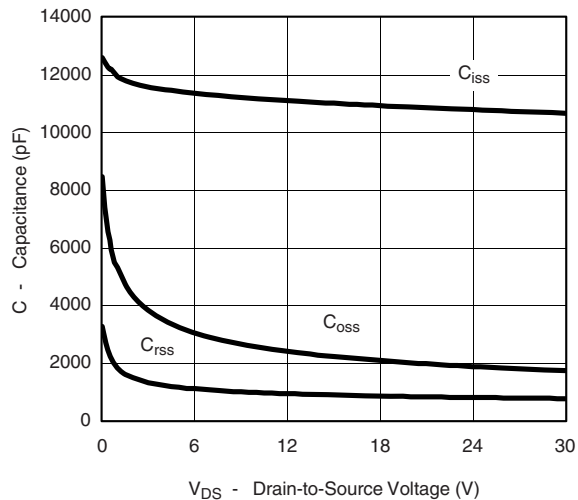
Transfer Characteristics



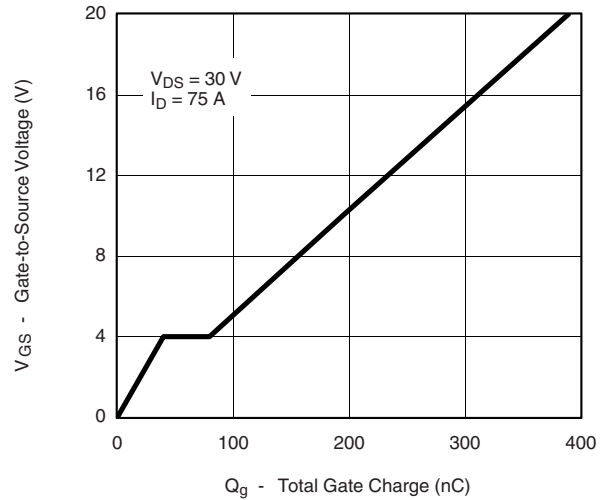
Transconductance



On-Resistance vs. Drain Current

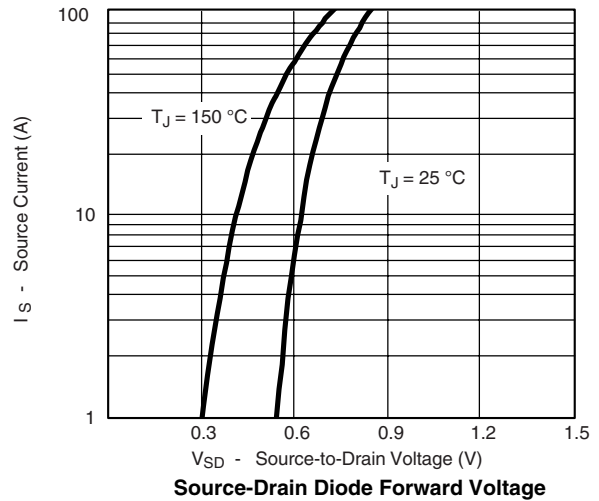
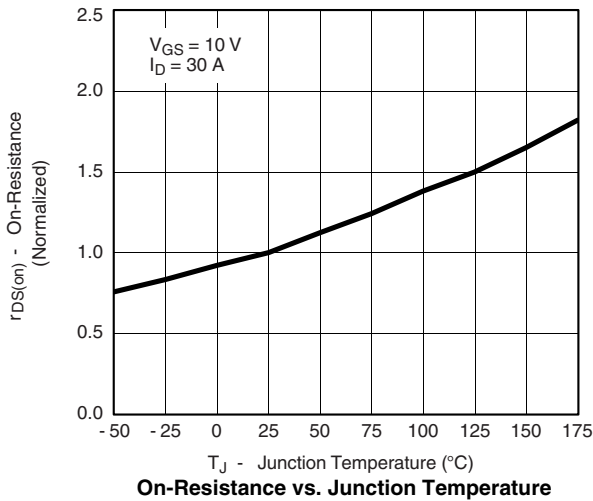


Capacitance

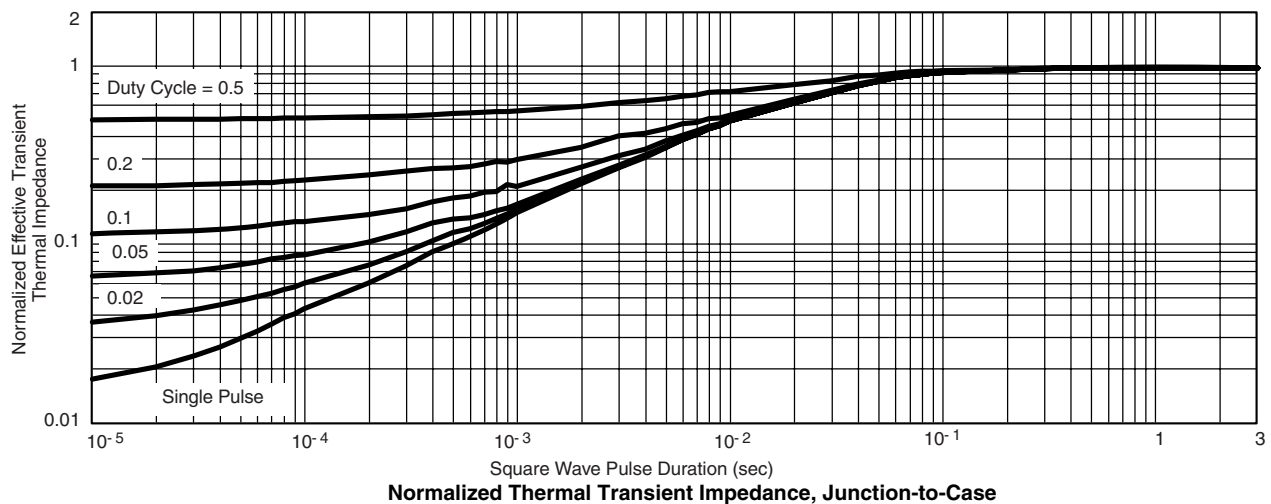
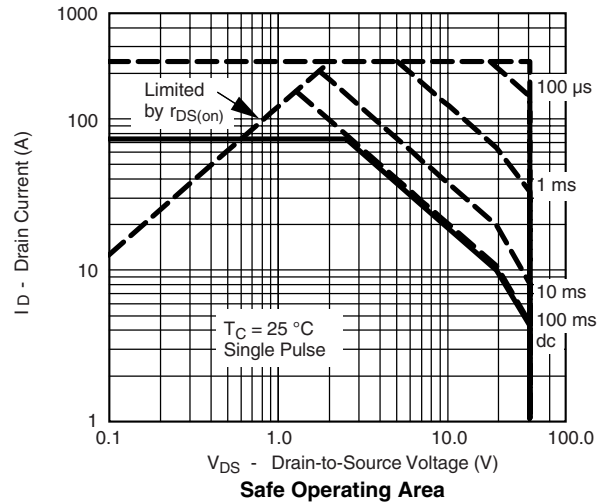
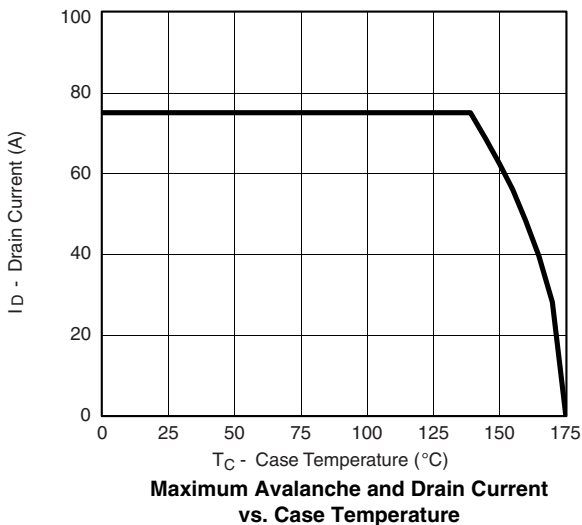


Gate Charge

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



THERMAL RATINGS



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?70745>.



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