FAIRCHILD SEMICONDUCTOR™

March 2001
Revised January 2005

NC7WZ125
TinyLogic® UHS Dual Buffer with 3-STATE Outputs

General Description

The NC7WZ125 is a Dual Non-Inverting Buffer with independent active LOW enables for the 3-STATE outputs. The Ultra High Speed device is fabricated with advanced CMOS technology to achieve superior switching performance with high output drive while maintaining low static power dissipation over a broad V_{CC} operating range. The device is specified to operate over the 1.65V to 5.5V V_{CC} operating range. The inputs and outputs are high impedance when V_{CC} is 0V. Inputs tolerate voltages up to 5.5V independent of V_{CC} operating range. Outputs tolerate voltages above V_{CC} when in the 3-STATE condition.

Features

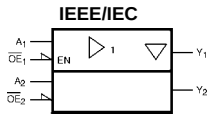
- Space saving US8 surface mount package
- MicroPak™ Pb-Free leadless package
- Ultra High Speed; t_{PD} 2.6 ns typ into 50 pF at 5V V_{CC}
- High Output Drive; ±24 mA at 3V V_{CC}
- Broad V_{CC} Operating Range; 1.65V to 5.5V
- Matches the performance of LCX when operated at 3.3V V_{CC}
- Power down high impedance inputs/outputs
- Overvoltage tolerant inputs facilitate 5V to 3V translation
- Outputs are overvoltage tolerant in 3-STATE mode
- Proprietary noise/EMI reduction circuitry implemented

Ordering Code:

Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
NC7WZ125K8X	MAB08A	WZ25	8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide	3k Units on Tape and Reel
NC7WZ125L8X	MAC08A	P3	Pb-Free 8-Lead MicroPak, 1.6 mm Wide	5k Units on Tape and Reel

Pb-Free package per JEDEC J-STD-020B.

Logic Symbol



Pin Descriptions

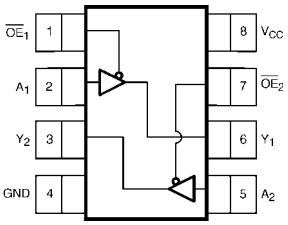
Pin Names	Description
$\overline{OE}_n$	Enable Inputs for 3-STATE Outputs
A_n	Input
Y_n	3-STATE Outputs

Function Table

Inputs		Output
$\overline{OE}$	A_n	Y_n
L	L	L
L	H	H
H	L	Z
H	H	Z

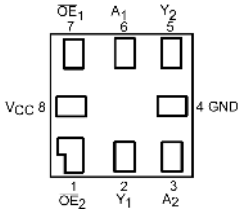
H = HIGH Logic Level L = LOW Logic Level Z = 3-STATE

Connection Diagrams



(Top View)

Pad Assignments for MicroPak



(Top Thru View)

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MicroPak™ is a trademark of Fairchild Semiconductor Corporation.

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	−0.5V to +7V
DC Input Voltage (V_{IN}) (Note 2)	−0.5V to +7V
DC Output Voltage (V_{OUT})	−0.5V to +7V
DC Input Diode Current (I_{IK})	
@V_{IN} < 0V	−50 mA
DC Output Diode Current (I_{OK})	
@V_{OUT} < 0V	−50 mA
DC Output Source/Sink Current (I_{OUT})	± 50 mA
DC V_{CC}/Ground Current (I_{CC}/I_{GND})	± 100 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Junction Lead Temperature under Bias (T_J)	+150°C
Junction Lead Temperature (T_L)	
(Soldering, 10 seconds)	+260°C
Power Dissipation (P_D) @ +85°C	250 mW

Recommended Operating Conditions (Note 3)

Supply Voltage Operating (V_{CC})	1.65V to 5.5V
Supply Voltage Data Retention (V_{CC})	1.5V to 5.5V
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	
Active State	0V to V_{CC}
3-STATE	0V to 5.5V
Operating Temperature (T_A)	−40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
V_{CC} @ 1.8V, 0.15V, 2.5V ± 0.2V	0 ns/V to 20 ns/V
V_{CC} @ 3.3V ± 0.3V	0 ns/V to 10 ns/V
V_{CC} @ 5.0V ± 0.5V	0 ns/V to 5 ns/V
Thermal Resistance (θ_{JA})	250°C/W

Note 1: Absolute maximum ratings are DC values beyond which the device may be damaged or have its useful life impaired. The datasheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside datasheet specifications.

Note 2: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 3: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = +25°C			T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	HIGH Level Input Voltage	1.65 to 1.95	0.75 V_{CC}			0.75 V_{CC}		V		
		2.3 to 5.5	0.7 V_{CC}			0.7 V_{CC}				
V_{IL}	LOW Level Input Voltage	1.65 to 1.95			0.25 V_{CC}		0.25 V_{CC}	V		
		2.3 to 5.5			0.3 V_{CC}		0.3 V_{CC}			
V_{OH}	HIGH Level Output Voltage	1.65	1.55	1.65		1.55		V	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −100 µA
		2.3	2.2	2.3		2.2				
		3.0	2.9	3.0		2.9				
		4.5	4.4	4.5		4.4				
		1.65	1.29	1.52		1.29		V	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −4 mA
		2.3	1.9	2.15		1.9				I_{OH} = −8 mA
		3.0	2.4	2.80		2.4				I_{OH} = −16 mA
		3.0	2.3	2.68		2.3				I_{OH} = −24 mA
		4.5	3.8	4.20		3.8				I_{OH} = −32 mA
V_{OL}	LOW Level Output Voltage	1.65		0.0	0.10		0.10	V	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100 µA
		2.3		0.0	0.10		0.10			
		3.0		0.0	0.10		0.10			
		4.5		0.0	0.10		0.10			
		1.65		0.08	0.24		0.24	V		I_{OL} = 4 mA
		2.3		0.10	0.3		0.3			I_{OL} = 8 mA
		3.0		0.15	0.4		0.4			I_{OL} = 16 mA
		3.0		0.22	0.55		0.55			I_{OL} = 24 mA
		4.5		0.22	0.55		0.55			I_{OL} = 32 mA
I_{IN}	Input Leakage Current	0 to 5.5			±0.1		±1	µA	V_{IN} = 5.5V, GND	
I_{OZ}	3-STATE Output Leakage	1.65 to 5.5			±0.5		±5	µA	V_{IN} = V_{IH} or V_{IL} 0 ≤ V_{OUT} ≤ 5.5V	
I_{OFF}	Power Off Leakage Current	0.0			1		10	µA	V_{IN} or V_{OUT} = 5.5V	
I_{CC}	Quiescent Supply Current	1.65 to 5.5			1		10	µA	V_{IN} = 5.5V, GND	

Noise Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$		Units	Conditions
			Typ	Max		
V_{OLP} (Note 4)	Quiet Output Maximum Dynamic V_{OL}	5.0		1.0	V	$C_L = 50$ pF
V_{OLV} (Note 4)	Quiet Output Minimum Dynamic V_{OL}	5.0		1.0	V	$C_L = 50$ pF
V_{OHV} (Note 4)	Quiet Output Minimum Dynamic V_{OH}	5.0		4.0	V	$C_L = 50$ pF
V_{IHD} (Note 4)	Minimum HIGH Level Dynamic Input Voltage	5.0		3.5	V	$C_L = 50$ pF
V_{ILD} (Note 4)	Maximum LOW Level Dynamic Input Voltage	5.0		1.5	V	$C_L = 50$ pF

Note 4: Parameter guaranteed by design.

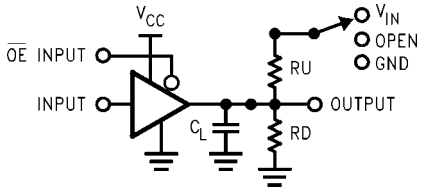
AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$			$T_A = -40°C$ to $+85°C$		Units	Conditions	Figure Number
			Min	Typ	Max	Min	Max			
t_{PLH}, t_{PHL}	Propagation Delay A_N to Y_N	1.8 ± 0.15	2.0		12.0	2.0	13.0	ns	$C_L = 15$ pF, $R_D = 1$ MΩ, S1= Open	Figures 1, 3
		2.5 ± 0.2	1.0		7.5	1.0	8.0			
		3.3 ± 0.3	0.8		5.2	0.8	5.5			
		5.0 ± 0.5	0.5		4.5	0.5	4.8			
t_{PLH}, t_{PHL}	Propagation Delay A_N to Y_N	3.3 ± 0.3	1.2		5.7	1.2	6.0	ns	$C_L = 50$ pF, $R_D = 500\Omega$, S1= Open	Figures 1, 3
		5.0 ± 0.5	0.8		5.0	0.8	5.3			
t_{OSLH}, t_{OSHL}	Output to Output Skew (Note 5)	3.3 ± 0.3			1.0		1.0	ns	$C_L = 50$ pF, $R_D = 500\Omega$, S1= Open	Figures 1, 3
		5.0 ± 0.5			0.8		0.8			
t_{PZL}, t_{PZH}	Output Enable Time	1.8 ± 0.15	3.0		14.0	3.0	15.0	ns	$C_L = 50$ pF, R_D, $R_U = 500\ \Omega$, S1 = GND for t_{PZH}, S1 = V_I for t_{PZL}, $V_I = 2 \times V_{CC}$	Figures 1, 3
		2.5 ± 0.2	1.8		8.5	1.8	9.0			
		3.3 ± 0.3	1.2		6.2	1.2	6.5			
		5.5 ± 0.5	0.8		5.5	0.8	5.8			
t_{PLZ}, t_{PHZ}	Output Disable Time	1.8 ± 0.15	2.5		12.0	2.5	13.0	ns	$C_L = 50$ pF, R_D, $R_U = 500\ \Omega$, S1 = GND for t_{PZH}, S1 = V_I for t_{PZL}, $V_I = 2 \times V_{CC}$	Figures 1, 3
		2.5 ± 0.2	1.5		8.0	1.5	8.5			
		3.3 ± 0.3	0.8		5.7	0.8	6.0			
		5.0 ± 0.5	0.3		4.7	0.3	5.0			
C_{IN}	Input Capacitance	0		2.5				pF		
C_{OUT}	Output Capacitance	5.0		4						
C_{PD}	Power Dissipation Capacitance	3.3		10				pF	(Note 6)	Figure 2
		5.0		12						

Note 5: Parameter guaranteed by design. $t_{OSLH} = |t_{PLHmax} - t_{PLHmin}|$; $t_{OSHL} = |t_{PHLmax} - t_{PHLmin}|$.

Note 6: C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure 2.) C_{PD} is related to I_{CCD} dynamic operating current by the expression: $I_{CCD} = (C_{PD})(V_{CC})(f_{IN}) + (I_{CC}\text{static})$.

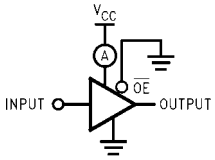
AC Loading and Waveforms



C_L includes load and stray capacitance

Input PRR = 1.0 MHz; t_w = 500 ns

FIGURE 1. AC Test Circuit



Input = AC Waveform; $t_r = t_f$ = 1.8 ns;

PRR = 10 MHz; Duty Cycle = 50%

FIGURE 2. I_{CCD} Test Circuit

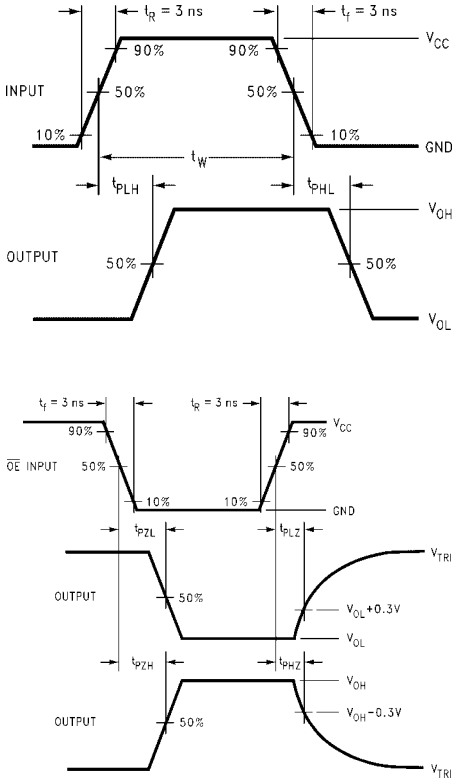


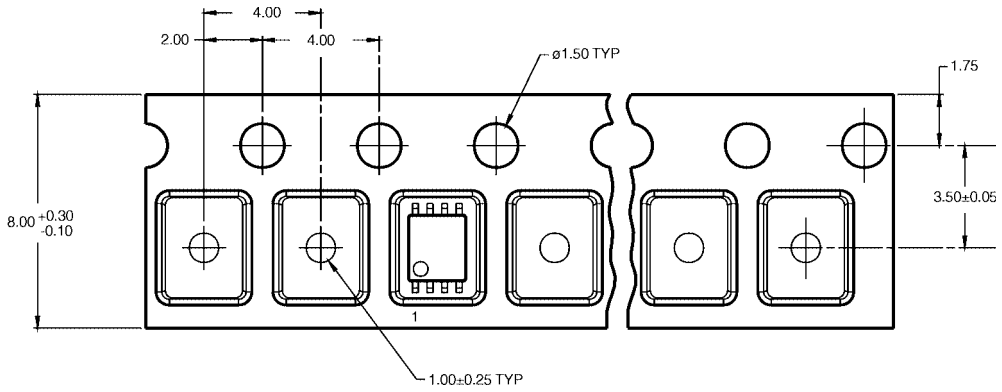
FIGURE 3. AC Waveforms

Tape and Reel Specification

Tape Format for US8

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
K8X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

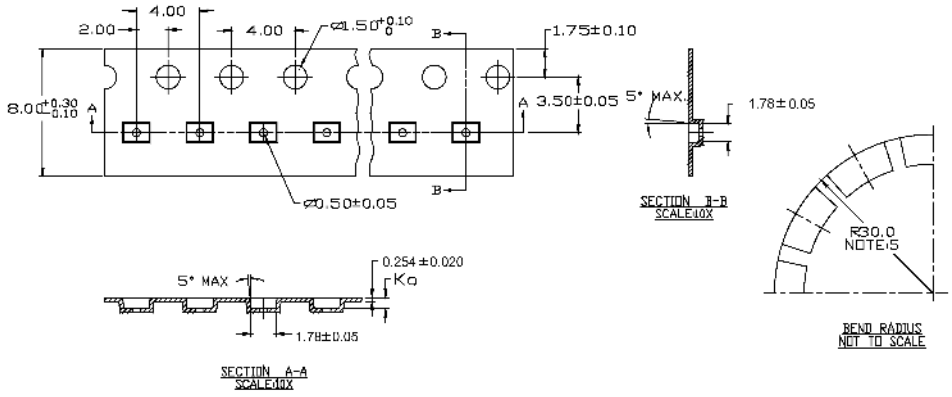
TAPE DIMENSIONS inches (millimeters)



Tape Format for MicroPak

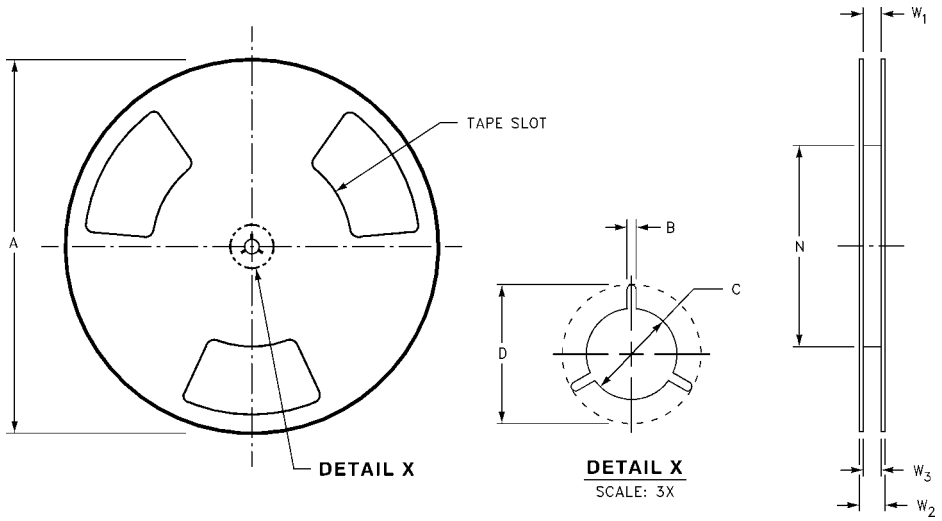
Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
L8X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

TAPE DIMENSIONS inches (millimeters)

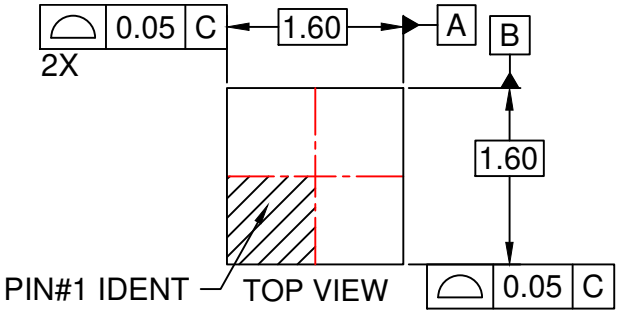


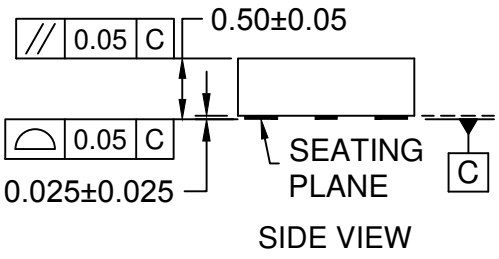
Tape and Reel Specification (Continued)

REEL DIMENSIONS inches (millimeters)

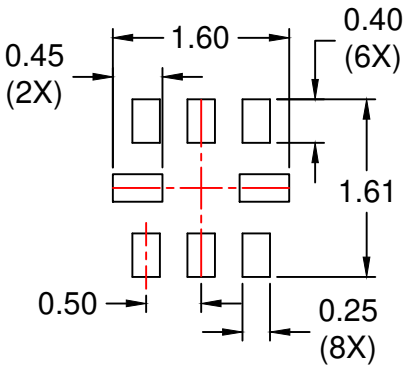


Tape Size	A	B	C	D	N	W1	W2	W3
8 mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.331 + 0.059/–0.000 (8.40 + 1.50/–0.00)	0.567 (14.40)	W1 + 0.078/–0.039 (W1 + 2.00/–1.00)

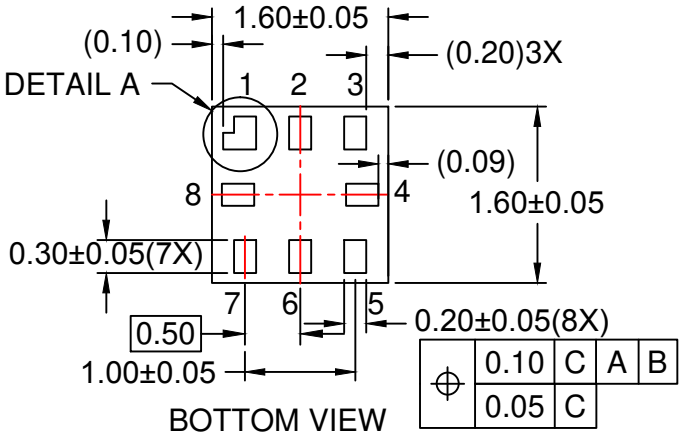




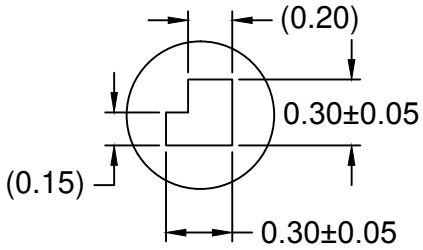
SIDE VIEW



RECOMMENDED
LAND PATTERN



BOTTOM VIEW



DETAIL A
SCALE : 2X

NOTES:

A. PACKAGE CONFORMS TO JEDEC MO-255 VARIATION UAAD.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

E. DRAWING FILENAME: MKT-MAC08Arev5.

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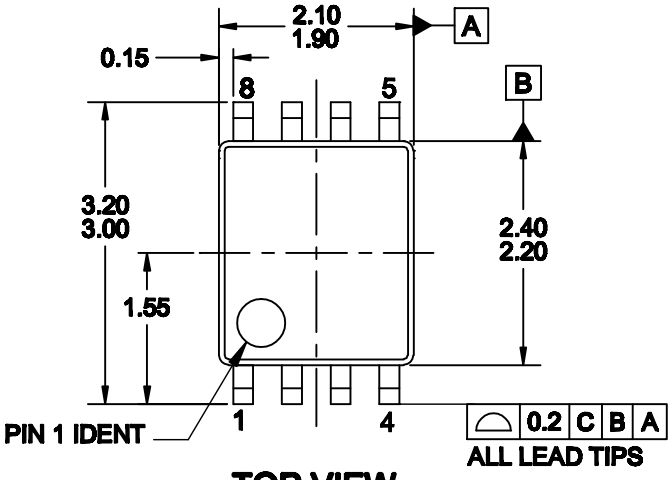
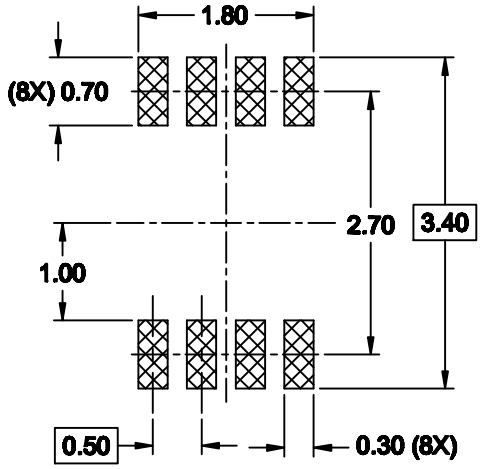


TOP VIEW



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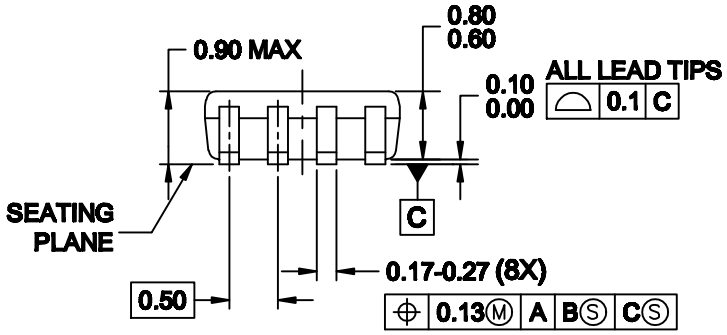

SIDE VIEW

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-187

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1994.

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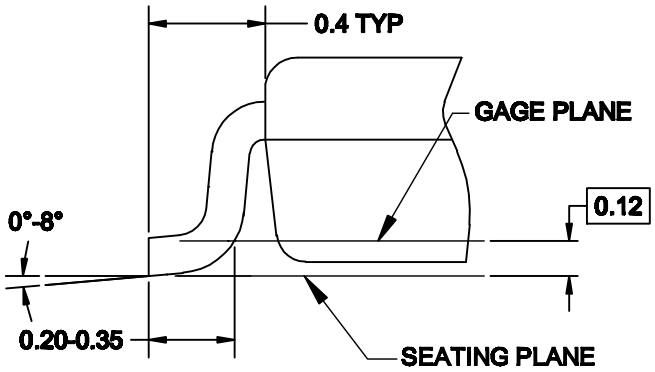
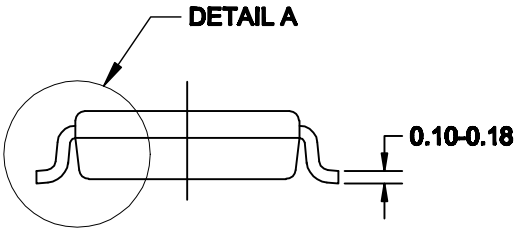


DETAIL A



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Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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