19-3389; Rev 0; 8/04

Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

General Description

The MAX9969 dual, low-power, high-speed, pin electronics driver/comparator with 35mA load IC includes, for each channel, a three-level pin driver, a dual comparator, variable clamps, and an active load. An additional differential comparator allows comparisons between the two channels. The driver features a wide voltage range and high-speed operation, includes high-impedance and active-termination (3rd-level drive) modes, and is highly linear even at low voltage swings. The dual comparator provides low dispersion (timing variation) over a wide variety of input conditions, and differential outputs. The clamps provide damping of high-speed device-under-test (DUT) waveforms when the device is configured as a high-impedance receiver. The programmable load supplies up to 35mA of source and sink current. The load facilitates contact/continuity testing, at-speed parametric testing of IOH and IOL, and pullup of high-output-impedance devices. The MAX9969A features tighter matching of offset for the drivers and the comparators.

The MAX9969 provides high-speed, differential control inputs with optional internal termination resistors that are compatible with LVPECL, LVDS, and GTL. Flexible open-collector outputs with optional internal pullup resistors are available for the comparators. These features significantly reduce the discrete component count on the circuit board.

A 3-wire, low-voltage, CMOS-compatible serial interface programs the low-leakage, slew-rate limit, and tri-state/terminate operational configurations of the MAX9969.

The MAX9969's operating range is -1.5V to +6.5V with power dissipation of only 1.4W per channel. The device is available in a 100-pin, 14mm x 14mm body, and 0.5mm pitch TQFP. An exposed 8mm x 8mm die pad on the top of the package facilitates efficient heat removal. The device is specified to operate with an internal die temperature of +60°C to +100°C, and features a die temperature monitor output.

Applications

High-Performance Mixed-Signal/ System-on-Chip ATE

High-Performance Memory ATE

Features

- **Low-Power Dissipation: 1.4W/Channel (typ)**
- **Greatly Reduced Power Penalty when Load Commutated**
- **High Speed: 1200Mbps at $3V_{P-P}$ and 1800Mbps at $1V_{P-P}$**
- **Programmable 35mA Active-Load Current**
- **Low Timing Dispersion**
- **Wide -1.5V to +6.5V Operating Range**
- **Active Termination (3rd-Level Drive)**
- **Low-Leakage Mode: 15nA**
- **Integrated Clamps**
- **Integrated Differential Comparator**
- **Interfaces Easily with Most Logic Families**
- **Digitally Programmable Slew Rate**
- **Internal Termination Resistors**
- **Low Offset Error**
- **Pin Compatible with the MAX9967**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9969ADCCQ	0°C to +70°C	100 TQFP-EPR**
MAX9969AGCCQ*	0°C to +70°C	100 TQFP-EPR**
MAX9969ALCCQ	0°C to +70°C	100 TQFP-EPR**
MAX9969ARCCQ*	0°C to +70°C	100 TQFP-EPR**
MAX9969BDCCQ	0°C to +70°C	100 TQFP-EPR**
MAX9969BGCCQ*	0°C to +70°C	100 TQFP-EPR**
MAX9969BLCCQ	0°C to +70°C	100 TQFP-EPR**
MAX9969BRCCQ	0°C to +70°C	100 TQFP-EPR**

*Future product—contact factory for availability.
**EPR = Exposed pad reversed (TOP).

Pin Configuration and Selector Guide appear at end of data sheet.

Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +11V
V_{EE} to GND .....-5.75V to +0.3V
V_{CC} - V_{EE} .....-0.3V to +16.75V
GS to GND .....±1V
DUT_ to GND .....-2.75V to +7.5V
LDH_, LDL_ to GND .....-0.3V to +6V
DATA_, NDATA_, RCV_, NRCV_, LDEN_, NLDEN_ to GND .....-2.5V to +5V
DATA_ to NDATA_, RCV_ to NRCV_, LDEN_ to NLDEN_ .....±1.5V
TDATA_, TRCV_, TLDEN_ to GND .....-2.5V to +5V
DATA_, NDATA_, to TDATA_ .....±2V
RCV_, NRCV_, to TRCV_ .....±2V
LDEN_, NLDEN_ to TLDEN_ .....±2V
$V_{CCO\_}$ to GND .....-0.3V to +5V
SCLK, DIN, $\overline{CS}$, $\overline{RST}$ to GND .....-1V to +5V
DHV_, DLV_, DTV_, CHV_, CLV_, COM_ to GND .....-2.5V to +7.5V
CPHV_ to GND .....-1V to +8.5V
CPLV_ to GND .....-3.5V to +6V
DHV_ to DLV_ .....±10V
DHV_ to DTV_ .....±10V
DLV_ to DTV_ .....±10V
CHV_ or CLV_ to DUT_ .....±10V
CH_, NCH_, CL_, NCL_ to GND .....-1V to +5V
All Other Pins to GND .....(V_{EE} - 0.3V) to (V_{CC} + 0.3V)
TEMP Current .....-0.5mA to +20mA
DUT_ Short Circuit to -1.5V to +6.5V .....Continuous
Continuous Power Dissipation (T_A = +70°C)
MAX9969_ _CCQ (derate 167mW/°C above +70°C) ...13.3W*
Storage Temperature Range .....-65°C to +150°C
Junction Temperature .....+125°C

**Dissipation wattage values are based on still air with no heat sink. Actual maximum power dissipation is a function of heat extraction technique and may be substantially higher.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +9.75V, V_{EE} = -4.75V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Positive Supply	V_{CC}		9.5	9.75	10.5	V
Negative Supply	V_{EE}		-5.25	-4.75	-4.50	V
Positive Supply Current (Note 2)	I_{CC}	$V_{LDH\_}$ = $V_{LDL\_}$ = 0, R_L ≥ 10MΩ		165	185	mA
		$V_{LDH\_}$ = $V_{LDL\_}$ = 3.5V, R_L = 0, $V_{COM\_}$ = 1.5V, load enabled, driver = high impedance		245	275	
Negative Supply Current (Note 2)	I_{EE}	$V_{LDH\_}$ = $V_{LDL\_}$ = 0, R_L ≥ 10MΩ		-235	-260	mA
		$V_{LDH\_}$ = $V_{LDL\_}$ = 3.5V, R_L = 0, $V_{COM\_}$ = -1V, load enabled, driver = high impedance		-315	-350	
Power Dissipation (Notes 2, 3)	P_D	$V_{LDH\_}$ = $V_{LDL\_}$ = 0		2.8	3.2	W
		$V_{LDH\_}$ = $V_{LDL\_}$ = 3.5V, R_L = 0, $V_{COM\_}$ = 1.5V, load enabled, driver = high impedance		3.3	3.7	
DUT_ CHARACTERISTICS						
Operating Voltage Range	V_{DUT}	(Note 4)	-1.5		+6.5	V
Leakage Current in High-Impedance Mode	I_{DUT}	LLEAK = 0; $V_{DUT\_}$ = -1.5V, 0, +3V, +6.5V			±3	µA
Leakage Current in Low-Leakage Mode		LLEAK = 1; $V_{DUT\_}$ = -1.5V, 0, +3V, +6.5V			±15	nA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -4.75V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Combined Capacitance	C_{DUT}	Driver in term mode (DUT_ = DTV_)		3	5	pF
		Driver in high-impedance mode		5	6	
Low-Leakage Enable Time		(Notes 5, 6)		20		µs
Low-Leakage Disable Time		(Notes 6, 7)		0.1		µs
Low-Leakage Recovery		Time to return to the specified maximum leakage after a 3V, 4V/ns step at DUT_ (Note 7)		4		µs
LEVEL PROGRAMMING INPUTS (DHV_, DLV_, DTV_, CHV_, CLV_, CPHV_, CPLV_, COM_, LDH_, LDL_)						
Input Bias Current	I_{BIAS}	MAX9969_RCCQ			±25	µA
Settling Time		To 0.1% of full scale change (Note 7)		1		µs
DIFFERENTIAL CONTROL INPUTS (DATA_, NDATA_, RCV_, NRCV_, LDEN_, NLDEN_)						
Input High Voltage	V_{IH}		0		3.5	V
Input Low Voltage	V_{IL}		-0.2		+3.1	V
Differential Input Voltage	V_{DIFF}	Between differential inputs	±0.15		±1.00	V
		Between a differential input and its termination voltage (Note 7)			±1.9	
Input Bias Current		MAX9969_DCCQ, MAX9969_RCCQ			±25	µA
Input Termination Voltage	$V_{TDATA\_}$ $V_{TRCV\_}$ $V_{TLDEN\_}$	MAX9969_GCCQ, MAX9969_LCCQ and MAX9969_RCCQ	0		+3.5	V
Input Termination Resistor		MAX9969_GCCQ, MAX9969_LCCQ, and MAX9969_RCCQ between signal and corresponding termination voltage input	47.5		52.5	Ω
SINGLE-ENDED CONTROL INPUTS ($\overline{CS}$, SCLK, DIN, $\overline{RST}$)						
Internal Threshold Reference	V_{THRINT}		1.05	1.25	1.45	V
Internal Reference Output Resistance	R_O			20		kΩ
External Threshold Reference	V_{THR}		0.43		1.73	V
Input High Voltage	V_{IH}		V_{THR} + 0.2		3.5	V
Input Low Voltage	V_{IL}		-0.1		V_{THR} - 0.2	V
Input Bias Current	I_B				±25	µA
SERIAL INTERFACE TIMING (Figure 5)						
SCLK Frequency	f_{SCLK}				50	MHz
SCLK Pulse-Width High	t_{CH}		8			ns
SCLK Pulse-Width Low	t_{CL}		8			ns
$\overline{CS}$ Low to SCLK High Setup	t_{CSS0}		3.5			ns
$\overline{CS}$ High to SCLK High Setup	t_{CSS1}		3.5			ns

Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -4.75V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SCLK High to $\overline{CS}$ High Hold	t_{CSH1}			3.5			ns
DIN to SCLK High Setup	t_{DS}			3.5			ns
DIN to SCLK High Hold	t_{DH}			3.5			ns
$\overline{CS}$ Pulse Width High	t_{CSWH}			20			ns
TEMPERATURE MONITOR (TEMP)							
Nominal Voltage		T_J = +70°C, $R_L \geq 10M\Omega$			3.33		V
Temperature Coefficient					+10		mV/°C
Output Resistance					20		kΩ
DRIVERS (Note 8)							
DC OUTPUT CHARACTERISTICS ($R_L \geq 10M\Omega$)							
DHV_, DLV_, DTV_, Output Offset Voltage	V_{OS}	At DUT_ with $V_{DHV\_}$, $V_{DTV\_}$, $V_{DLV\_}$ independently tested at +1.5V	MAX9969A			±15	mV
			MAX9969B			±100	
DHV_, DLV_, DTV_, Output Offset Temperature Coefficient					+200		µV/°C
DHV_, DLV_, DTV_, Gain	A_V	Measured with $V_{DHV\_}$, $V_{DLV\_}$, and $V_{DTV\_}$ at 0 and 4.5V		0.960		1.001	V/V
DHV_, DLV_, DTV_, Gain Temperature Coefficient					-50		ppm/°C
Linearity Error		$V_{DUT\_}$ = 1.5V, 3V (Note 9)				±5	mV
		Full range (Notes 9, 10)				±15	
DHV_ to DLV_ Crosstalk		$V_{DLV\_}$ = 0; $V_{DHV\_}$ = 200mV, 6.5V				±2	mV
DLV_ to DHV_ Crosstalk		$V_{DHV\_}$ = 5V; $V_{DLV\_}$ = -1.5V, +4.8V				±2	mV
DTV_ to DLV_ and DHV_ Crosstalk		$V_{DHV\_}$ = 3V; $V_{DLV\_}$ = 0; $V_{DTV\_}$ = -1.5V, +6.5V				±2	mV
DHV_ to DTV_ Crosstalk		$V_{DTV\_}$ = 1.5V; $V_{DLV\_}$ = 0; $V_{DHV\_}$ = 1.6V, 3V				±2	mV
DLV_ to DTV_ Crosstalk		$V_{DTV\_}$ = 1.5V; $V_{DHV\_}$ = 3V; $V_{DLV\_}$ = 0, 1.4V				±2	mV
DHV_, DTV_, DLV_ DC Power-Supply Rejection Ratio	PSRR	(Note 11)				±18	mV/V
Maximum DC Drive Current	$I_{DUT\_}$			±40		±80	mA
DC Output Resistance	$R_{DUT\_}$	$I_{DUT\_}$ = ±30mA (Note 12)		49	50	51	Ω
DC Output Resistance Variation	$\_R_{DUT\_}$	$I_{DUT\_}$ = ±1mA, ±8mA			0.5	1	Ω
		$I_{DUT\_}$ = ±1mA, ±8mA, ±15mA, ±40mA			0.75	1.5	
DYNAMIC OUTPUT CHARACTERISTICS (Z_L = 50Ω)							
AC Drive Current				±80			mA
Drive-Mode Overshoot		$V_{DLV\_}$ = 0, $V_{DHV\_}$ = 0.1V			15	22	mV
		$V_{DLV\_}$ = 0, $V_{DHV\_}$ = 1V			110	130	
		$V_{DLV\_}$ = 0, $V_{DHV\_}$ = 3V			210	370	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -4.75V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Drive-Mode Undershoot		$V_{DLV\_}$ = 0, $V_{DHV\_}$ = 0.1V			4	11	mV
		$V_{DLV\_}$ = 0, $V_{DHV\_}$ = 1V			20	65	
		$V_{DLV\_}$ = 0, $V_{DHV\_}$ = 3V			30	185	
Term-Mode Overshoot		(Note 13)	$V_{DUT\_}$ = 1.0V_{P-P}, t_R = t_F = 250ps 10% to 90%		60	150	mV
			$V_{DUT\_}$ = 3.0V_{P-P}, t_R = t_F = 500ps 10% to 90%		0		
Term-Mode Spike		$V_{DHV\_}$ = $V_{DTV\_}$ = 1V, $V_{DLV\_}$ = 0			180	250	mV
		$V_{DLV\_}$ = $V_{DTV\_}$ = 0, $V_{DHV\_}$ = 1V			180	250	
High-Impedance Mode Spike		$V_{DLV\_}$ = -1.0V, $V_{DHV\_}$ = 0			100		mV
		$V_{DLV\_}$ = 0, $V_{DHV\_}$ = 1V			100		
Settling Time to within 25mV		3V step (Note 14)			4		ns
Settling Time to within 5mV		3V step (Note 14)			40		ns
TIMING CHARACTERISTICS (Z_L = 50Ω) (Note 15)							
Prop Delay, Data to Output	t_{PDD}			1.5	1.7	2.0	ns
Prop Delay Match, t_{LH} vs. t_{HL}		3V_{P-P}			±40	±80	ps
Prop Delay Match, Drivers within Package		(Note 16)			40		ps
Prop Delay Temperature Coefficient					+1.6		ps/°C
Prop Delay Change vs. Pulse Width		0.2V_{P-P}, 40MHz, 0.6ns to 24.4ns pulse width, relative to 12.5ns pulse width	MAX9969_DCCQ		±70		ps
			MAX9969_GCCQ MAX9969_LCCQ MAX9969_RCCQ		±25	±50	
		1V_{P-P}, 40MHz, 0.6ns to 24.4ns pulse width, relative to 12.5ns pulse width	MAX9969_DCCQ		±70		
			MAX9969_GCCQ MAX9969_LCCQ MAX9969_RCCQ		±25	±50	
		3V_{P-P}, 40MHz, 0.9ns to 24.1ns pulse width, relative to 12.5ns pulse width	MAX9969_DCCQ		±80		
			MAX9969_GCCQ MAX9969_LCCQ MAX9969_RCCQ		±35	±60	
		5V_{P-P}, Z_L = 500Ω, 40MHz, 1.4ns to 23.6ns pulse width, relative to 12.5ns pulse width	MAX9969_DCCQ		±100		
			MAX9969_GCCQ MAX9969_LCCQ MAX9969_RCCQ		±100		

Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -4.75V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Prop Delay Change vs. Common-Mode Voltage		$V_{DHV\_}$ - $V_{DLV\_}$ = 1V, $V_{DHV\_}$ = 0 to 6V		50	75	ps
Prop Delay, Drive to High Impedance	t_{PDDZ}	$V_{DHV\_}$ = 1.0V, $V_{DLV\_}$ = -1.0V, $V_{DTV\_}$ = 0	2.0	2.3	2.6	ns
Prop Delay, High Impedance to Drive	t_{PDZD}	$V_{DHV\_}$ = 1.0V, $V_{DLV\_}$ = -1.0V, $V_{DTV\_}$ = 0	3.0	3.4	3.9	ns
Prop Delay Match, t_{PDDZ} vs. t_{PDZD}			-1.3	-1.1	-0.9	ns
Prop Delay Match, t_{PDDZ} vs. t_{LH}			0.4	0.6	0.8	ns
Prop Delay, Drive to Term	t_{PDDT}	$V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = 1.5V	1.7	2.0	2.3	ns
Prop Delay, Term to Drive	t_{PDTD}	$V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = 1.5V	2.0	2.3	2.7	ns
Prop Delay Match, t_{PDDT} vs. t_{PDTD}			0.5	0.3	0.1	ns
Prop Delay Match, t_{PDDT} vs. t_{LH}			0.1	0.3	0.5	ns
DYNAMIC PERFORMANCE (Z_L = 50Ω)						
Rise and Fall Time	t_R, t_F	$0.2V_{P-P}$, 10% to 90%	300	350	400	ps
		$1V_{P-P}$, 10% to 90%	330	390	450	
		$3V_{P-P}$, 10% to 90%	500	650	750	
		$5V_{P-P}$, Z_L = 500Ω, 10% to 90%	800	1000	1200	
Rise and Fall Time Match	t_R vs. t_F	$3V_{P-P}$, 10% to 90%		±50		ps
SC1 = 0, SC0 = 1 Slew Rate		Percent of full speed (SC0 = SC1 = 0), $3V_{P-P}$, 20% to 80%	63	70	77	%
SC1 = 1, SC0 = 0 Slew Rate		Percent of full speed (SC0 = SC1 = 0), $3V_{P-P}$, 20% to 80%	40	47	55	%
SC1 = 1, SC0 = 1 Slew Rate		Percent of full speed (SC0 = SC1 = 0), $3V_{P-P}$, 20% to 80%	18	25	32	%
Minimum Pulse Width		(Note 17), $0.2V_{P-P}$		550		ps
		(Note 17), $1V_{P-P}$		550	630	
		(Note 17), $3V_{P-P}$		850	1000	
		(Note 17), $5V_{P-P}$, Z_L = 500Ω		1300		
Data Rate		(Note 18), $0.2V_{P-P}$		1800		Mbps
		(Note 18), $1V_{P-P}$		1800		
		(Note 18), $3V_{P-P}$		1200		
		(Note 18), $5V_{P-P}$, Z_L = 500Ω		800		
Dynamic Crosstalk		(Note 19)		12		mV_{P-P}
Rise and Fall Time, Drive to Term	t_{DTR}, t_{DTF}	$V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = 1.5V, 10% to 90%, Figure 1a (Note 20)	0.6	1.0	1.3	ns
Rise and Fall Time, Term to Drive	t_{TDR}, t_{TDF}	$V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = 1.5V, 10% to 90%, Figure 1b (Note 20)	0.6	1.0	1.3	ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -4.75V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
COMPARATORS (Note 8)							
DC CHARACTERISTICS							
Input Voltage Range	V_{IN}	(Note 4)		-1.5		+6.5	V
Differential Input Voltage	V_{DIFF}			±8			V
Hysteresis	V_{HYST}				0		mV
Input Offset Voltage	V_{OS}	$V_{DUT\_}$ = 1.5V	MAX9969A			±20	mV
			MAX9969B			±100	
Input Offset Voltage Temperature Coefficient					±10		µV/°C
Common-Mode Rejection Ratio	CMRR	$V_{DUT\_}$ = -1.5V, +6.5V (Note 21)			±0.25	±2	mV/V
Linearity Error		(Note 10)	$V_{DUT\_}$ = 1.5V, 3V			±3	mV
			$V_{DUT\_}$ = -1.5V, +6.5V			±10	
Power-Supply Rejection Ratio	PSRR	$V_{DUT\_}$ = 1.5V (Note 11)			±0.035	±2	mV/V
AC CHARACTERISTICS (Note 22)							
Bandwidth		Term mode, t_R = t_F = 150ps		2	3		GHz
		High-impedance mode		0.65	0.75		
Minimum Pulse Width	$t_{PW(MIN)}$	(Note 23)	MAX9969_LCCQ and MAX9969_RCCQ		500	650	ps
			MAX9969_DCCQ and MAX9969_GCCQ		600		
Prop Delay	t_{PDL}			1.0	1.3	1.6	ns
Prop Delay Temperature Coefficient					+1.7		ps/°C
Prop Delay Match, High/Low vs. Low/High					±10	±50	ps
Prop Delay Match High vs. Low Comparator					±50		ps
Prop Delay Match, Comparators within Package		(Note 16)			±80		ps
Prop Delay Dispersion vs. Common-Mode Input		$V_{CHV\_}$ = $V_{CLV\_}$ = -1.4V to +6.4V (Note 24)			40	60	ps
Prop Delay Dispersion vs. Overdrive		$V_{CHV\_}$ = $V_{CLV\_}$ = 0.1V to 0.9V, $V_{DUT\_}$ = $1V_{P-P}$, t_R = t_F = 250ps, 10% to 90% relative to timing at 50% point			±40	±60	ps
		$V_{CHV\_}$ = $V_{CLV\_}$ = 40mV to 160mV, $V_{DUT\_}$ = $0.2V_{P-P}$, t_R = t_F = 150ps, 10% to 90% relative to timing at 50% point			±40	±60	
Prop Delay Dispersion vs. Pulse Width		0.6ns to 24.4ns pulse width, relative to 12.5ns pulse width			±30	±50	ps

Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -4.75V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Prop Delay Dispersion vs. Slew Rate		0.5V/ns to 6V/ns slew rate, relative to 4V/ns slew rate		±30	±60	ps
Waveform Tracking 10% to 90%		$V_{DUT\_}$ = 1.0V_{P-P}, t_R = t_F = 250ps, 10% to 90% relative to timing at 50% point, term mode		±40	±60	ps
		$V_{DUT\_}$ = 1.0V_{P-P}, t_R = t_F = 250ps, 10% to 90% relative to timing at 50% point, high-impedance mode		±190	±250	
		$V_{DUT\_}$ = 3V_{P-P}, t_R = t_F = 500ps, 10% to 90% relative to timing at 50% point, high-impedance mode		±150	±200	
DUT_ Slew-Rate Tracking		Term mode		6		V/ns
		High-impedance mode		5		
LOGIC OUTPUTS (CH_, NCH_, CL_, NCL_)						
$V_{CCO\_}$ Voltage Range	$V_{VCCO\_}$		0		3.5	V
$V_{CCO\_}$ Current	$I_{VCCO\_}$			32		mA
Output Low Voltage Compliance		Set by I_{OL}, R_{TERM}, and $V_{CCO\_}$		-0.5		V
Output High Current	I_{OH}	MAX9969_DCCQ, MAX9969_GCCQ	-0.1		+0.3	mA
Output Low Current	I_{OL}	MAX9969_DCCQ, MAX9969_GCCQ		8		mA
Output Current Swing		MAX9969_DCCQ, MAX9969_GCCQ	7.6		8.4	mA
Output High Voltage	V_{OH}	$I_{CH\_}$ = $I_{NCH\_}$ = $I_{CL\_}$ = $I_{NCL\_}$ = 0, MAX9969_LCCQ, MAX9969_RCCQ	$V_{CCO\_}$ - 0.05	$V_{CCO\_}$ - 0.005	$V_{CCO\_}$ + 0.01	V
Output Low Voltage	V_{OL}	$I_{CH\_}$ = $I_{NCH\_}$ = $I_{CL\_}$ = $I_{NCL\_}$ = 0, MAX9969_LCCQ, MAX9969_RCCQ		$V_{CCO\_}$ - 0.4		V
Output Voltage Swing		$I_{CH\_}$ = $I_{NCH\_}$ = $I_{CL\_}$ = $I_{NCL\_}$ = 0, MAX9969_LCCQ, MAX9969_RCCQ	380	400	420	mV
Output Termination Resistor	R_{TERM}	Single-ended measurement from $V_{CCO\_}$ to CH_, NCH_, CL_, NCL_, MAX9969_LCCQ, MAX9969_RCCQ	48		52	Ω
Differential Rise and Fall Times	t_R, t_F	20% to 80%, MAX9969_DCCQ, MAX9969_GCCQ, R_{TERM} = 50Ω at end of line		240		ps
		20% to 80%, MAX9969_LCCQ, MAX9969_RCCQ		190	230	
CLAMPS						
High Clamp Input Voltage Range	$V_{CPH\_}$		0		+7.5	V
Low Clamp Input Voltage Range	$V_{CPL\_}$		-2.5		+5.0	V
Clamp Offset Voltage	V_{OS}	At DUT_ with $I_{DUT\_}$ = 1mA, $V_{CPHV\_}$ = 0			±100	mV
		At DUT_ with $I_{DUT\_}$ = -1mA, $V_{CPLV\_}$ = 0			±100	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -4.75V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Offset-Voltage Temperature Coefficient					±250		µV/°C
Clamp Power-Supply Rejection Ratio	PSRR	(Note 11)	$I_{DUT\_}$ = 1mA, $V_{CPHV\_}$ = 0		±10		mV/V
			$I_{DUT\_}$ = -1mA, $V_{CPLV\_}$ = 0		±10		
Voltage Gain	A_V			0.960		1.005	V/V
Voltage-Gain Temperature Coefficient					-30		ppm/°C
Clamp Linearity		$I_{DUT\_}$ = 1mA, $V_{CPLV\_}$ = -1.5V, $V_{CPHV\_}$ = 0 to 6.5V			±10		mV
		$I_{DUT\_}$ = -1mA, $V_{CPHV\_}$ = 6.5V, $V_{CPLV\_}$ = -1.5V to +5V			±10		
Short-Circuit Output Current	$I_{SCDUT\_}$	$V_{CPHV\_}$ = 0, $V_{CPLV\_}$ = -1.5V, $V_{DUT\_}$ = 6.5V		40		80	mA
		$V_{CPHV\_}$ = 6.5V, $V_{CPLV\_}$ = 5V, $V_{DUT\_}$ = -1.5V		-80		-40	
Clamp DC Impedance	R_{OUT}	$V_{CPHV\_}$ = 3V, $V_{CPLV\_}$ = 0, $I_{DUT\_}$ = ±5mA and ±15mA		50		55	Ω
Clamp DC Impedance Variation		$V_{CPHV\_}$ = 2.5V; $V_{CPLV\_}$ = -1.5V; $I_{DUT\_}$ = 10mA, 20mA, 30mA			1.5		Ω
		$V_{CPHV\_}$ = 6.5V; $V_{CPLV\_}$ = 2.5V; $I_{DUT\_}$ = -10mA, -20mA, -30mA			1.5		
ACTIVE LOAD ($V_{COM\_}$ = 1.5V, R_L > 1MΩ, driver in high-impedance mode unless otherwise noted)							
COM_ Voltage Range	$V_{COM\_}$			-1		+6	V
Differential Voltage Range		$V_{DUT\_}$ - $V_{COM\_}$		-7.5		+7.5	V
COM_ Offset Voltage	Vos	I_{SOURCE} = I_{SINK} = 20mA				±100	mV
Offset-Voltage Temperature Coefficient					+100		µV/°C
COM_ Voltage Gain	A_V	$V_{COM\_}$ = 0, 4.5V; I_{SOURCE} = I_{SINK} = 20mA		0.98		1.00	V/V
Voltage-Gain Temperature Coefficient					-10		ppm/°C
COM_ Linearity Error		$V_{COM\_}$ = -1V, +6V; I_{SOURCE} = I_{SINK} = 20mA			±3	±15	mV
COM_ Output Voltage Power-Supply Rejection Ratio	PSRR	$V_{COM\_}$ = 2.5V, I_{SOURCE} = I_{SINK} = 20mA				±10	mV/V

Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -4.75V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Resistance, Sink or Source	Ro	$V_{DUT\_}$ = 3V, 6.5V with $V_{COM\_}$ = -1V and $V_{DUT\_}$ = -1.5V, +2V with $V_{COM\_}$ = 6V	I_{SOURCE} = I_{SINK} = 35mA	30			kΩ
			I_{SOURCE} = I_{SINK} = 1mA	500			
Output Resistance, Linear Region	Ro	$I_{DUT\_}$ = ±33.25mA, I_{SOURCE} = I_{SINK} = 35mA, $V_{COM\_}$ = 2.5V verfied by deadband test			11	15	Ω
Deadband		$V_{COM\_}$ = 2.5V, 95% I_{SOURCE} to 95% I_{SINK}			700	800	mV
SOURCE CURRENT ($V_{DUT\_}$ = 4.5V)							
Maximum Source Current		$V_{LDL\_}$ = 3.8V		36		40	mA
Source Programming Gain	ATC	$V_{LDL\_}$ = 0.2V, 3V; $V_{LDH\_}$ = 0.1V		9.75	10	10.25	mA/V
Source Current Offset (Combined Offset of LDL_ and GS)	I_{OS}	$V_{LDL\_}$ = 200mV		-1000		0	µA
Source-Current Temperature Coefficient		I_{SOURCE} = 35mA			-15		µA/°C
Source-Current Power-Supply Rejection Ratio	PSRR	I_{SOURCE} = 25mA				±60	µA/V
		I_{SOURCE} = 35mA				±84	
Source Current Linearity		(Note 25)	$V_{LDL\_}$ = 100mV, 1V, 2.25V			±60	µA
			$V_{LDL\_}$ = 3V			±130	
SINK CURRENT ($V_{DUT\_}$ = -1.5V)							
Maximum Sink Current		$V_{LDH\_}$ = 3.8V		-40		-36	mA
Sink Programming Gain	ATC	$V_{LDH\_}$ = 0.2V, 3V; $V_{LDL\_}$ = 0.1V		-10.25	-10	-9.75	mA/V
Sink-Current Offset (Combined Offset of LDH_ and GS)	I_{OS}	$V_{LDH\_}$ = 200mV		0		1000	µA
Sink-Current Temperature Coefficient		I_{SINK} = 35mA			+8		µA/°C
Sink-Current Power-Supply Rejection Ratio	PSRR	I_{SINK} = 25mA				±60	µA/V
		I_{SINK} = 35mA				±84	
Sink-Current Linearity		(Note 25)	$V_{LDH\_}$ = 100mV, 1V, 2.25V			±60	µA
			$V_{LDH\_}$ = 3V			±130	
GROUND SENSE							
GS Voltage Range	V_{GS}	Verified by GS common-mode error test		±250			mV
GS Common-Mode Error		$V_{DUT\_}$ = -1.5V, V_{GS} = ±250mV, $V_{LDH\_}$ - V_{GS} = 0.2V				±20	µA
		$V_{DUT\_}$ = +4.5V, V_{GS} = ±250mV, $V_{LDL\_}$ - V_{GS} = 0.2V				±20	
GS Input Bias Current		V_{GS} = 0				±25	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -4.75V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
AC CHARACTERISTICS (Z_L = 50Ω to GND)							
Enable Time	t_{EN}	(Note 26)	I_{SOURCE} = 10mA, $V_{COM\_}$ = -1V	3	3.5	4	ns
			I_{SINK} = 10mA, $V_{COM\_}$ = 1V	3	3.5	4	
Disable Time	t_{DIS}	(Note 26)	I_{SOURCE} = 10mA, $V_{COM\_}$ = 1V	1.7	2	2.3	ns
			I_{SINK} = 10mA, $V_{COM\_}$ = -1V	1.7	2	2.3	
Current Settling Time on Commutation		I_{SOURCE} = I_{SINK} = 1mA (Note 27)	To 10%		15		ns
			To 1.5%		50		
		I_{SOURCE} = I_{SINK} = 20mA (Note 27)	To 10%		3	5	
			To 1.5%		15		
Spike During Enable/Disable Transition		I_{SOURCE} = I_{SINK} = 35mA, $V_{COM\_}$ = 0			200	300	mV

Note 1: All minimum and maximum DC and driver 3V rise- and fall-time test limits are 100% production tested. All other test limits are guaranteed by design. Tests are performed at nominal supply voltages, unless otherwise noted.

Note 2: Total for dual device at worst-case setting.

Note 3: Does not include above ground internal dissipation of the comparator outputs. Additional power dissipation is typically (32mA x $V_{VCCO\_}$)

Note 4: Externally forced voltages may exceed this range provided that the Absolute Maximum Ratings are not exceeded.

Note 5: Transition time from LLEAK being asserted to leakage current dropping below specified limits.

Note 6: Based on simulation results only.

Note 7: Transition time from LLEAK being deasserted to output returning to normal operating mode.

Note 8: With the exception of offset and gain/CMRR tests, reference input values are calibrated for offset and gain.

Note 9: Specifications measured at the endpoints of the full range. Full range is -1.3V ≤ $V_{DHV\_}$ ≤ +6.5V, -1.5V ≤ $V_{DLV\_}$ ≤ +6.3V, -1.5V ≤ $V_{DTV\_}$ ≤ +6.5V.

Note 10: Relative to straight line between 0 and 4.5V.

Note 11: Change in offset voltage with power supplies independently set to their minimum and maximum values.

Note 12: Nominal target value is 50Ω. Contact factory for alternate trim selections within the 45Ω to 51Ω range.

Note 13: $V_{DTV\_}$ = midpoint of voltage swing, R_S = 50Ω. Measurement is made using the comparator.

Note 14: Measured from the crossing point of DATA_ inputs to the settling of the driver output.

Note 15: Prop delays are measured from the crossing point of the differential input signals to the 50% point of the expected output swing. Rise time of the differential inputs DATA_ and RCV_ are 250ps (10% to 90%).

Note 16: Rising edge to rising edge or falling edge to falling edge.

Note 17: Specified amplitude is programmed. At this pulse width, the output reaches at least 90% of its nominal (DC) amplitude. The pulse width is measured at DATA_.

Note 18: Specified amplitude is programmed. Maximum data rate is specified in transitions per second. A square wave that reaches at least 90% of its programmed amplitude may be generated at one-half of this frequency.

Note 19: Crosstalk from either driver to the other. Aggressor channel is driving $3V_{P-P}$ into a 50Ω load. Victim channel is in term mode with $V_{DTV\_}$ = +1.5V.

Note 20: Indicative of switching speed from DHV_ or DLV_ to DTV_ and DTV_ to DHV_ or DLV_ when $V_{DLV\_}$ < $V_{DTV\_}$ < $V_{DHV\_}$. If $V_{DTV\_}$ < $V_{DLV\_}$ or $V_{DTV\_}$ > $V_{DHV\_}$, switching speed is degraded by a factor of approximately 3.

Note 21: Change in offset voltage over the input range.

Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -4.75V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

Note 22: Unless otherwise noted, all propagation delays are measured at 40MHz, $V_{DUT\_}$ = 0 to +1V, $V_{CHV\_}$ = $V_{CLV\_}$ = +0.5V, t_R = t_F = 250ps, Z_S = 50Ω, driver in term mode with $V_{DTV\_}$ = +0.5V. Comparator outputs are terminated with 50Ω to 1.25V and $V_{CCO\_}$ = 2.5V. Measured from $V_{DUT\_}$ crossing calibrated CHV_/CLV_ threshold to crossing point of differential outputs.

Note 23: At this pulse width, the output reaches at least 90% of its DC voltage swing. The pulse width is measured at the crossing points of the differential outputs.

Note 24: $V_{DUT\_}$ = 200mV_{P-P}. Overdrive = 100mV.

Note 25: Relative to segmented interpolations between 200mV, 2V, 2.5V, and 3.5V.

Note 26: Measured from crossing of LDEN_ inputs to the 50% point of the output current change.

Note 27: V_{COM} = 1V, R_S = 50Ω, driving voltage = 1.55V to 0.45V transition and 0.45V to 1.55V transition (at 1mA) or +2.5V to -0.5V transition and -0.5V to +2.5V transition (at 20mA). Settling time is measured from $V_{DUT\_}$ = 1V to I_{SINK}/I_{SOURCE} settling within specified tolerance.

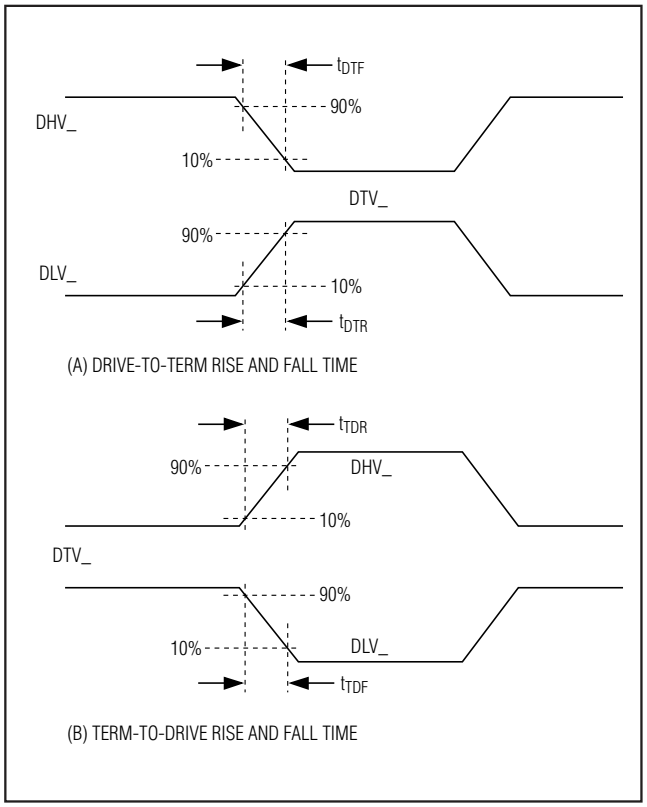


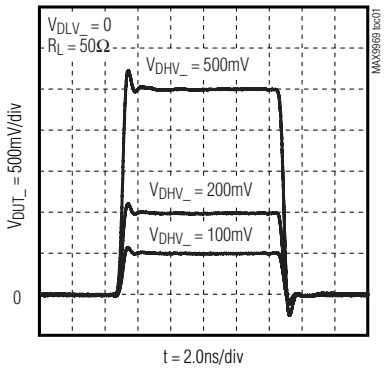
Figure 1. Drive-to-Term and Term-to-Drive Rise and Fall Times

Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

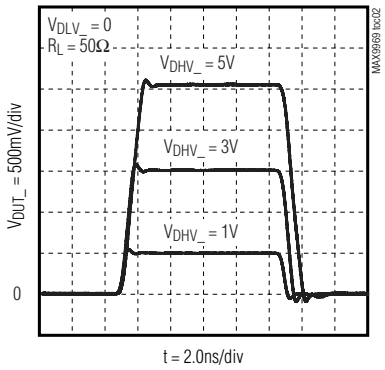
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

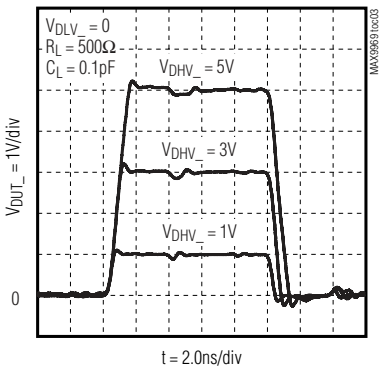
DRIVER SMALL-SIGNAL RESPONSE



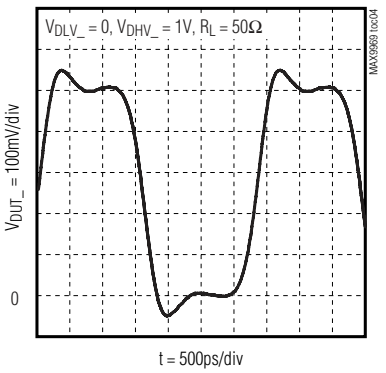
DRIVER LARGE-SIGNAL RESPONSE



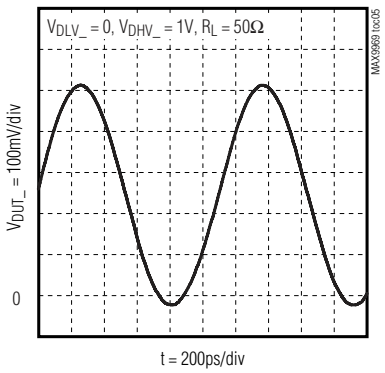
DRIVER LARGE-SIGNAL RESPONSE INTO 500Ω



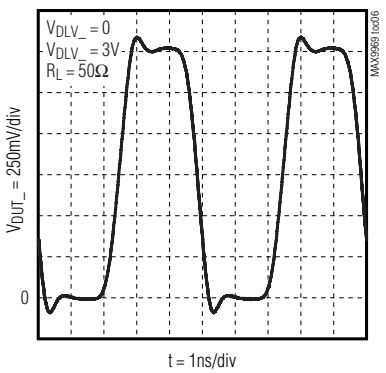
DRIVER 1V 600Mbps SIGNAL RESPONSE



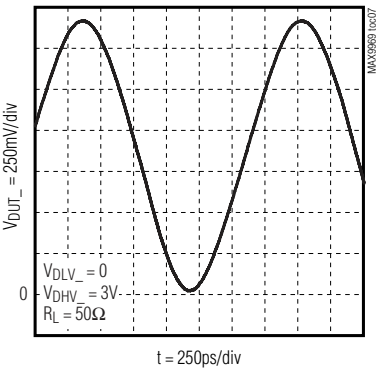
DRIVER 1V 1800Mbps SIGNAL RESPONSE



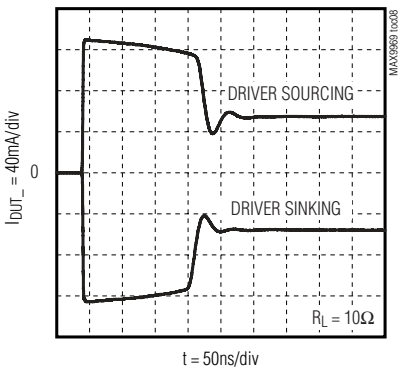
DRIVER 3V 400Mbps SIGNAL RESPONSE



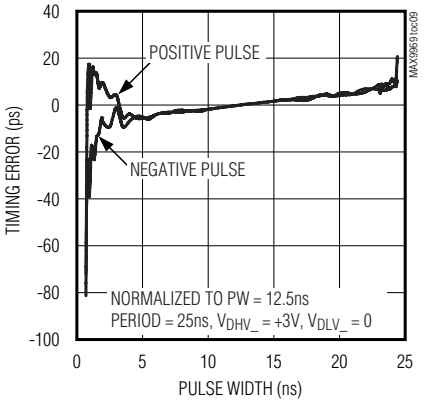
DRIVER 3V 1200Mbps SIGNAL RESPONSE



DRIVER DYNAMIC CURRENT-LIMIT RESPONSE



DRIVER 3V TRAILING-EDGE TIMING ERROR vs. PULSE WIDTH

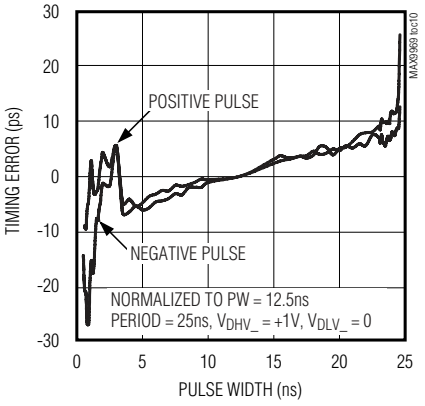


Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

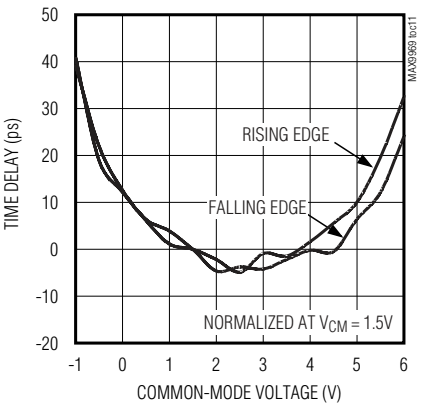
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

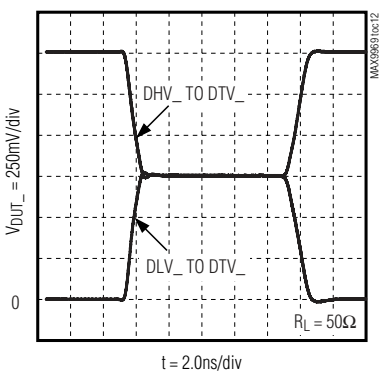
DRIVER 1V TRAILING-EDGE TIMING ERROR vs. PULSE WIDTH



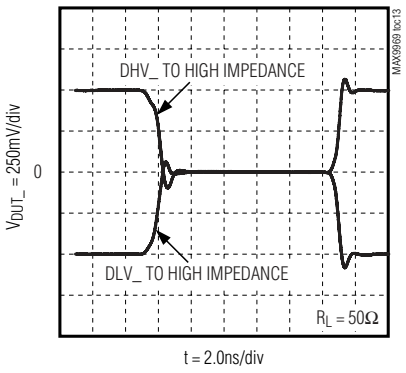
DRIVER TIME DELAY vs. COMMON-MODE VOLTAGE



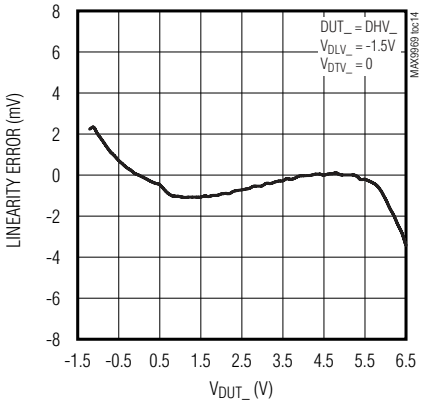
DRIVE-TO-TERM TRANSITION



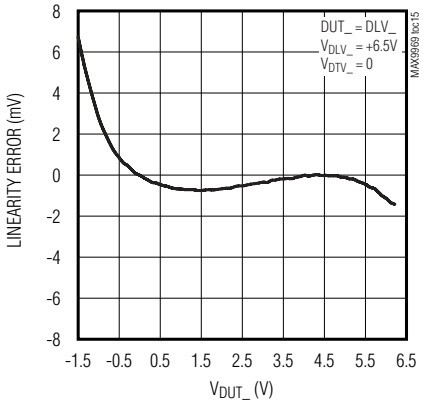
DRIVE TO HIGH-IMPEDANCE TRANSITION



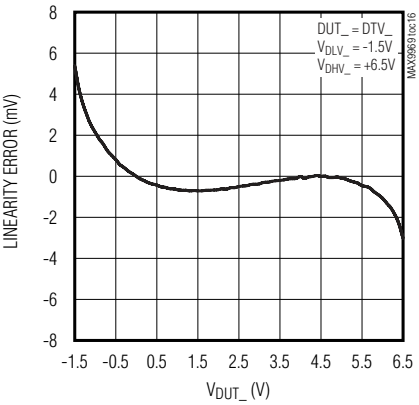
DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE



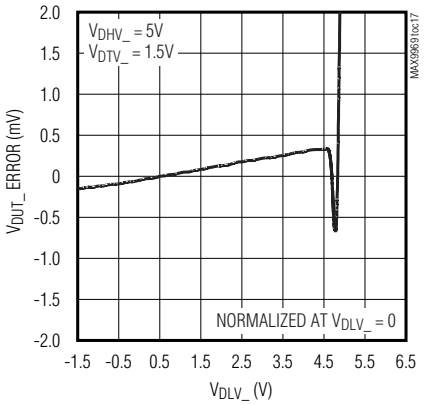
DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE



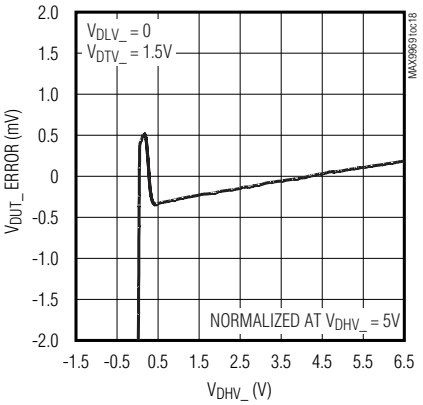
DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE



CROSSTALK TO DUT_ FROM DLV_ WITH DUT_ = DHV_



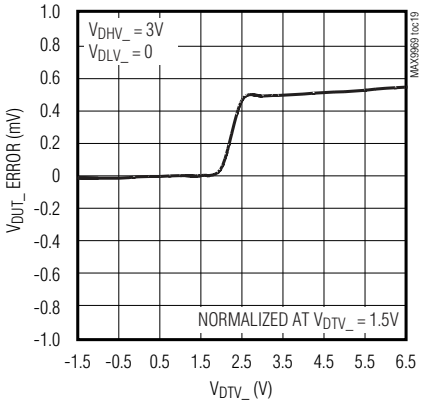
CROSSTALK TO DUT_ FROM DHV_ WITH DUT_ = DLV_



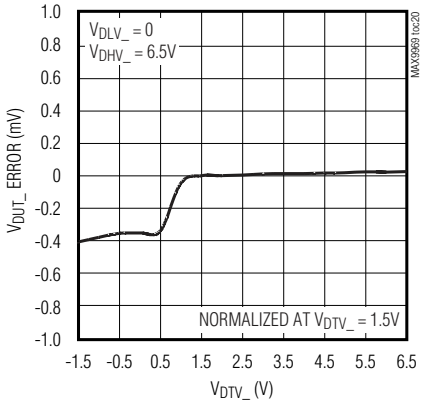
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

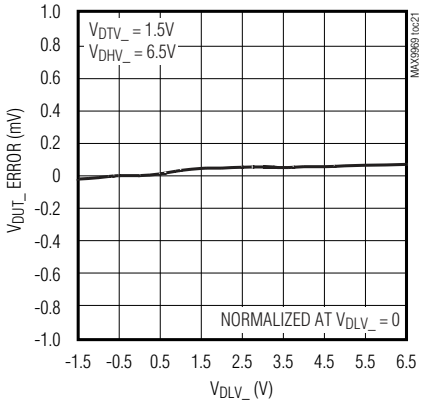
CROSSTALK TO DUT_ FROM DTV_ WITH DUT_ = DHV_



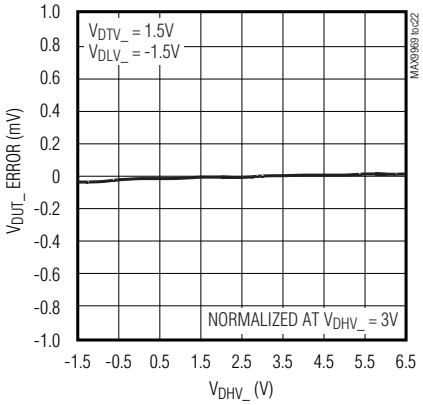
CROSSTALK TO DUT_ FROM DTV_ WITH DUT_ = DLV_



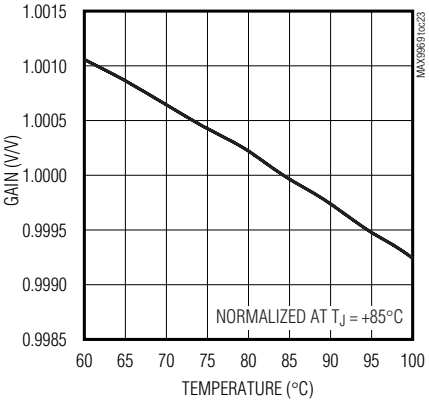
CROSSTALK TO DUT_ FROM DLV_ WITH DUT_ = DTV_



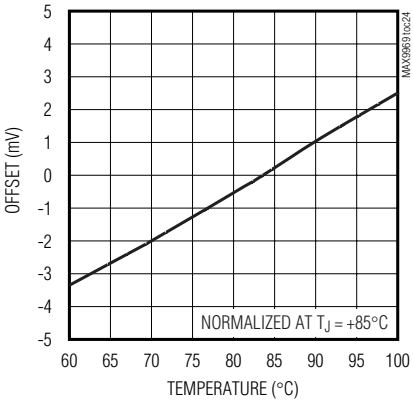
CROSSTALK TO DUT_ FROM DHV_ WITH DUT_ = DTV_



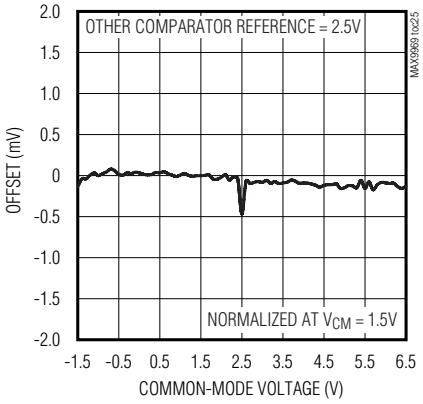
DRIVER GAIN vs. TEMPERATURE



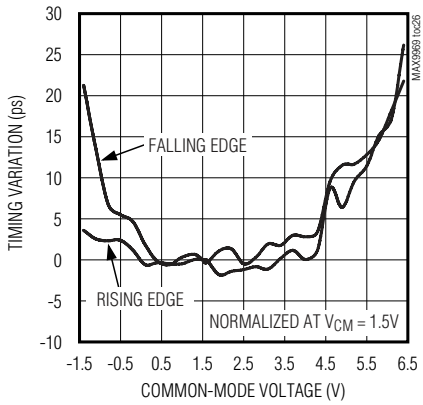
DRIVER OFFSET vs. TEMPERATURE



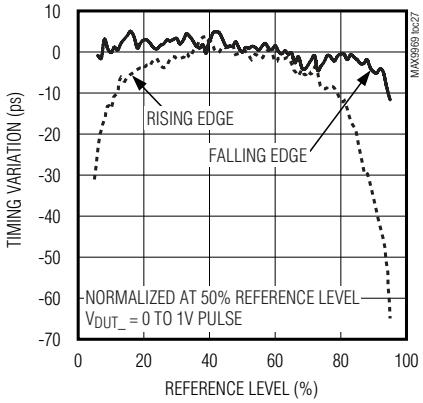
COMPARATOR OFFSET vs. COMMON-MODE VOLTAGE



COMPARATOR TIMING VARIATION vs. COMMON-MODE VOLTAGE



COMPARATOR WAVEFORM TRACKING

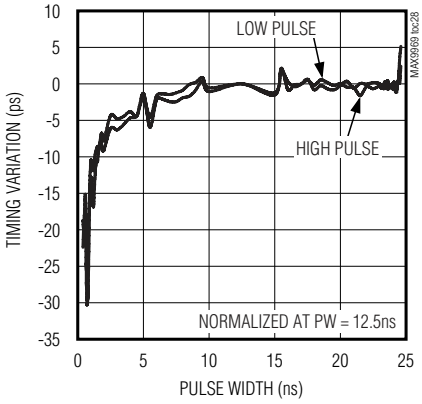


Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

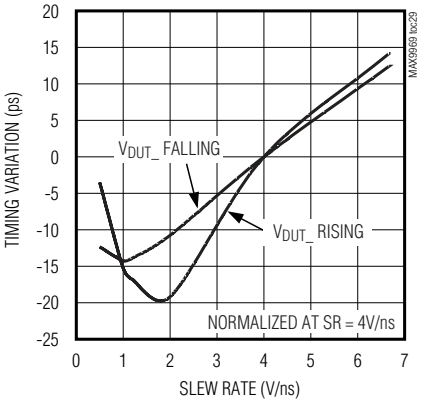
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

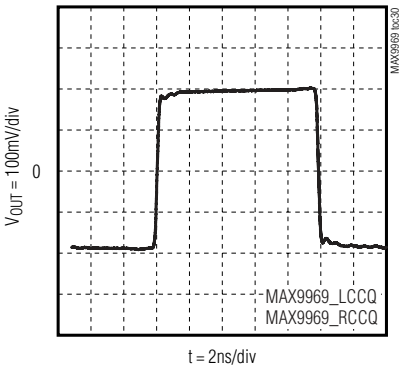
COMPARATOR TRAILING-EDGE TIMING VARIATION vs. PULSE WIDTH



COMPARATOR TIMING VARIATION vs. INPUT SLEW RATE

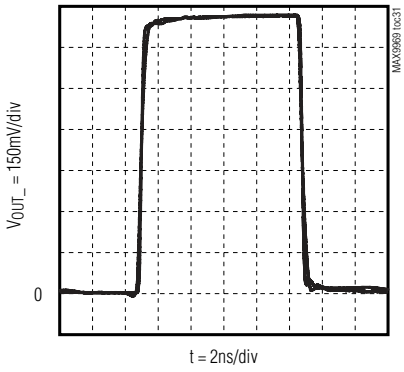


COMPARATOR DIFFERENTIAL OUTPUT RESPONSE



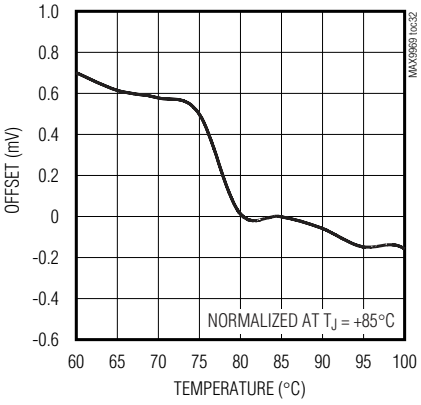
$V_{DUT\_}$ = 0 TO 3V PULSE
$V_{CHV\_} = V_{CLV\_}$ = 1.5V
EXTERNAL LOAD = 50Ω

COMPARATOR RESPONSE TO HIGH SLEW RATE OVERDRIVE

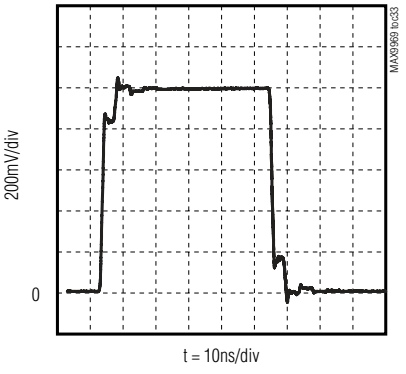


INPUT SLEW RATE = 4V/ns
HIGH IMPEDANCE

COMPARATOR OFFSET vs. TEMPERATURE

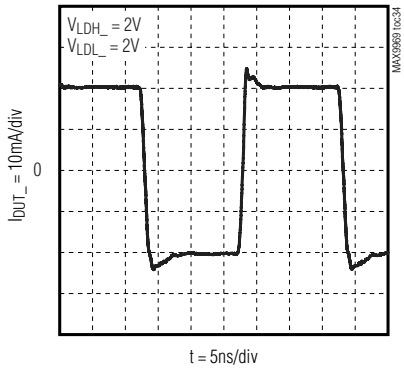


CLAMP RESPONSE AT SOURCE

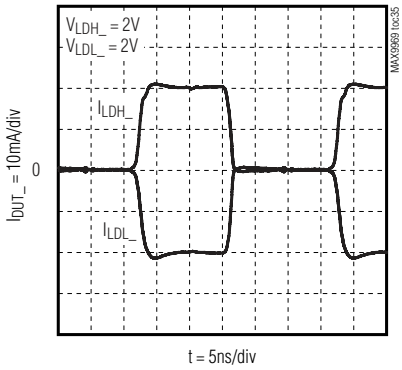


$V_{DUT\_}$ = 0 TO 1V SQUARE WAVE
R_S = 10Ω
$V_{CPLV\_}$ = -0.1V, $V_{CPHV\_}$ = +1.1V

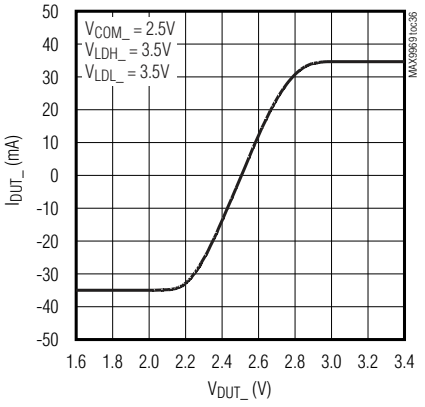
ACTIVE-LOAD COMMUTATION SIGNAL RESPONSE



ACTIVE-LOAD ENABLE SIGNAL RESPONSE



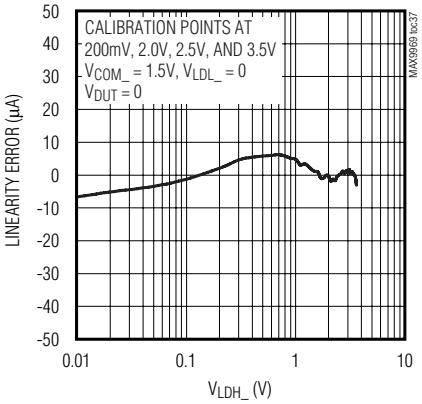
ACTIVE-LOAD CURRENT vs. LOAD VOLTAGE



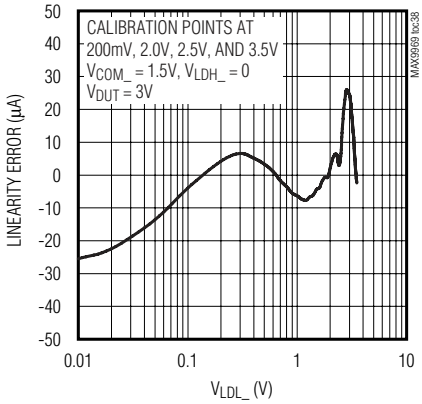
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

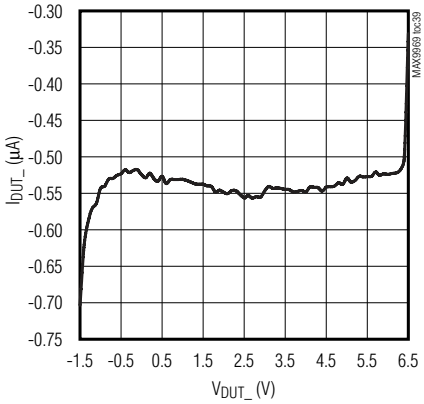
ACTIVE-LOAD LINEARITY ERROR $I_{DUT\_}$ vs. $V_{LDH\_}$



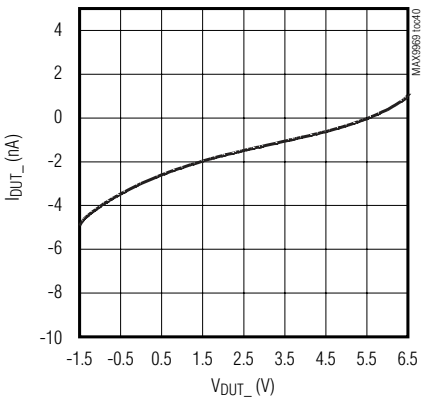
ACTIVE-LOAD LINEARITY ERROR $I_{DUT\_}$ vs. $V_{LDL\_}$



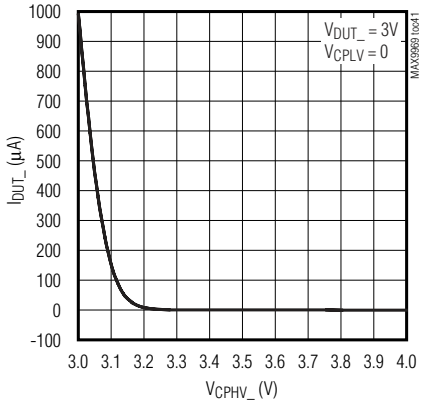
HIGH-IMPEDANCE CURRENT vs. DUT_ VOLTAGE



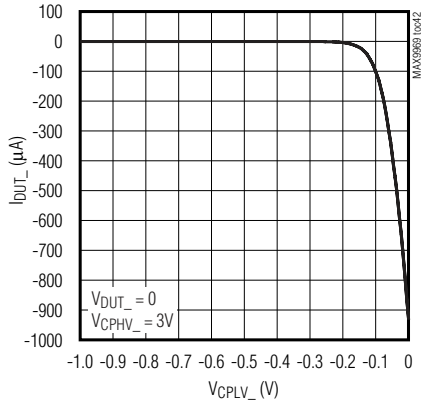
LOW-LEAKAGE CURRENT vs. DUT_ VOLTAGE



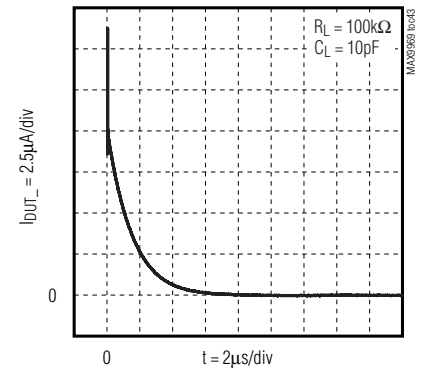
CLAMP CURRENT vs. DIFFERENCE VOLTAGE



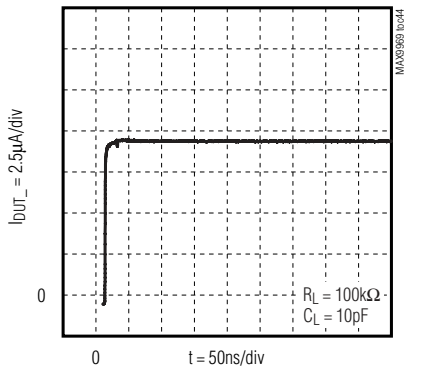
CLAMP CURRENT vs. DIFFERENCE VOLTAGE



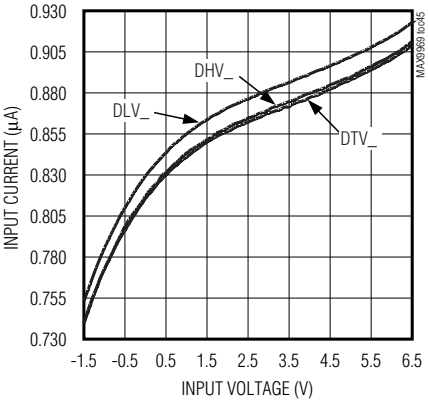
DRIVE 1V TO LOW-LEAKAGE TRANSITION



LOW-LEAKAGE TO DRIVE 1V TRANSITION



DRIVER REFERENCE CURRENT vs. DRIVER REFERENCE VOLTAGE

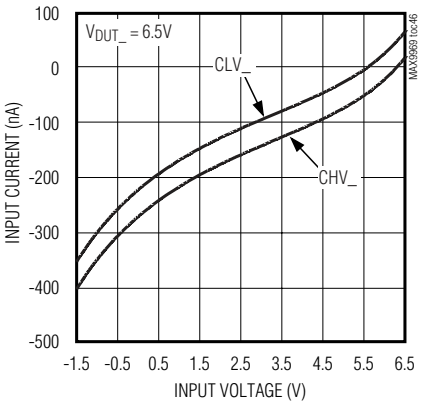


Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

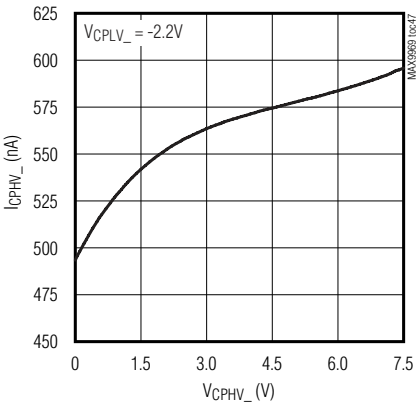
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

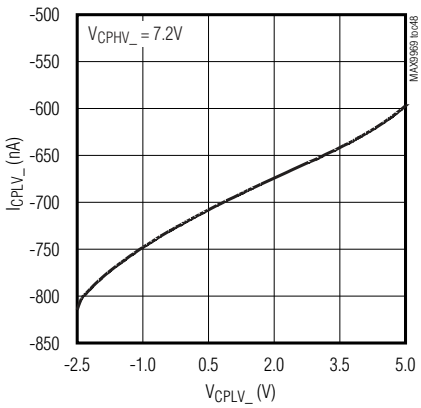
COMPARATOR REFERENCE CURRENT vs. INPUT VOLTAGE



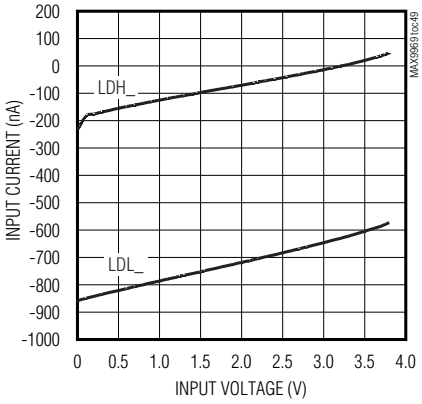
INPUT CURRENT vs. INPUT VOLTAGE, CPHV_



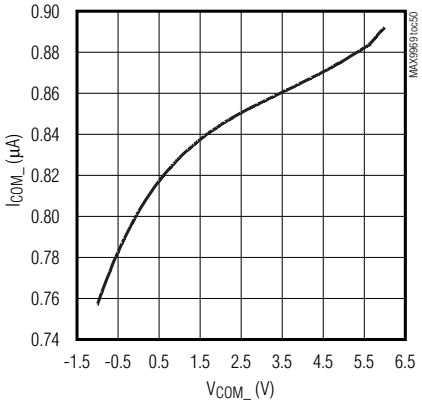
INPUT CURRENT vs. INPUT VOLTAGE, CPLV_



LOAD REFERENCE INPUT CURRENT vs. INPUT VOLTAGE



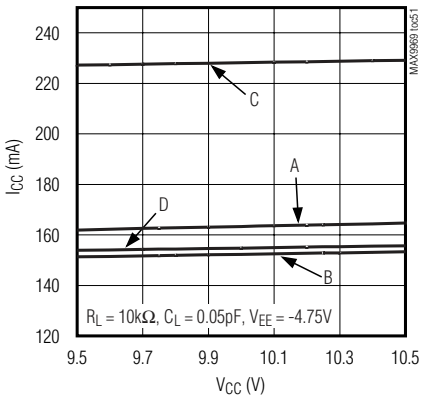
INPUT CURRENT vs. INPUT VOLTAGE, COM_



Typical Operating Characteristics (continued)

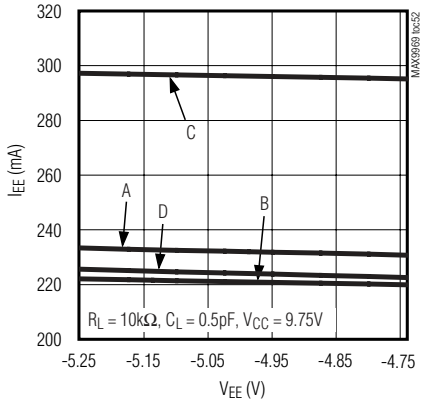
(T_A = +25°C, unless otherwise noted.)

SUPPLY CURRENT I_{CC} vs. V_{CC}



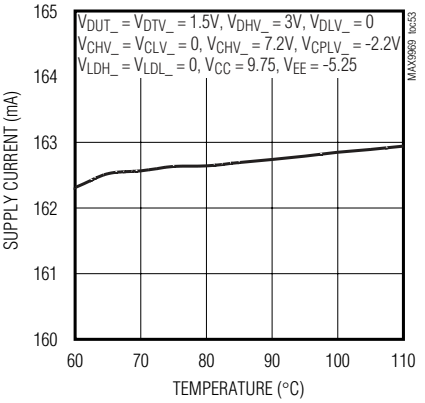
A: $V_{DUT\_} = V_{DTV\_} = 1.5V$, $V_{DHV\_} = 3V$, $V_{DLV\_} = 0$
$V_{CHV\_} = V_{CLV\_} = 0$, $V_{CPHV\_} = 7.2V$, $V_{CPLV\_} = -2.2V$
$V_{LDH\_} = V_{LDL\_} = 0$, $I_{SOURCE} = I_{SINK} = 0$
B: SAME AS A EXCEPT DRIVER DISABLED HIGH-Z AND LOAD ENABLED
C: SAME AS B EXCEPT $I_{SOURCE} = I_{SINK}$ = 35mA, $V_{COM\_}$ = 1.5V, RL = 0
D: SAME AS C EXCEPT LOW-LEAKAGE MODE ASSERTED

SUPPLY CURRENT I_{EE} vs. V_{EE}

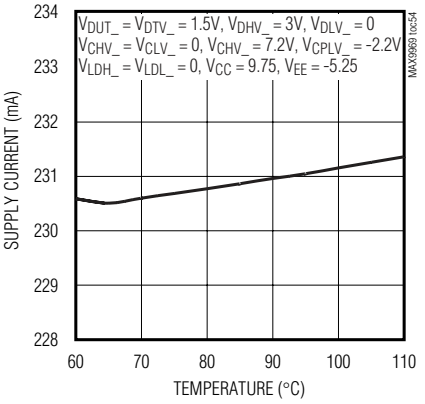


A: $V_{DUT\_} = V_{DTV\_} = 1.5V$, $V_{DHV\_} = 3V$, $V_{DLV\_} = 0$
$V_{CHV\_} = V_{CLV\_} = 0$, $V_{CPHV\_} = 7.2V$, $V_{CPLV\_} = -2.2V$
$V_{LDH\_} = V_{LDL\_} = 0$, $I_{SOURCE} = I_{SINK} = 0$
B: SAME AS A EXCEPT DRIVER DISABLED HIGH-Z AND LOAD ENABLED
C: SAME AS B EXCEPT $I_{SOURCE} = I_{SINK}$ = 35mA, $V_{COM\_}$ = -1V, $R_L = 0$
D: SAME AS C EXCEPT LOW-LEAKAGE MODE ASSERTED

I_{CC} vs. TEMPERATURE



I_{EE} vs. TEMPERATURE



Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

Pin Description

PIN	NAME	FUNCTION
1	TEMP	Temperature Monitor Output
2, 9, 12, 14, 17, 24, 35, 45, 46, 60, 80, 81, 91	V_{EE}	Negative Power-Supply Input
3, 5, 10, 16, 21, 23, 25, 34, 43, 44, 82, 83, 92	GND	Ground Connection
4, 11, 15, 22, 33, 41, 42, 66, 84, 85, 93	V_{CC}	Positive Power-Supply Input
6, 8, 18, 20, 50, 76	N.C.	No Connection. Do not connect.
7	DUT1	Channel 1 DUT Input/Output. Combined I/O for driver, comparator, clamp, and load.
13	GS	Ground Sense. GS is the ground reference for LDH_ and LDL_.
19	DUT2	Channel 2 DUT Input/Output. Combined I/O for driver, comparator, clamp, and load.
26	CLV2	Channel 2 Low-Comparator Reference Input
27	CHV2	Channel 2 High-Comparator Reference Input
28	DLV2	Channel 2 Driver-Low Reference Input
29	DTV2	Channel 2 Driver-Termination Reference Input
30	DHV2	Channel 2 Driver-High Reference Input
31	CPLV2	Channel 2 Low-Clamp Reference Input
32	CPHV2	Channel 2 High-Clamp Reference Input
36	NCH2	Channel 2 High-Comparator Output. Differential output of channel 2 high comparator.
37	CH2	
38	V_{CCO2}	Channel 2 Collector Voltage Input. Voltage input for channel 2 comparator output termination resistors. Provides pullup voltage and current for the output termination resistors. Not internally connected for versions without internal termination resistors.
39	NCL2	Channel 2 Comparator Low Output. Differential output of channel 2 low comparator.
40	CL2	
47	COM2	Channel 2 Active-Load Commutation-Voltage Reference Input

Pin Description (continued)

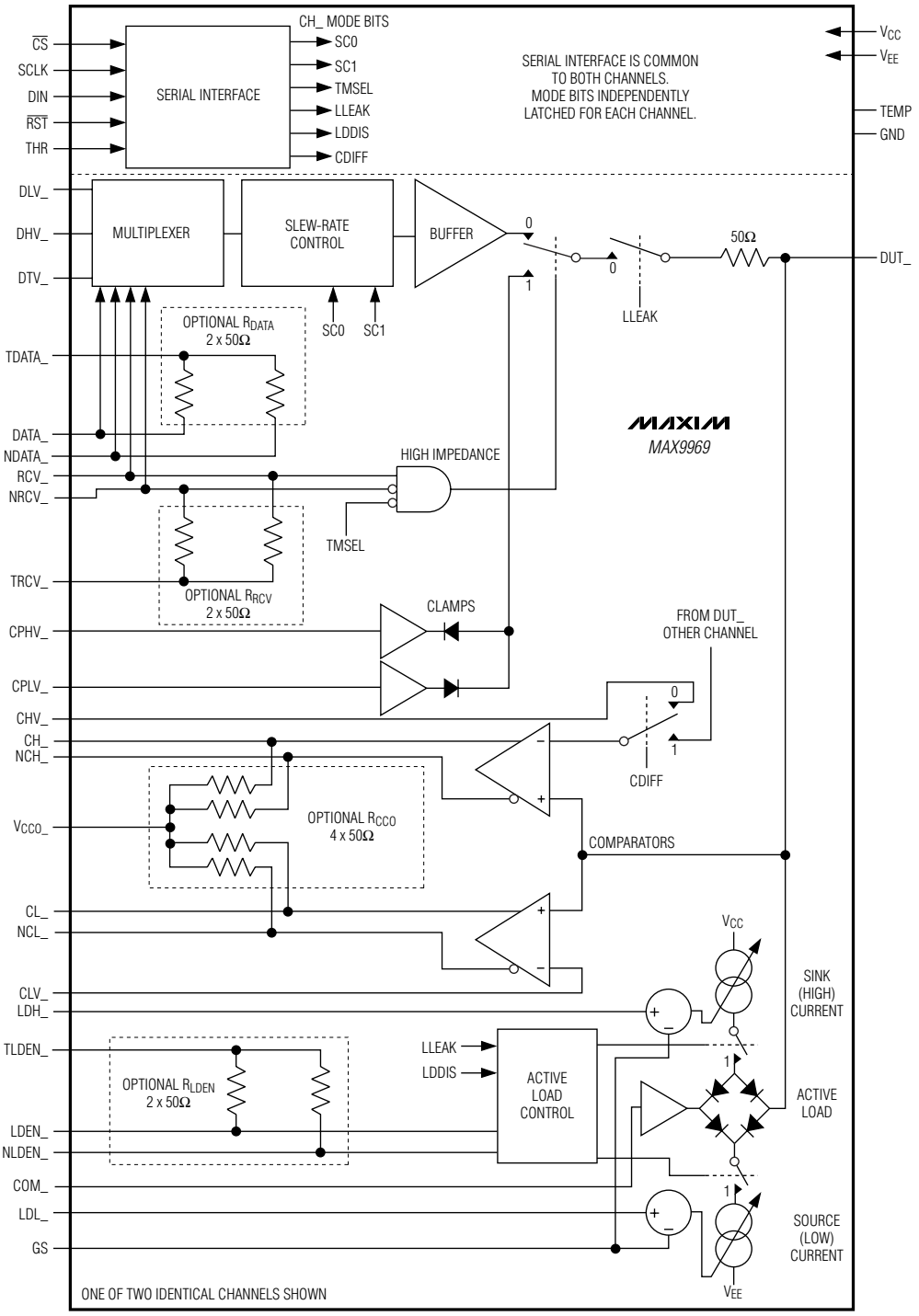
PIN	NAME	FUNCTION
48	LDL2	Channel 2 Active-Load Source-Current Reference Input
49	LDH2	Channel 2 Active-Load Sink-Current Reference Input
51	TDATA2	Channel 2 Data-Termination Voltage Input. Termination voltage input for the DATA2 and NDATA2 differential inputs. Not internally connected on versions without internal termination resistors.
52	NDATA2	Channel 2 Multiplexer Control Inputs. Differential controls DATA2 and NDATA2 select driver 2's input from DHV2 or DLV2. Drive DATA2 above NDATA2 to select DHV2. Drive NDATA2 above DATA2 to select DLV2.
53	DATA2	
54	TRCV2	Channel 2 RCV Termination Voltage Input. Termination voltage input for the RCV2 and NRCV2 differential inputs. Not internally connected on versions without internal termination resistors.
55	NRCV2	Channel 2 Multiplexer Control Inputs. Differential controls RCV2 and NRCV2 place channel 2 in receive mode. Drive RCV2 above NRCV2 to place channel 2 into receive mode. Drive NRCV2 above RCV2 to place channel 2 into drive mode.
56	RCV2	
57	TLDEN2	Channel 2 Load-Enable Termination Voltage Input. Termination voltage input for the LDEN2 and NLDEN2 differential inputs. Not internally connected on versions without internal termination resistors.
58	NLDEN2	Channel 2 Multiplexer Control Inputs. Differential controls LDEN2 and NLDEN2 enable/disable the active load. Drive LDEN2 above NLDEN2 to enable the channel 2 active load. Drive NLDEN2 above LDEN2 to disable the channel 2 active load.
59	LDEN2	
61	$\overline{RST}$	Reset Input. Asynchronous reset input for the serial register. $\overline{RST}$ is active low.
62	$\overline{CS}$	Chip-Select Input. Serial port activation input. $\overline{CS}$ is active low.
63	THR	Single-Ended Logic Threshold. Leave THR unconnected to set the threshold to +1.25V or force THR to a desired threshold voltage.
64	SCLK	Serial Clock Input. Clock for serial port.
65	DIN	Data Input. Serial port data input.
67	LDEN1	Channel 1 Multiplexer Control Inputs. Differential controls LDEN1 and NLDEN1 enable/disable the active load. Drive LDEN1 above NLDEN1 to enable the channel 1 active load. Drive NLDEN1 above LDEN1 to disable the channel 1 active load.
68	NLDEN1	
69	TLDEN1	Channel 1 Load-Enable Termination Voltage Input. Termination voltage input for the LDEN1 and NLDEN1 differential inputs. Not internally connected on versions without internal termination resistors.

Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

Pin Description (continued)

PIN	NAME	FUNCTION
70	RCV1	Channel 1 Multiplexer Control Inputs. Differential controls RCV1 and NRCV1 place channel 1 in receive mode. Drive RCV1 above NRCV1 to place channel 1 into receive mode. Drive NRCV1 above RCV1 to place channel 1 into drive mode.
71	NRCV1	
72	TRCV1	Channel 1 RCV Termination Voltage Input. Termination voltage input for the RCV1 and NRCV1 differential inputs. Not internally connected on versions without internal termination resistors.
73	DATA1	Channel 1 Multiplexer Control Inputs. Differential controls DATA1 and NDATA1 select driver 1's input from DHV1 or DLV1. Drive DATA1 above NDATA1 to select DHV1. Drive NDATA1 above DATA1 to select DLV1.
74	NDATA1	
75	TDATA1	Channel 1 Data-Termination Voltage Input. Termination voltage input for the DATA1 and NDATA1 differential inputs. Not internally connected on versions without internal termination resistors.
77	LDH1	Channel 1 Active-Load Sink-Current Reference Input
78	LDL1	Channel 1 Active-Load Source-Current Reference Input
79	COM1	Channel 1 Active-Load Commutation-Voltage Reference Input
86	CL1	Channel 1 Low-Comparator Output. Differential output of channel 1 low comparator.
87	NCL1	
88	V_{CCO1}	Channel 1 Collector Voltage Input. Voltage input for channel 1 comparator output-termination resistors. Provides pullup voltage and current for the output-termination resistors. Not internally connected for versions without internal termination resistors.
89	CH1	Channel 1 High-Comparator Output. Differential output of channel 1 high comparator.
90	NCH1	
94	CPHV1	Channel 1 High-Clamp Reference Input
95	CPLV1	Channel 1 Low-Clamp Reference Input
96	DHV1	Channel 1 Driver-High Reference Input
97	DTV1	Channel 1 Driver-Termination Reference Input
98	DLV1	Channel 1 Driver-Low Reference Input
99	CHV1	Channel 1 High-Comparator Reference Input
100	CLV1	Channel 1 Low-Comparator Reference Input

Functional Diagram



Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

Detailed Description

The MAX9969 dual, low-power, high-speed, pin electronics DCL IC includes, for each channel, a three-level pin driver, a dual comparator, variable clamps, and an active load. An additional differential comparator allows comparisons between the two channels. The driver features a -1.5V to +6.5V operating range and high-speed operation, includes high-impedance and active-termination (3rd-level drive) modes, and is highly linear even at low-voltage swings. The dual comparator provides low dispersion (timing variation) over a wide variety of input conditions, and differential outputs. The clamps provide damping of high-speed DUT waveforms when the device is configured as a high-impedance receiver. The programmable load supplies up to 35mA of source and sink current. The load facilitates contact/continuity testing, at-speed parametric test of IOH and IOL, and pullup of high-output-impedance devices. The MAX9969A features tighter matching of offset for the drivers and the comparators.

Optional internal resistors at the high-speed inputs provide compatibility with LVPECL, LVDS, and GTL interfaces. Connect the termination voltage inputs (TDATA_, TRCV_, TLDEN_) to the appropriate voltage for terminating LV_PECL, GTL, or other logic. Leave the inputs unconnected for 100Ω differential LVDS termination. In addition, flexible open-collector outputs with optional internal pullup resistors are available for the comparators. These features significantly reduce the discrete component count on the circuit board.

A 3-wire, low-voltage CMOS-compatible serial interface programs the low-leakage, load-disable, slew-rate, differential/window comparator and tri-state/terminate operational configurations of the MAX9969.

Output Driver

The driver input is a high-speed multiplexer that selects one of three voltage inputs: DHV_, DLV_, or DTV_. This switching is controlled by high-speed inputs DATA_ and RCV_ and mode-control bit TMSEL (Table 1). A slew-rate circuit controls the slew rate of the buffer input. Select to one of four possible slew rates according to Table 2. The speed of the internal multiplexer sets the 100% driver slew rate (see the Driver Large-Signal Response graph in the *Typical Operating Characteristics*).

DUT_ can be toggled at high speed between the buffer output and high-impedance mode, or it can be placed into low-leakage mode (Figure 2, Table 1). In high-impedance mode, the clamps are connected. High-speed input RCV_ and mode-control bits TMSEL and

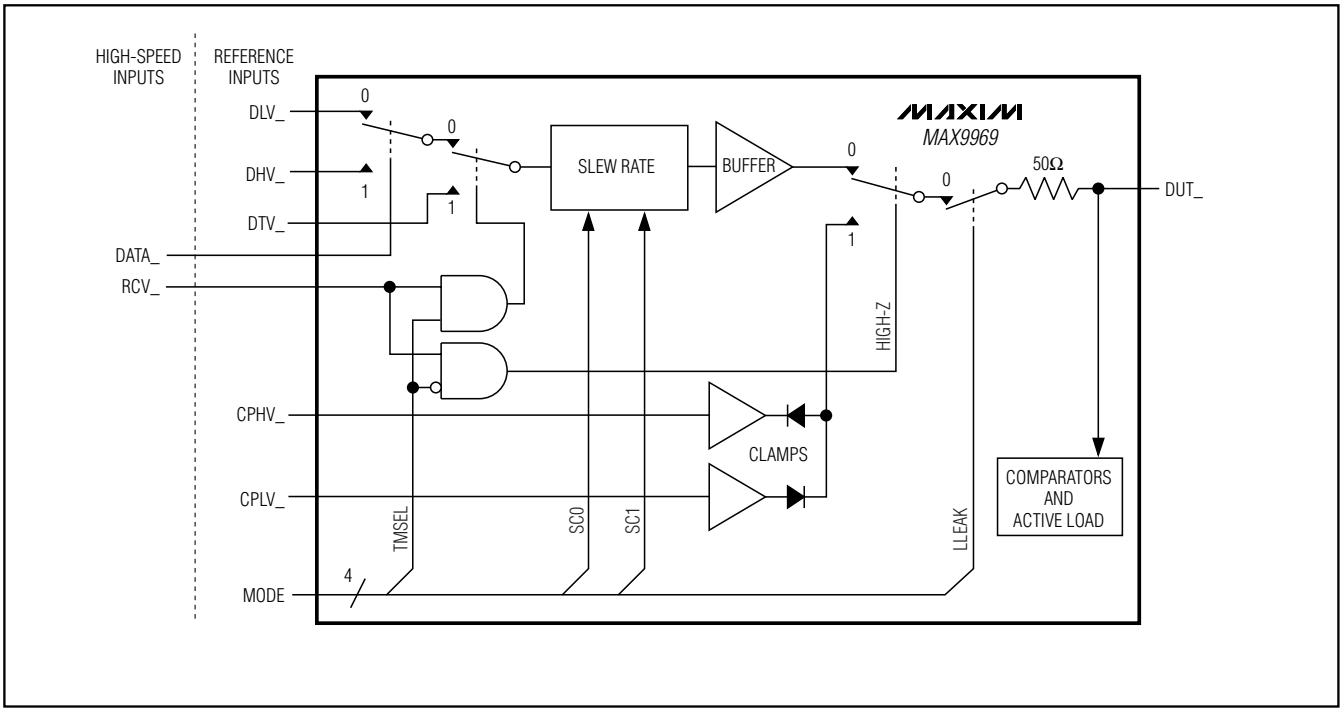


Figure 2. Simplified Driver Channel

Table 1. Driver Logic

EXTERNAL CONNECTIONS		INTERNAL CONTROL REGISTER		DRIVER OUTPUT
DATA	RCV	TMSEL	LLEAK	
1	0	X	0	Drive to DHV_
0	0	X	0	Drive to DLV_
X	1	1	0	Drive to DTV_ (term mode)
X	1	0	0	High-impedance mode (high-Z)
X	X	X	1	Low-leakage mode

Table 2. Slew-Rate Logic

SC1	SC0	DRIVER SLEW RATE (%)
0	0	100
0	1	75
1	0	50
1	1	25

LLEAK control the switching. In high-impedance mode, the bias current at DUT_ is less than 3µA over the 0 to 3V range, while the node maintains its ability to track high-speed signals. In low-leakage mode, the bias current at DUT_ is further reduced to less than 15nA, and signal tracking slows. See the *Low-Leakage Mode, LLEAK* section for more details.

The nominal driver output resistance is 50Ω. Contact the factory for different resistance values within the 45Ω to 51Ω range.

Clamps

Configure the voltage clamps (high and low) to limit the voltage at DUT_ and to suppress reflections when the channel is configured as a high-impedance receiver. The clamps behave as diodes connected to the outputs of high-current buffers. Internal circuitry compensates for the diode drop at 1mA clamp current. Set the clamp voltages using the external connections CPHV_ and CPLV_. The clamps are enabled only when the driver is in high-impedance mode (Figure 2). For transient suppression, set the clamp voltages to approximately the minimum and maximum expected DUT_ voltage range. The optimal clamp voltages are application specific and must be empirically determined. If clamping is not desired, set the clamp voltages at least 0.7V outside the expected DUT_ voltage range; overvoltage protection remains active without loading DUT_.

Table 3a. Comparator Logic, CDIFF = 0

DUT_ > CHV_	DUT_ > CLV_	CL_, NCL_	CH_, NCH_
0	0	0	0
0	1	1	0
1	0	0	1
1	1	1	1

Table 3b. Comparator Logic, CDIFF = 1

DUT1 > DUT2	DUT_ > CLV_	CL_, NCL_	CH_, NCH_
0	0	0	0
0	1	1	0
1	0	0	1
1	1	1	1

Comparators

The MAX9969 provides two independent high-speed comparators for each channel. Each comparator has one input connected internally to DUT_ and the other input connected to either CHV_ or CLV_ (see the *Functional Diagram*). Comparator outputs are a logical result of the input conditions, as indicated in Tables 3a and 3b.

The comparator differential outputs are open-collector outputs to ease interfacing with a wide variety of logic families. Versions with and without internal termination resistors switch an 8mA current source between the two outputs (Figure 3). The optional termination resistors connect the outputs to voltage input $V_{CCO\_}$. For versions without internal termination, leave $V_{CCO\_}$ unconnected and add the required external resistors. These resistors are typically 50Ω to the pullup voltage at the receiving end of the output trace. Alternate configurations can be used provided that the *Absolute Maximum Ratings* are not exceeded. For versions with internal termination, connect $V_{CCO\_}$ to the desired V_{OH} voltage. Each output provides a nominal 400mV_{P-P} swing and 50Ω source termination.

The upper comparators are configurable as differential receivers for LVDS and other differential DUT_ signals. When mode bit CDIFF is asserted, the upper comparator inputs are routed from the DUT_ outputs for both channels.

Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

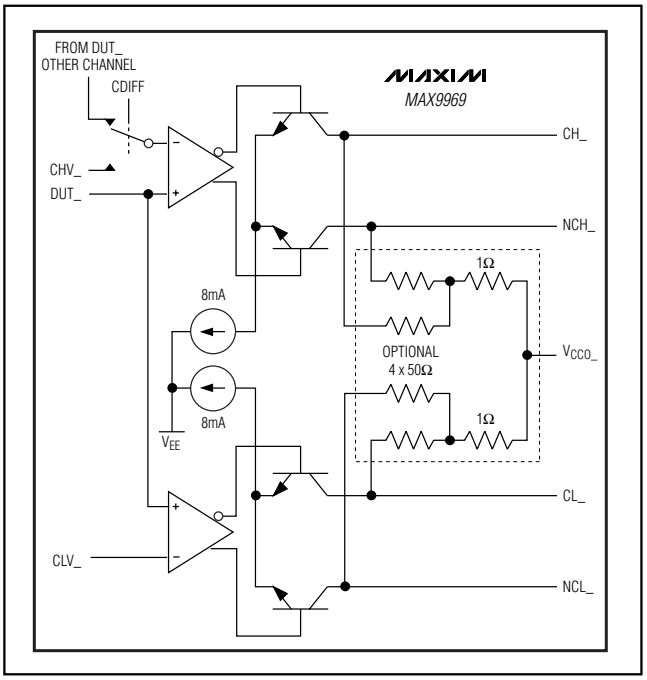


Figure 3. Open-Collector Comparator Outputs

Active Load

The active load consists of linearly programmable, class AB source and sink current sources, a commutation buffer, and a diode bridge (see the *Functional Diagram*). Analog control inputs LDH_ and LDL_ program the sink and source currents, respectively, within the 0 to 35mA range. Analog reference input COM_ sets the commutation buffer output voltage. The source and sink naming convention is referenced to the DUT. Current out of the MAX9969 constitutes sink current and current into the MAX9969 constitutes source current. The class AB loads of the MAX9969 offer substantial efficiency improvement over conventional active-load circuitry.

The programmed source (low) current loads the DUT when $V_{DUT\_} > V_{COM\_}$. The programmed sink (high) current loads the DUT when $V_{DUT\_} < V_{COM\_}$.

High-speed differential input LDEN_ and 2 bits of the control word (LDDIS and LLEAK) control the load (Table 4). When the load is enabled, the internal source and sink current sources connect to the diode bridge. When the load is disabled, the internal current sources shunt to ground and the top and bottom of the bridge float (see the *Functional Diagram*). LLEAK places the load in low-leakage mode, and overrides LDEN_. See the *Low-Leakage Mode, LLEAK* section for more detailed information.

Table 4. Active Load Programming

EXTERNAL CONNECTIONS	INTERNAL CONTROL REGISTER		MODE
LDEN_	LDDIS	LLEAK	
0	0	0	Normal operating mode, load disabled
1	0	0	Normal operating mode, load enabled
X	1	0	Load disabled
X	X	1	Low-leakage mode

LDDIS

In some tester configurations, the load enable is driven with the complement of the driver high-impedance signal (RCV_), so disabling the driver enables the load and vice versa. The LDDIS signal allows the load to be disabled independent of the state of LDEN_ (Table 4).

GS Input

The GS input allows a single level-setting DAC, such as the MAX5631 or MAX5734, to program the MAX9969's active load, driver, comparator, and clamps. Although all the DAC levels are typically offset by V_{GS}, the operation of the MAX9969's ground-sense input nullifies this offset with respect to the active-load current. Connect GS to the ground reference used by the DAC. ($V_{LDL\_}$ - V_{GS}) sets the source current by +10mA/V. ($V_{LDH\_}$ - V_{GS}) sets the sink current by -10mA/V.

To maintain an 8V range in the presence of GS variations, DHV_, DLV_, DTV_, CPHV_, CPLV_, and COM_ ranges are offset by GS. Adequate supply headroom must be maintained in the presence of GS variations. Ensure:

$$V_{CC} \geq 9.5V + Max(V_{GS})$$

$$V_{EE} \leq -4.5V + Min(V_{GS})$$

Low-Leakage Mode, LLEAK

Asserting LLEAK through the serial port or with $\overline{RST}$ places the MAX9969 into a very low-leakage state (see the *Electrical Characteristics*). With LLEAK asserted, the comparators function at a reduced speed, and the driver, clamps, and active load are disabled. This mode is convenient for making IDDQ and PMU measurements without the need for an output disconnect relay. LLEAK is programmed independently for each channel.

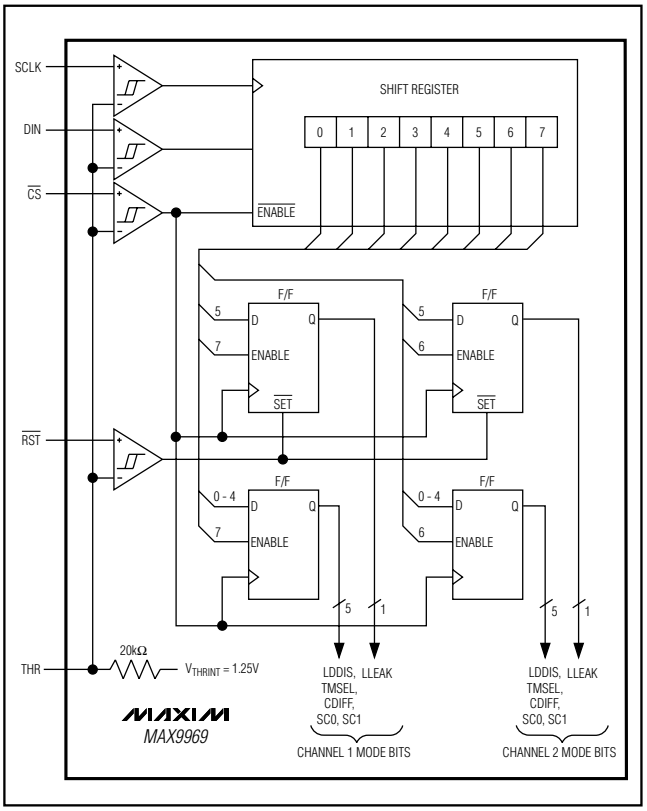


Figure 4. Serial Interface

When DUT_ is driven with a high-speed signal while LLEAK is asserted, the leakage current momentarily increases beyond the limits specified for normal operation. The low-leakage recovery specification in the *Electrical Characteristics* table indicates device behavior under this condition.

Serial Interface and Device Control

A CMOS-compatible serial interface controls the MAX9969 modes (Figure 4 and Table 5). Control data flow into an 8-bit shift register (MSB first) and are latched when $\overline{CS}$ is taken high, as shown in Figure 5. Latches contain 6 control bits for each channel of the dual pin driver. Data from the shift register are loaded to either or both of the latches as determined by bits D6 and D7. When CDIFF = 1, its effect is independent of bits D6 and D7. The control bits, in conjunction with external inputs DATA_ and RCV_, manage the features of each channel, as shown in Tables 1 and 2. $\overline{RST}$ sets LLEAK = 1 for both channels, forcing them into low-leakage mode. All other bits are unaffected. At power-up, hold $\overline{RST}$ low until V_{CC} and V_{EE} have stabilized.

Analog control input THR sets the threshold for the input logic, allowing operation with CMOS logic as low as 0.9V. Leaving THR unconnected results in a nominal threshold of 1.25V from an internal reference, providing compatibility with 2.5V to 3.3V logic.

MAX9967 Compatibility

The MAX9969 is pin compatible with the MAX9967 with minor changes.

- No PMU force/sense connection on the MAX9969
- Different common-mode ranges for control inputs
- MAX9967 comparator outputs additionally support open emitter
- Different serial interface bit structures

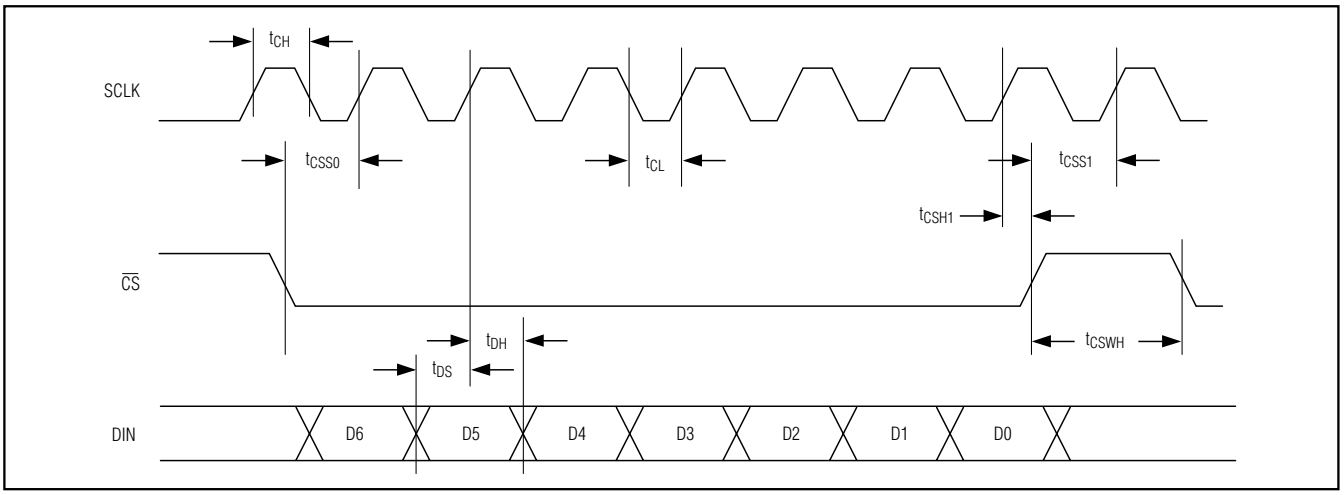


Figure 5. Serial-Interface Timing

Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

Table 5. Shift Register Functions

BIT	NAME	DESCRIPTION
D7	CH1	Channel 1 Write Enable. Set to 1 to update the control byte for channel 1. Set to 0 to make no changes to channel 1.
D6	CH2	Channel 2 Write Enable. Set to 1 to update the control byte for channel 2. Set to 0 to make no changes to channel 2.
D5	LLEAK	Low-Leakage Select. Set to 1 to put driver, load, and clamps in low-leakage mode. Comparators remain active in low-leakage mode, but at reduced speed. Set to 0 for normal operation.
D4	TMSEL	Termination Select. Driver Termination Select Bit. Set to 1 to force the driver output to the DTV_ voltage when RCV_ = 1 (term mode). Set to 0 to place the driver into high-impedance mode when RCV_ = 1 (high-Z). See Table 1.
D3	SC1	Driver Slew Rate Select. SC1 and SC0 set the driver slew rate. See Table 2.
D2	SC0	
D1	CDIFF	Differential Comparator Enable. Set to 1 to enable the differential comparators and disable the CH_ window comparators. Set to 0 to enable the CH_ window comparators and disable the differential comparators. See Tables 3a and 3b.
D0	LDDIS	Load Disable. Set LDDIS to 1 to disable the load. Set to 0 for normal operation. See Table 4.

Temperature Monitor

The MAX9969 supplies a temperature output signal, TEMP, that asserts a 3.33V nominal output voltage at a +70°C (343K) die temperature. The output voltage changes proportionally with temperature at 10mV/°C.

Heat Removal

Under normal circumstances, the MAX9969 requires heat removal through the exposed pad by use of an external heat sink. The exposed pad is electrically at V_{EE} potential, and must be either connected to V_{EE} or isolated.

Power dissipation is highly dependent upon the application. The *Electrical Characteristics* table indicates power dissipation under the condition that the source and sink currents are programmed to 0mA. Maximum dissipation occurs when the source and sink currents are both at 35mA, the $V_{DUT\_}$ is at an extreme of the voltage range (-1.5V or +6.5V), and the diode bridge is fully commutated. Under these conditions, the additional power dissipated (per channel) is:

If DUT_ is sourcing current:

$$P_D = (V_{DUT\_} - V_{EE}) \times I_{SOURCE}$$

If DUT_ is sinking current:

$$P_D = (V_{CC} - V_{DUT\_}) \times I_{SINK}$$

DUT_ sources the programmed (low) current when $V_{DUT\_} > V_{COM\_}$. The path of the current is from DUT_ through the outside of the diode bridge and the source (low) current source to V_{EE}. The programmed sink current is greatly reduced by the class AB load architecture.

DUT_ sinks the programmed (high) current when $V_{DUT\_} < V_{COM\_}$. The path of the current is from V_{CC} through the sink (high) current source and the outside of the diode bridge to DUT_. The programmed source current is greatly reduced by the class AB architecture.

θ_{JC} of the exposed-pad package is very low, approximately 1°C/W to 2°C/W. Die temperature is thus highly dependent upon the heat removal techniques used in the application. Maximum total power dissipation occurs under the following conditions:

- V_{CC} = +10.5V
- V_{EE} = -5.25V
- I_{SOURCE} = I_{SINK} = 35mA for both channels
- Load enabled
- $V_{DUT\_}$ = -1.5V
- $V_{COM\_}$ = +0.5V

Under these extreme conditions, the total power dissipation is 3.9W typical and 4.4W maximum. If the die temperature cannot be maintained at an acceptable level under these conditions, use software clamping to limit the load output currents to lower values and/or reduce the supply voltages.

Power-Supply Considerations

Bypass all V_{CC} and V_{EE} power input pins with 0.01µF capacitors, and use bulk bypassing of at least 10µF on each supply.

Chip Information

TRANSISTOR COUNT: 5284

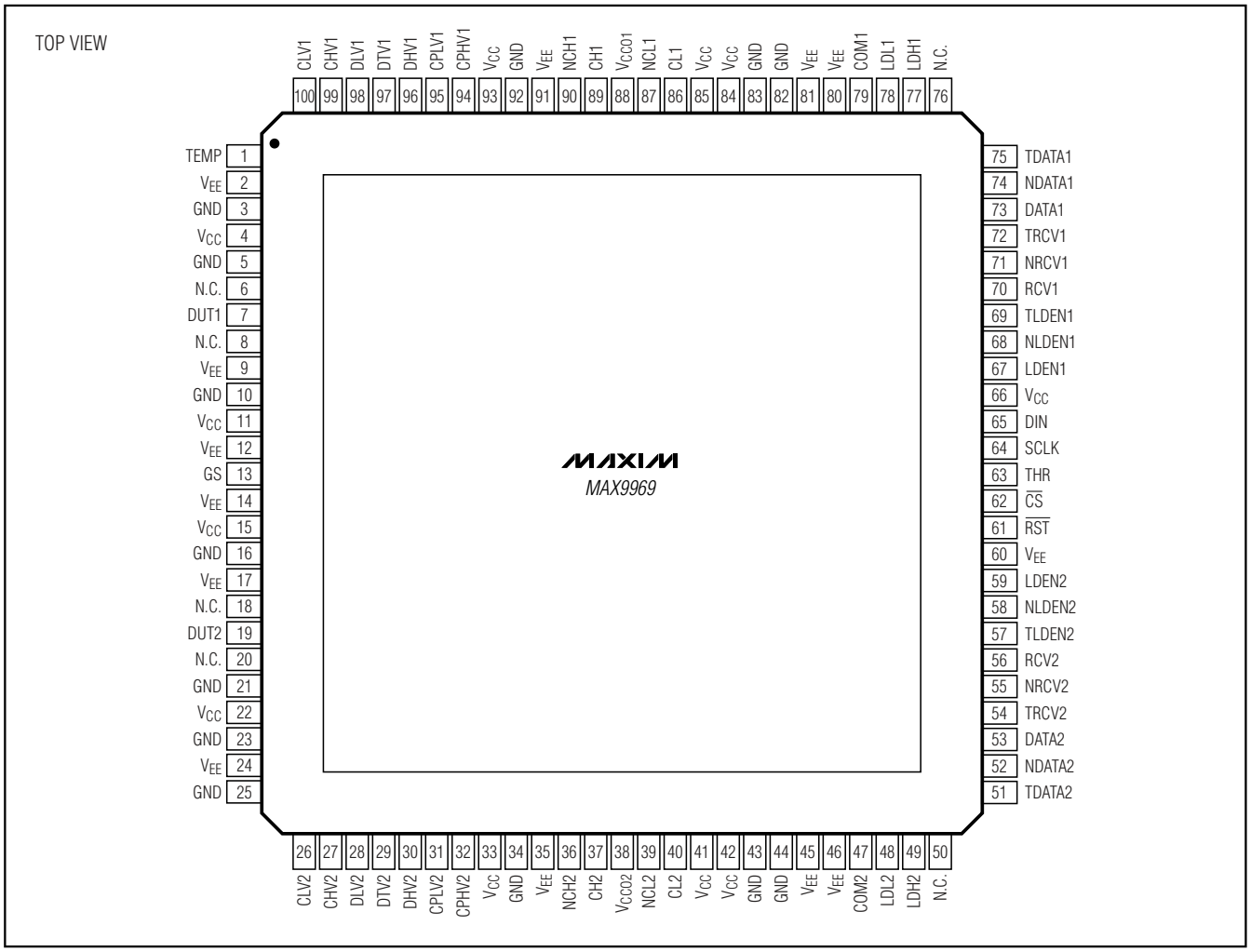
PROCESS: Bipolar

Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

Selector Guide

PART	ACCURACY GRADE	COMPARATOR OUTPUT TERMINATION	HIGH-SPEED DIGITAL INPUT TERMINATION (Ω)			HEAT EXTRACTION
			RCV_	DATA_	LDEN_	
MAX9969ADCCQ	A	None	None	None	None	Top
MAX9969AGCCQ	A	None	100	100	100	Top
MAX9969ALCCQ	A	50Ω to VCCO_	100	100	100	Top
MAX9969ARCCQ	A	50Ω to VCCO_	None	100	100	Top
MAX9969BDCCQ	B	None	None	None	None	Top
MAX9969BGCCQ	B	None	100	100	100	Top
MAX9969BLCCQ	B	50Ω to VCCO_	100	100	100	Top
MAX9969BRCCQ	B	50Ω to VCCO_	None	100	100	Top

Pin Configuration

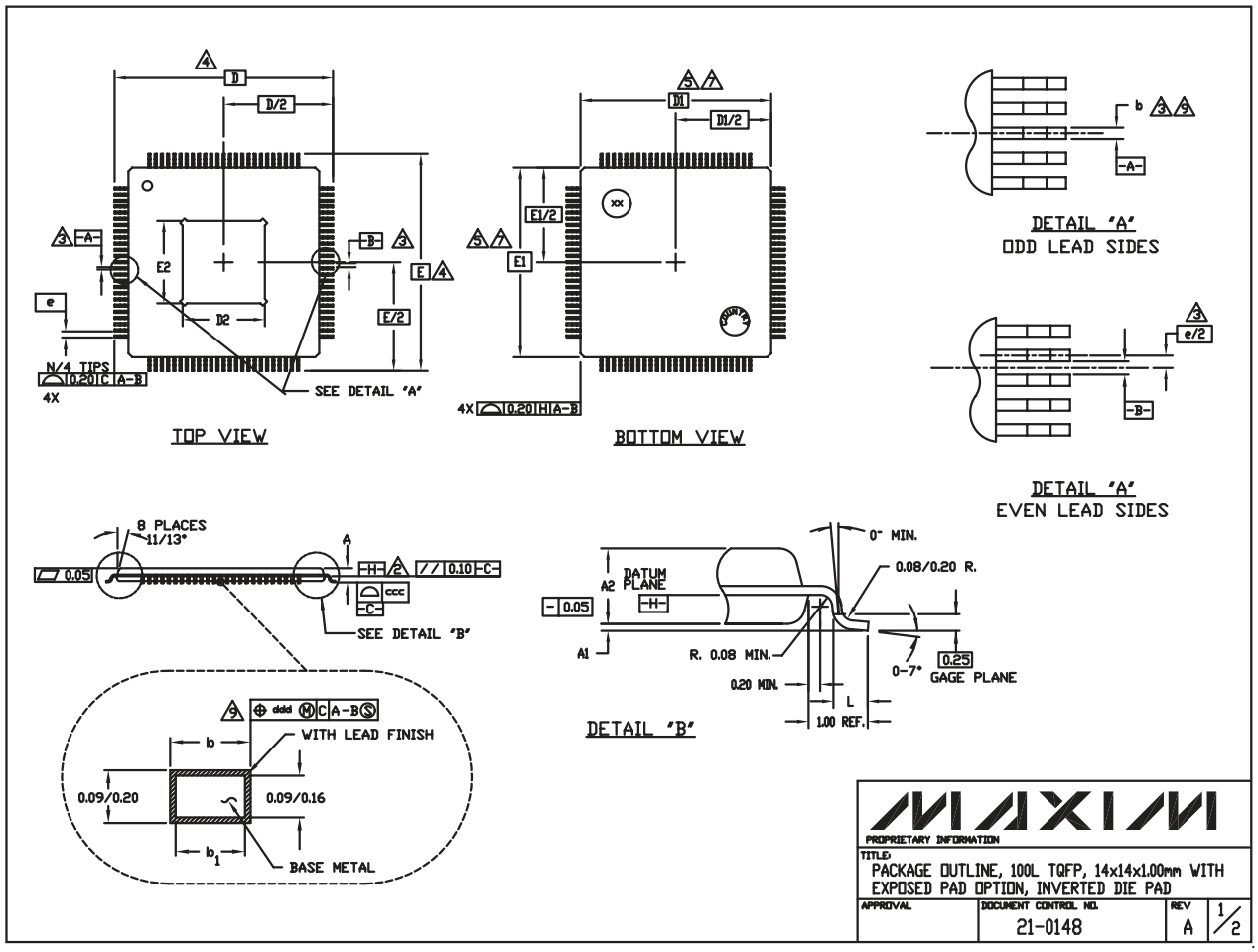


Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

TQFP 14x14.EPS



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M–1994.
2. DATUM PLANE -H- LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DATUM A-B TO BE DETERMINED AT CENTERLINE BETWEEN LEADS WHERE LEADS EXIT PLASTIC BODY AT DATUM PLANE -H- .
4. TO BE DETERMINED AT SEATING PLANE -C- .
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254mm ON D1 AND E1 DIMENSIONS.
6. "N" IS THE TOTAL NUMBER OF TERMINALS.
7. THESE DIMENSIONS TO BE DETERMINED AT DATUM PLANE -H- .
8. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15mm.
9. DIMENSIONS b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
10. CONTROLLING DIMENSION: MILLIMETER
11. MAXIMUM ALLOWABLE DIE THICKNESS TO BE ASSEMBLED IN THIS PACKAGE FAMILY IS 0.50mm.
12. THIS OUTLINE IS NOT YET JEDEC REGISTERED.
13. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
14. EXPOSED DIE PAD SHALL BE COPLANAR WITH BOTTOM OF PACKAGE WITHIN 0.05mm.
15. METAL AREA OF EXPOSED DIE PAD SHALL BE WITHIN 0.30mm OF THE NOMINAL DIE PAD SIZE.
16. COUNTRY OF ORIGIN MUST BE MARKED ON THE PACKAGE.

SYMBOL	COMMON DIMENSIONS			
	ALL DIMENSIONS ARE IN MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	—	—	1.20	
A_1	0.05	—	0.15	13
A_2	0.95	1.00	1.05	
D	16.00 BSC.			4
D_1	14.00 BSC.			7,8
E	16.00 BSC.			4
E_1	14.00 BSC.			7,8
L	0.45	0.60	0.75	
N	100			
e	0.50 BSC.			
b	0.17	0.22	0.27	9
b1	0.17	0.20	0.23	
ccc	—	—	0.08	
ddd	—	—	0.08	

EXPOSED PAD VARIATIONS						
	D2			E2		
PKG. CODE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
C100E-8R	7.70	8.00	8.30	7.70	8.00	8.30

MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 100L TQFP, 14x14x1.00mm WITH EXPOSED PAD OPTION, INVERTED DIE PAD

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0148	A	2/2