Phase-Cut Dimmable Primary-Side Regulation LED Driver Controller with Active PFC

General Description

The RT7310 is a high power factor constant current LED driver which is optimized for the compatibility with phase-cut dimmers. It supports high power factor across a wide range of line voltages, and it drives the converter in the Quasi-Resonant (QR) mode to achieve higher efficiency. By using Primary Side Regulation (PSR), RT7310 controls the output current accurately without a shunt regulator and an opto-coupler at the secondary side, reducing the external component count, the cost, and the volume of the driver board.

The RT7310 supports phase-cut dimmers, including leading-edge (TRIAC) and trailing-edge dimmers.

RT7310 embeds comprehensive protection functions for robust designs, including LED open circuit protection, LED short circuit protection, output diode short-circuit protection, VDD Under-Voltage Lockout (UVLO), VDD Over-Voltage Protection (OVP), Over-Temperature Protection (OTP), and cycle-by-cycle current limitation.

Features

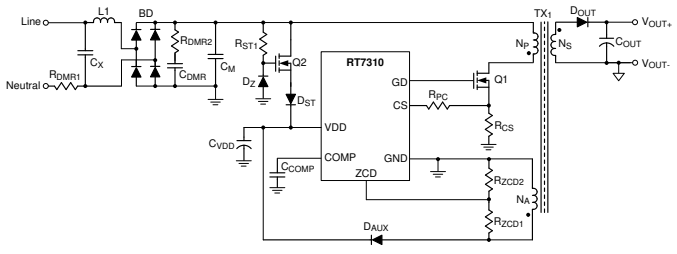
- **Supporting Phase-Cut Dimmers**
- **Tight LED Current Regulation**
- **No Opto-Coupler and TL431 Required**
- **Power Factor Correction (PFC)**
- **Quasi-Resonant**
- **Maximum/Minimum Switching Frequency Clamping**
- **Maximum/Minimum On-Time Limitation**
- **Wide VDD Range (up to 25V)**
- **Multiple Protection Features :**
  - **LED Open-Circuit Protection**
  - **LED Short-Circuit Protection**
  - **Output Diode Short-Circuit Protection**
  - **VDD Under-Voltage Lockout**
  - **VDD Over-Voltage Protection**
  - **Over-Temperature Protection**
  - **Cycle-by-Cycle Current Limitation**

Application

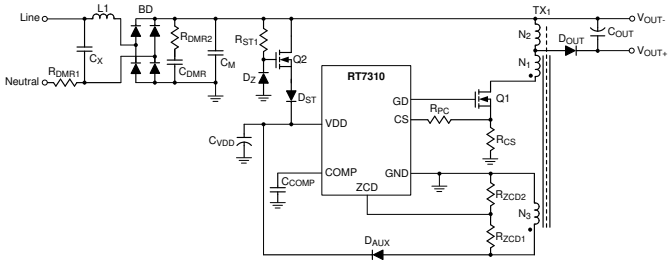
- Phase-Cut Dimmable LED luminaries

Simplified Application Circuit

Flyback Converter



Tapped-Inductor Buck-Boost Converter



Ordering Information

RT7310 □□

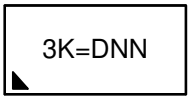
- Package Type
  E : SOT-23-6
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

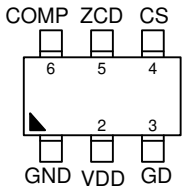
Marking Information



3K= : Product Code
DNN : Date Code

Pin Configuration

(TOP VIEW)

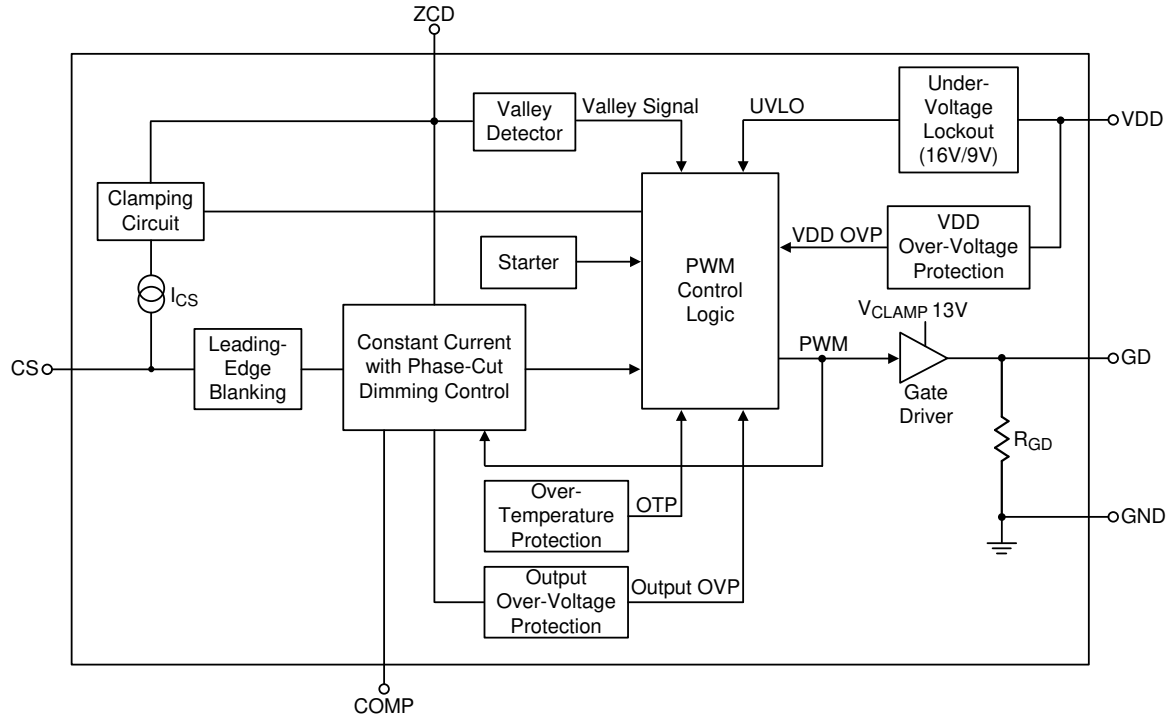


SOT-23-6

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	GND	Ground of the Controller.
2	VDD	Supply Voltage (V_{DD}) input. The controller will be enabled when V_{DD} exceeds V_{TH_ON} and disabled when V_{DD} is lower than V_{TH_OFF}.
3	GD	Gate Driver Output for External Power MOSFET.
4	CS	Current Sense Input. Connect this pin to the current sense resistor.
5	ZCD	Zero Current Detection Input. This pin is used to sense the voltage at auxiliary winding of the transformer for detecting demagnetization time of the magnetizing inductance.
6	COMP	Compensation Node. Output of the internal trans-conductance amplifier.

Function Block Diagram



Operation

Critical-Conduction Mode (CRM) with Constant On-Time Control

Figure 1 shows a typical flyback converter with input voltage (V_{IN}). When main switch Q_1 is turned on with a fixed on-time (t_{ON}), the peak current (I_{L_PK}) of the magnetic inductor (L_m) can be calculated by the following equation :

$$I_{L\_PK} = \frac{V_{IN}}{L_m} \times t_{ON}$$

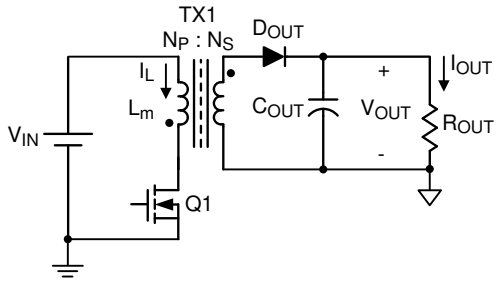


Figure 1. Typical Flyback Converter

If the input voltage is the output voltage of the full-bridge rectifier with sinusoidal input voltage ($V_{IN\_PK} \cdot \sin(\theta)$), the inductor peak current (I_{L_PK}) can be expressed as the following equation :

$$I_{L\_PK} = \frac{V_{IN\_PK} \times |\sin(\theta)| \times t_{ON}}{L_m}$$

When the converter operates in CRM with constant on-time control, the envelope of the peak inductor current will follow the input voltage waveform with in-phase. Thus, high power factor can be achieved, as shown in Figure 2.

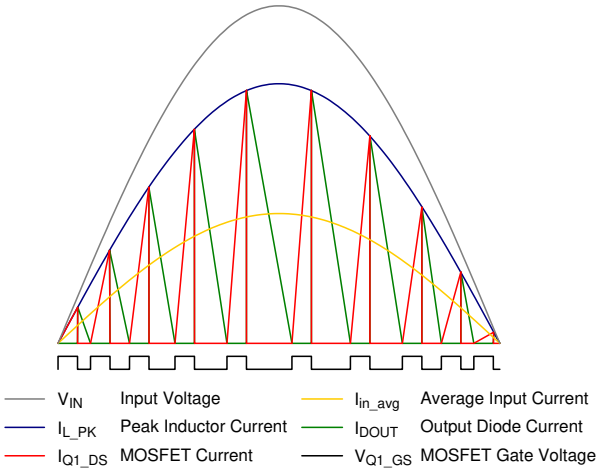


Figure 2. Inductor Current of CRM with Constant On-Time Control

Primary-Side Constant-Current Regulation

RT7310 needs no shunt regulator and opto-coupler at the secondary side to achieve the output current regulation. Figure 3 shows several key waveforms of a conventional flyback converter in Quasi-Resonant (QR) mode, in which V_{AUX} is the voltage on the auxiliary winding of the transformer.

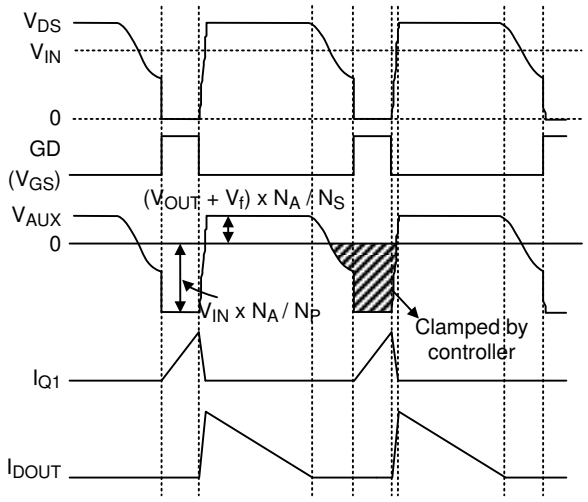


Figure 3. Key Waveforms of a Flyback Converter

Voltage Clamping Circuit

RT7310 provides a voltage clamping circuit at ZCD pin since the voltage on the auxiliary winding is negative when the main switch is turned on. The lowest voltage on ZCD pin is clamped near zero to prevent the IC from being damaged by the negative voltage. Meanwhile, the sourcing ZCD current (I_{ZCD_SH}), flowing through the upper resistor (R_{ZCD1}), is sampled and held to be a line-voltage-related signal for propagation delay compensation. RT7310 embeds the programmable propagation delay compensation through CS pin. A sourcing current I_{CS} (equal to I_{ZCD_SH} x K_{PC}) applies a voltage offset (I_{CS} x R_{PC}) which is proportional to line voltage on CS to compensate the propagation delay effect. Thus, the total power limit or output current can be equal at high and low line voltage.

Quasi-Resonant Operation

For improving converter's efficiency, RT7310 detects valleys of the Drain-to-Source voltage (V_{DS}) of main switch and turns it on near the selected valley. For the valley detections, a pulse of the "valley signal" is generated after a 500ns (typ.) delay time which starts at which the voltage (V_{ZCD}) on ZCD pin goes down and reaches the voltage threshold (V_{ZCDT}, 0.4V typ.). During the rising of the V_{ZCD}, the V_{ZCD} must reach the voltage threshold (V_{ZCDA}, 0.5V typ.). Otherwise, no pulse of the "valley signal" is generated. Moreover, if the timing when the falling V_{ZCD} reaches V_{ZCDT} is not later than a mask time (t_{MASK}, 2μs typ.) then the valley signal will be masked and regards as no valley, as shown in Figure 4.

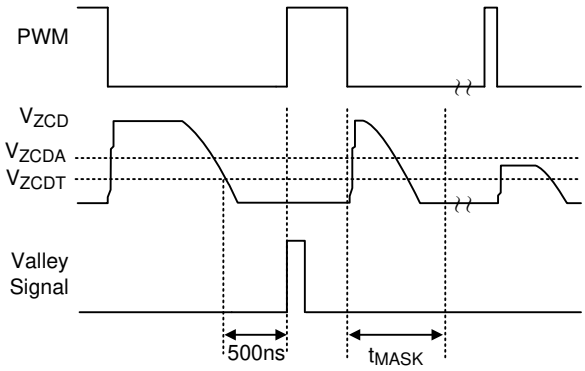


Figure 4. Valley Signal Generating Method

Figure 5 illustrates how valley signal triggers PWM. If no valley signal detected for a long time, the next PWM is triggered by a starter circuit at end of the interval (t_{START}, 75μs typ.) which starts at the rising edge of the previous PWM signal. A blanking time ($t_{S(MIN)}$, 8.5μs typ.), which starts at the rising edge of the previous PWM signal, limits minimum switching period. When the $t_{S(MIN)}$ interval is on-going, all of valley signals are not allowed to trigger the next PWM signal. After the end of the $t_{S(MIN)}$ interval, the coming valley will trigger the next PWM signal. If one or more valley signals are detected during the $t_{S(MIN)}$ interval and no valley is detected after the end of the $t_{S(MIN)}$ interval, the next PWM signal will be triggered automatically at end of the $t_{S(MIN)}$ + 5μs (typ.).

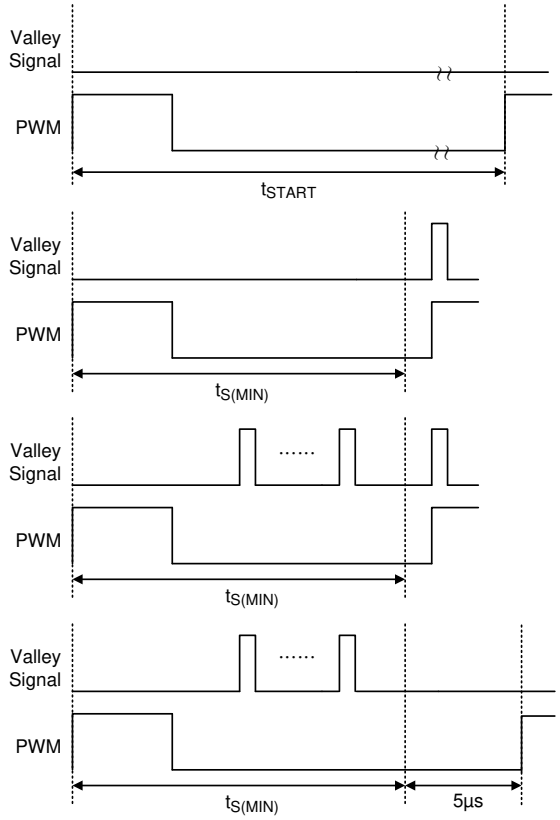


Figure 5. PWM Triggered Method

Protections

LED Open-Circuit Protection

In an event of output open circuit, the converter will be shut down to prevent being damaged. Once the LED is open-circuit, the output voltage and V_{ZCD} will rise. When the sample-and-hold ZCD voltage (V_{ZCD_SH}) exceeds its OV threshold (V_{ZCD_OVP}, 3.1V typ.), output OVP will be activated and the PWM output (GD pin) will be forced low to turn off the main switch.

LED Short-Circuit Protection

LED short-circuit protection can be achieved by cycle-by-cycle current limitation, and it will be auto-restarted when the output is recovered.

Output Diode Short-Circuit Protection

When the output diode is damaged as short-circuit, the transformer will be led to magnetic saturation and the main switch will suffer from a high current stress. To avoid the above situation, an output diode short-circuit protection is built-in. When CS voltage V_{CS} exceeds the threshold (V_{CS_SD} 1.5 typ.) of the output diode short-circuit protection, RT7310 will shut down the PWM output (GD pin) in few cycles to prevent the converter from damage.

VDD Under-Voltage Lockout (UVLO) and Over-Voltage Protection (VDD OVP)

RT7310 will be enabled when VDD voltage (V_{DD}) exceeds rising UVLO threshold (V_{TH_ON}, 16V typ.) and disabled when V_{DD} is lower than falling UVLO threshold (V_{TH_OFF}, 9V typ.).

When V_{DD} exceeds its over-voltage threshold (V_{OVP}, 27V typ.), the PWM output of RT7310 is shut down. It will be auto-restarted when the V_{DD} is recovered to a normal level.

Over-Temperature Protection (OTP)

The RT7310 provides an internal OTP function to protect the controller itself from suffering thermal stress and permanent damage. It is not suggested to use the function as precise control of over temperature. Once the junction temperature is higher than the OTP threshold (T_{SD}, 150°C typ.), the controller will shut down until the temperature cools down by 30°C (typ.).

Absolute Maximum Ratings (Note 1)

- VDD Supply Voltage, V_{DD} ---------- −0.3V to 30V
- GD to GND Voltage, V_{GD} ---------- −0.3V to 20V
- CS, ZCD, COMP to GND Voltage ---------- −0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  SOT-23-6 ---------- 0.42W
- Package Thermal Resistance (Note 2)
  SOT-23-6, θ_{JA} ---------- 235.6°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- −65°C to 150°C
- ESD Susceptibility (Note 3)
  Human Body Model ---------- 2kV
  Machine Model ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, V_{DD} ---------- 12V to 25V
- COMP Voltage, V_{COMP} ---------- 0.7V to 4.3V
- Ambient Temperature Range ---------- −40°C to 85°C
- Junction Temperature Range ---------- −40°C to 125°C

Electrical Characteristics

(V_{DD} = 15V, T_A = 25°C, unless otherwise specification)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDD Supply Current and Protections Section						
VDD OVP Threshold Voltage	V_{OVP}		25.5	27	28.5	V
VDD OVP De-bounce Time		(Note 5)	--	10	--	μs
Rising UVLO Threshold Voltage	V_{TH_ON}		15	16	17	V
Falling UVLO Threshold Voltage	V_{TH_OFF}		8	9	10	V
Operating Supply Current	I_{DD_OP}	I_{ZCD} = 0, GD open	--	--	3.5	mA
Start-up Current		V_{DD} = V_{TH_ON} – 1V	--	--	50	μA
ZCD Section						
Lower Clamp Voltage		I_{ZCD} = 0 to –2.5mA	--	0	0.3	V
ZCD OVP Threshold Voltage	V_{ZCD_OVP}	At the knee point (Note 5)	2.8	3.1	3.4	V
Constant Current Control Section						
Regulated factor for Constant-Current Control	K_{CC}		0.245	0.25	0.255	V
Maximum COMP Voltage		I_{COMP} < 30μA	4.5	--	--	V
Maximum COMP Sourcing Current	$I_{COMP(MAX)}$	V_{COMP} < 3.5V	--	62.5	--	μA

Timing Control Section						
Voltage Ramp Slope of the Ramp Generator Output	S_{ramp}		228	270	312	mV/μs
Minimum On-Time	$t_{ON(MIN)}$	I_{ZCD} = −150μA	2.2	2.7	3.2	μs
Maximum On-Time	$t_{ON(MAX)}$		--	65	--	μs
Minimum Switching Period	$t_{S(MIN)}$		7	8.5	10	μs
Duration of Starter	t_{START}	At no valley detected	--	75	--	μs
Current Sense Section						
Blanking Time	t_{LEB}	LEB + Propagation Delay (Note 5)	240	400	570	ns
Output Diode Short-Circuit Protection Voltage Threshold at CS	V_{CS_SD}		--	1.5	--	V
CS Voltage Threshold for Peak Current Limitation	V_{CS_CL}		0.93	1.03	1.13	V
Propagation Delay Compensation Factor	K_{PC}	Sourcing I_{CS} = I_{ZCD} x K_{PC}, I_{ZCD} = −150μA	--	0.02	--	A/A
Gate Driver Section						
GD Voltage Rising Time	t_R	C_L = 1nF	--	60	80	ns
GD Voltage Falling Time	t_F	C_L = 1nF	--	40	70	ns
GD Output Clamping Voltage	V_{CLAMP}	C_L = 1nF	--	13	--	V
Internal GD Pull Low Resistor	R_{GD}		--	40	--	kΩ
Over-Temperature Protection Section						
Over-Temperature Threshold	T_{SD}	(Note 5)	--	150	--	°C
Over-Temperature Threshold Hysteresis	T_{SD_HYS}	(Note 5)	--	30	--	°C

Note 1. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective two layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

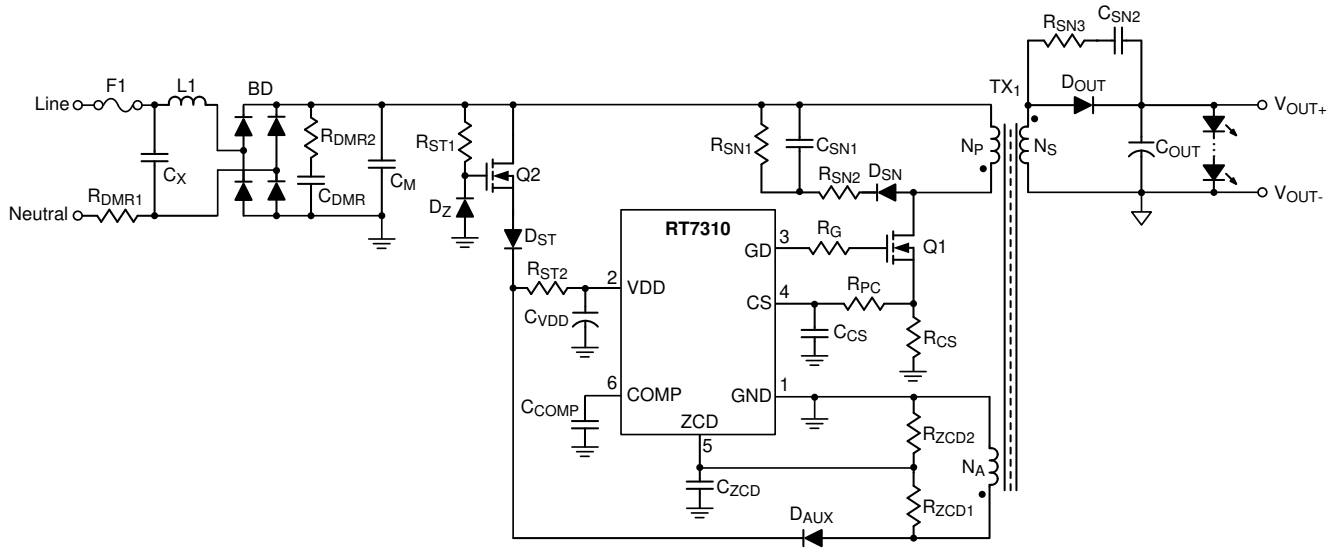
Note 3. Devices are ESD sensitive. Handling precaution recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

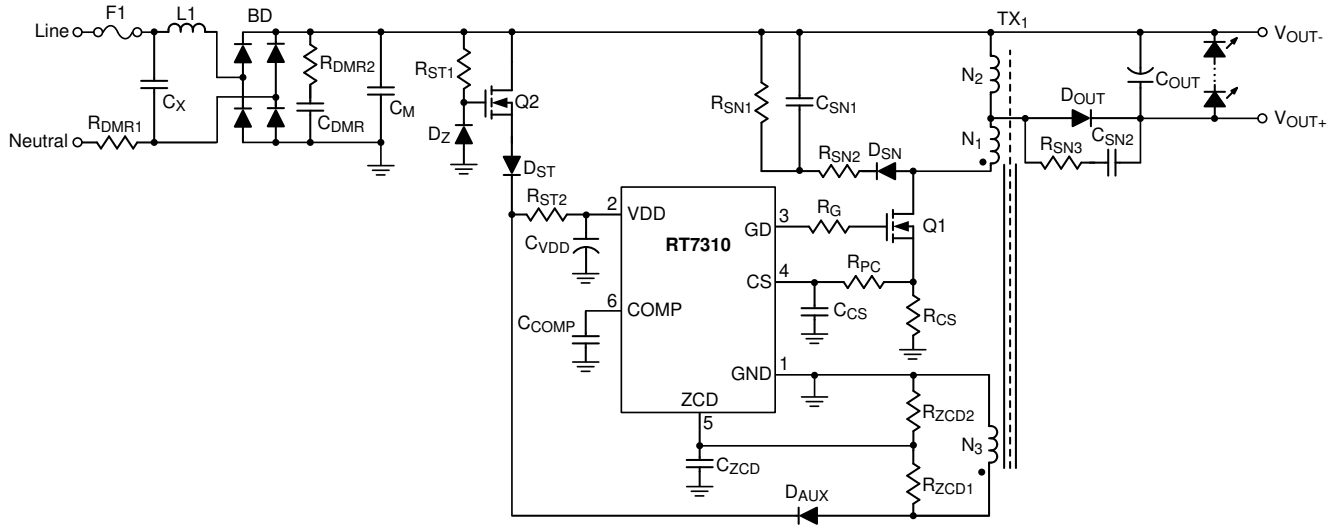
Note 5. Guaranteed by Design.

Typical Application Circuit

Flyback Application Circuit

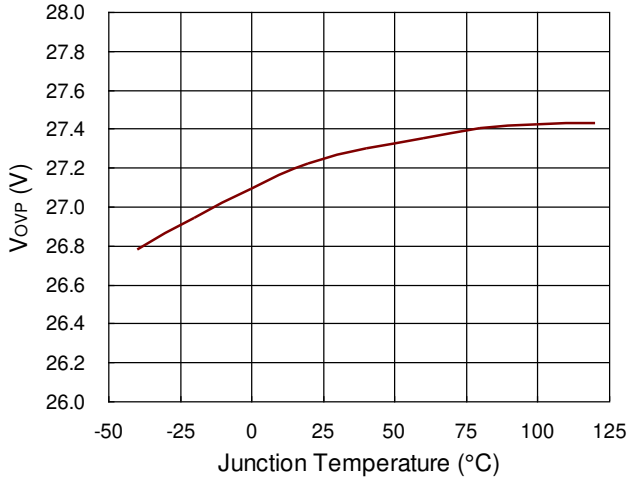


Buck-Boost Application Circuit

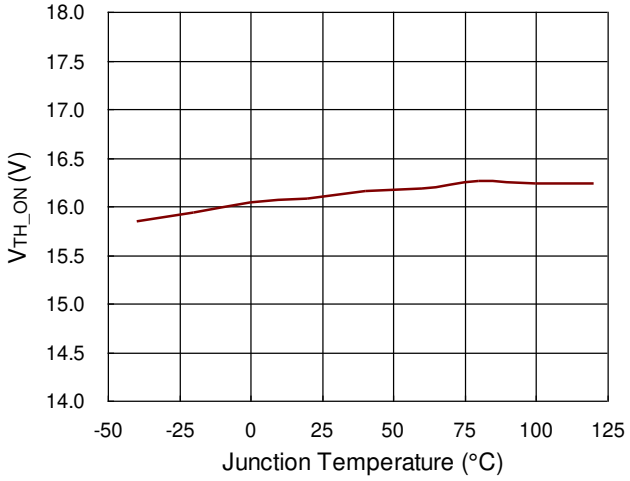


Typical Operating Characteristics

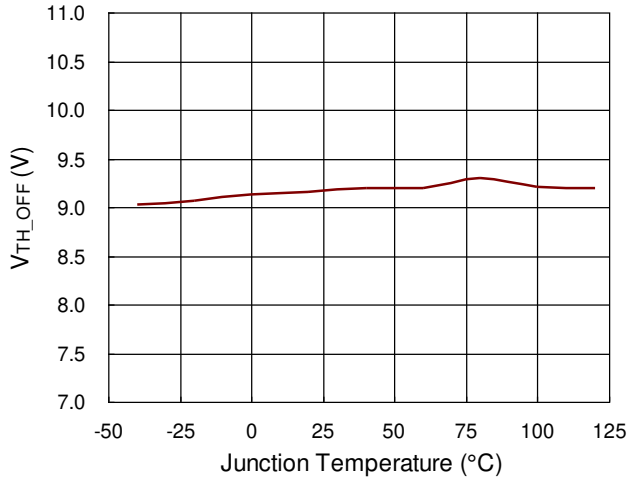
V_{OVP} vs. Junction Temperature



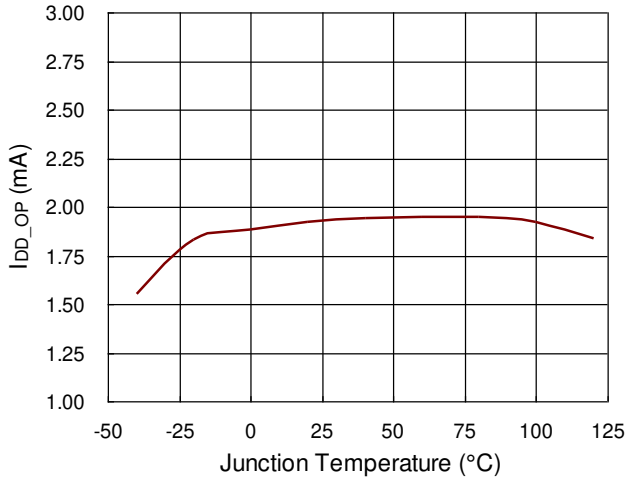
V_{TH_ON} vs. Junction Temperature



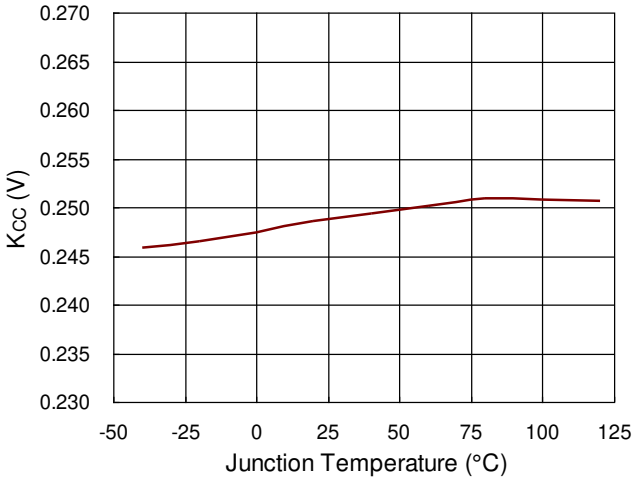
V_{TH_OFF} vs. Junction Temperature



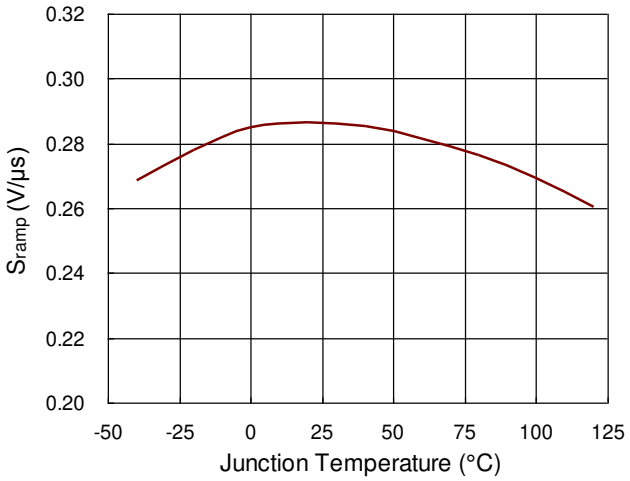
I_{DD_OP} vs. Junction Temperature



K_{CC} vs. Junction Temperature



S_{ramp} vs. Junction Temperature



Application Information

Output Current Setting

Considering the conversion efficiency, the programmed DC level of the average output current ($I_{OUT}(t)$) can be derived as:

$$I_{OUT\_CC} = \frac{1}{2} \times \frac{N_P}{N_S} \times \frac{K_{CC}}{R_{CS}} \times CTR_{TX1}$$

$$CTR_{TX1} = \frac{I_{SEC\_PK}}{I_{PRI\_PK}} \times \frac{N_S}{N_P},$$

in which CTR_{TX1} is the current transfer ratio of the transformer TX1, I_{SEC_PK} is the peak current of the secondary side, and I_{PRI_PK} is the peak current of the primary side. CTR_{TX1} can be estimated to be 0.9.

According to the above parameters, current sense resistor R_{CS} can be determined as the following equation :

$$R_{CS} = \frac{1}{2} \times \frac{N_P}{N_S} \times \frac{K_{CC}}{I_{OUT\_CC}} \times CTR_{TX1}$$

Propagation Delay Compensation Design

The V_{CS} deviation (ΔV_{CS}) caused by propagation delay effect can be derived as:

$$\Delta V_{CS} = \frac{V_{IN} \cdot t_d \cdot R_{CS}}{L_m},$$

in which t_d is the delay period which includes the propagation delay of RT7310 and the turn-off transition of the main MOSFET. The sourcing current from CS pin of RT7310 (I_{CS}) can be expressed as :

$$I_{CS} = K_{PC} \cdot V_{IN} \cdot \frac{N_A}{N_P} \cdot \frac{1}{R_{ZCD1}}$$

where N_A is the turns number of auxiliary winding.

R_{PC} can be designed by :

$$R_{PC} = \frac{\Delta V_{CS}}{I_{CS}} = \frac{t_d \cdot R_{CS} \cdot R_{ZCD1}}{L_m \cdot K_{PC}} \cdot \frac{N_P}{N_A}$$

Minimum On-Time Setting

RT7310 limits a minimum on-time ($t_{ON(MIN)}$) for each switching cycle. The $t_{ON(MIN)}$ is a function of the sample-and-hold ZCD current (I_{ZCD_SH}) as following :

$$t_{ON(MIN)} \cdot I_{ZCD\_SH} = 405p \cdot sec \cdot A \text{ (typ.)}$$

I_{ZCD_SH} can be expressed as :

$$I_{ZCD\_SH} = \frac{V_{IN} \cdot N_A}{R_{ZCD1} \cdot N_P}$$

Thus, R_{ZCD1} can be determined by:

$$R_{ZCD1} = \frac{t_{ON(MIN)} \cdot V_{IN}}{405p} \cdot \frac{N_A}{N_P} \quad (typ.)$$

In addition, the current flowing out of ZCD pin must be lower than 2.5mA (typ.). Thus, the R_{ZCD1} is also determined by:

$$R_{ZCD1} > \frac{\sqrt{2} \cdot V_{AC(MAX)}}{2.5m} \cdot \frac{N_A}{N_P}$$

where the $V_{AC(MAX)}$ is maximum input AC voltage.

Output Over-Voltage Protection Setting

Output OVP is achieved by sensing the knee voltage on the auxiliary winging. It is recommended that output OV level (V_{O_OVP}) is set at 120% of nominal output voltage (V_O). Thus, R_{ZCD1} and R_{ZCD2} can be determined by the equation as :

$$V_O \cdot \frac{N_A}{N_S} \cdot \frac{R_{ZCD2}}{R_{ZCD1} + R_{ZCD2}} \cdot 120\% = 3.1V \quad (typ.)$$

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

Where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For SOT-23-6 packages, the thermal resistance, θ_{JA}, is 235.6°C/W on a standard JEDEC 51-3 two-layer thermal test board. The maximum power

dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C − 25°C) / (235.6°C/W) = 0.42W for SOT-23-6 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 6 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

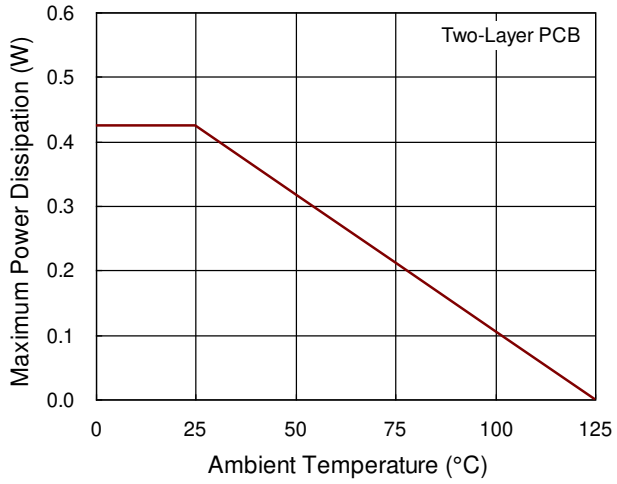


Figure 6. Derating Curve of Maximum Power Dissipation

Layout Considerations

A proper PCB layout can abate unknown noise interference and EMI issue in the switching power supply. Please refer to the guidelines when designing a PCB layout for switching power supply :

- The current path(1) from input capacitor, transformer, MOSFET, R_{CS} return to input capacitor is a high frequency current loop. The path(2) from GD pin, MOSFET, R_{CS} return to input capacitor is also a high frequency current loop. They must be as short as possible to decrease noise coupling and kept a space to other low voltage traces, such as IC control circuit paths, especially. Besides, the path(3) between MOSFET ground(b) and IC ground(d) is recommend to be as short as possible, too.
- The path(4) from RCD snubber circuit to MOSFET is a high switching loop. Keep it as small as possible.
- It is good for reducing noise, output ripple and EMI issue to separate ground traces of input capacitor(a), MOSFET(b), auxiliary winding(c) and IC control circuit(d). Finally, connect them together on input capacitor ground(a). The areas of these ground traces should be kept large.
- Placing bypass capacitor for abating noise on IC is highly recommended. The capacitors C_{COMP}, C_{ZCD}, and C_{CS} should be placed as close to controller as possible.
- To minimize parasitic trace inductance and EMI, minimize the area of the loop connecting the secondary winding, the output diode, and the output filter capacitor. In addition, apply sufficient copper area at the anode and cathode terminal of the diode for heat-sinking. It is recommended to apply a larger area at the quiet cathode terminal. A large anode area will induce high-frequency radiated EMI.

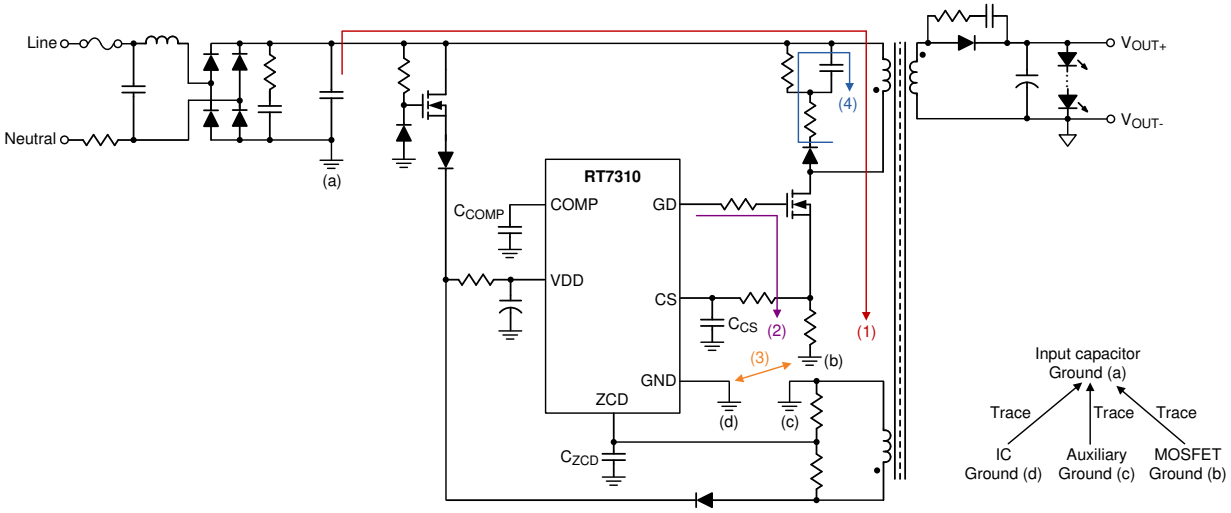
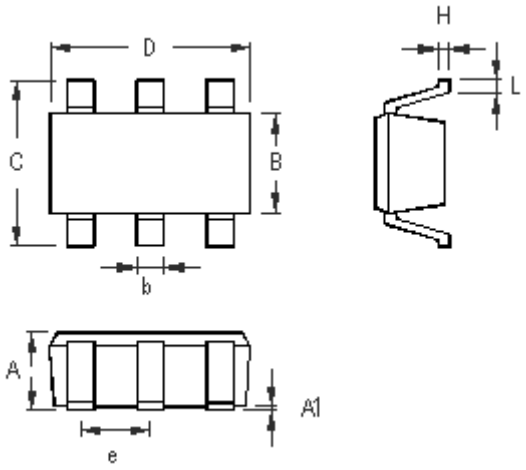


Figure 7. PCB Layout Guide

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.031	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.250	0.560	0.010	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

SOT-23-6 Surface Mount Package

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