

# HEF4521B

## 24-stage frequency divider and oscillator

Rev. 8 — 3 December 2021

Product data sheet

### 1. General description

The HEF4521B consists of a chain of 24 toggle flip-flops with an overriding asynchronous master reset input (MR), and an input circuit that allows three modes of operation. The single inverting stage (A2 to Y2) functions as: a crystal oscillator, an input buffer for an external oscillator or in combination with A1 as an RC oscillator. The crystal oscillator operates in Low-power mode when pins  $V_{SS1}$  and  $V_{DD1}$  are supplied via external resistors.

Each flip-flop divides the frequency of the previous flip-flop by two, consequently the HEF4521B counts up to  $2^{24} = 16777216$ . The counting advances on the HIGH-to-LOW transition of the clock (A2). The outputs from each of the last seven stages ( $2^{18}$  to  $2^{24}$ ) are available for additional flexibility.

It operates over a recommended  $V_{DD}$  power supply range of 3 V to 15 V referenced to  $V_{SS}$  (usually ground). Unused inputs must be connected to  $V_{DD}$ ,  $V_{SS}$ , or another input.

### 2. Features and benefits

- Wide supply voltage range from 3.0 V to 15.0 V
- CMOS low power dissipation
- High noise immunity
- Low power crystal oscillator operation
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Complies with JEDEC standard JESD 13-B
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C

### 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
HEF4521BT	-40 °C to +85 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

### 4. Functional diagram

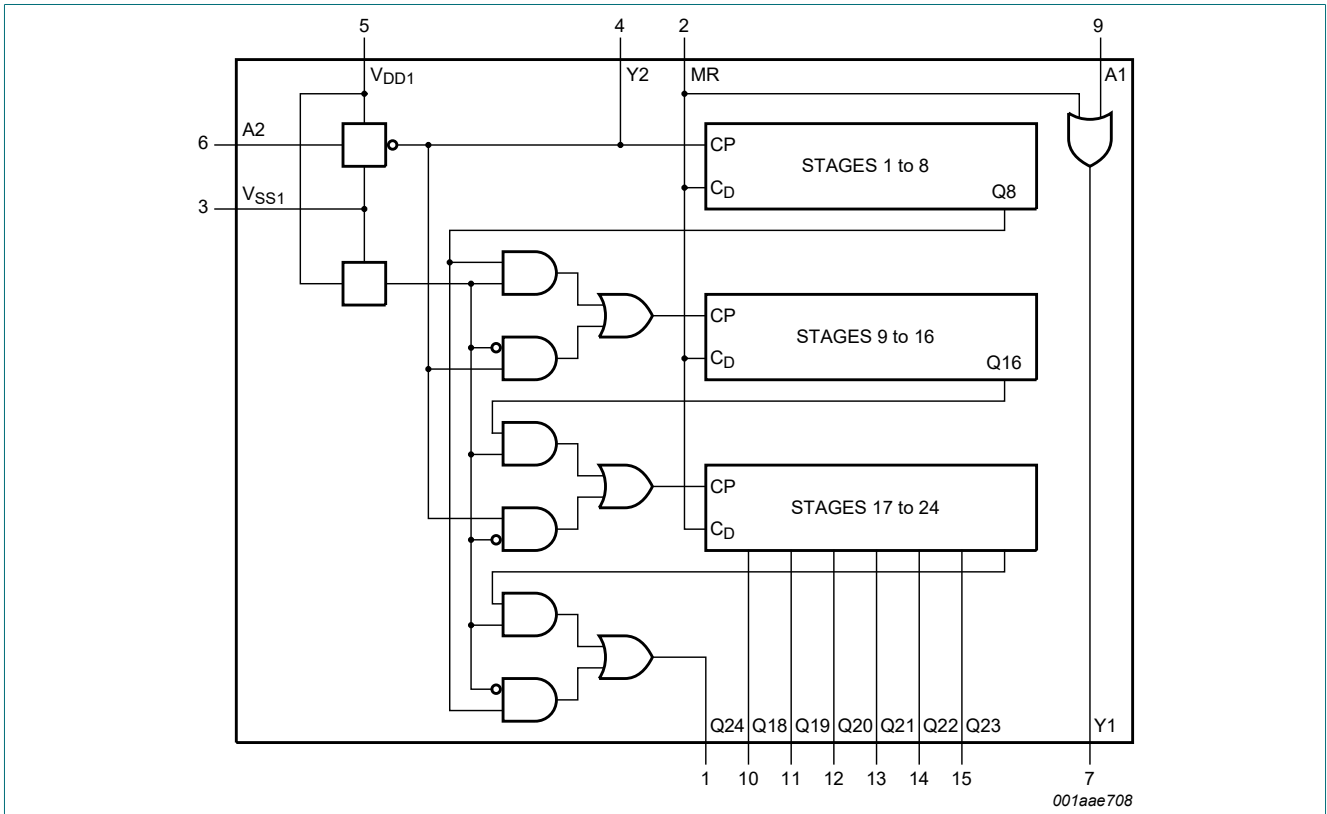


Fig. 1. Functional diagram

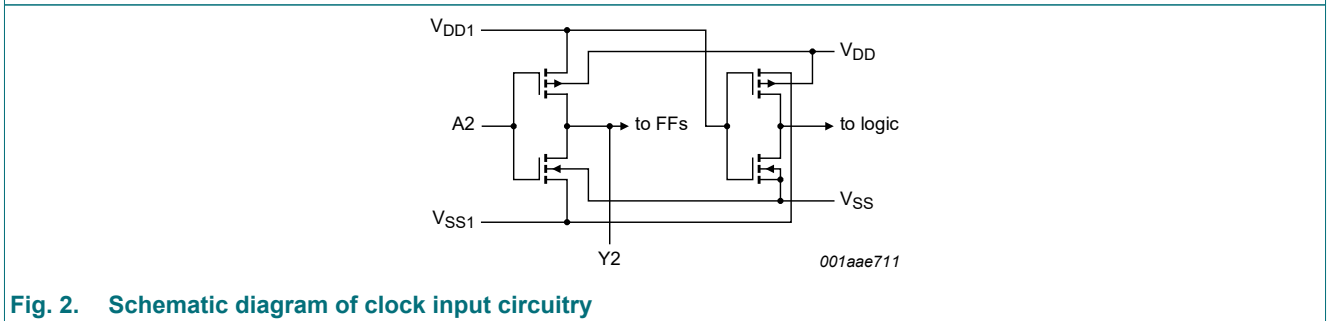


Fig. 2. Schematic diagram of clock input circuitry

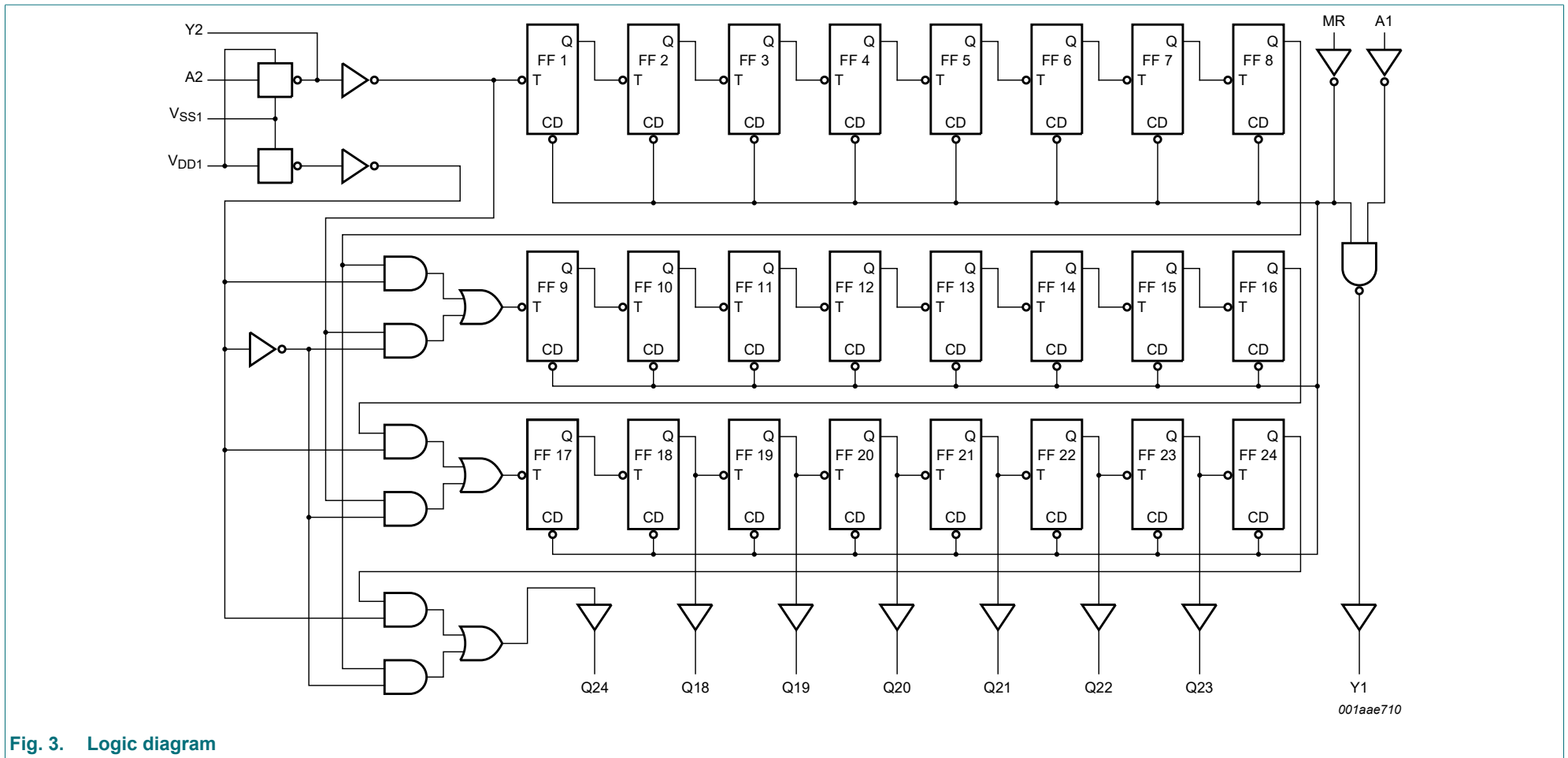
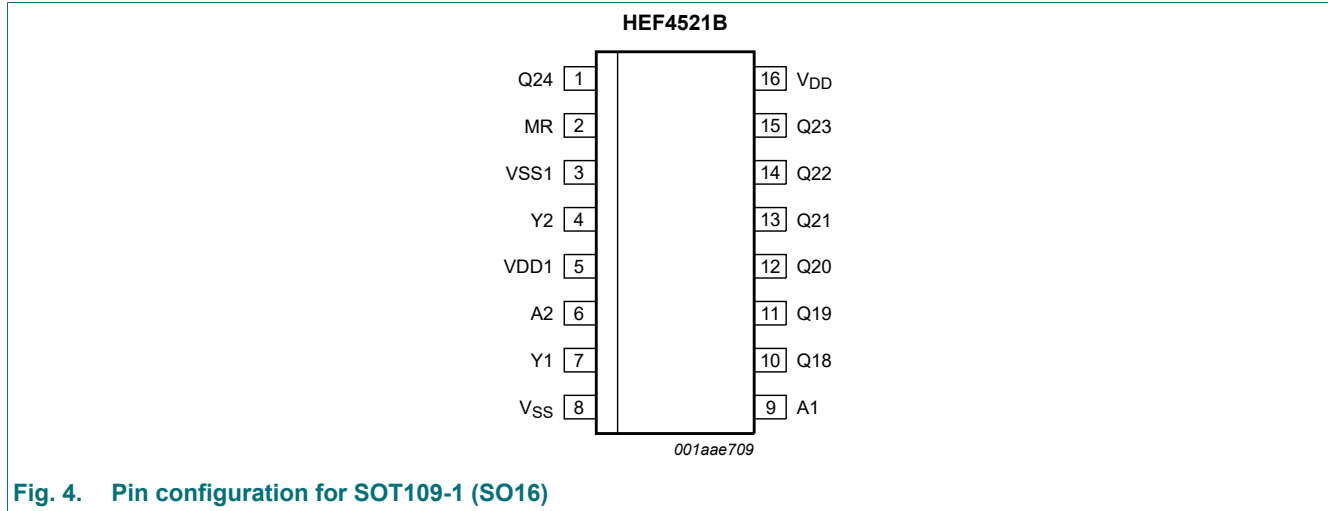


Fig. 3. Logic diagram

## 5. Pinning information

### 5.1. Pinning



### 5.2. Pin description

**Table 2. Pin description**

Symbol	Pin	Description
MR	2	master reset input
V <sub>SS1</sub>	3	ground supply voltage 1
V <sub>DD1</sub>	5	supply voltage 1
Y1, Y2	7, 4	external oscillator connection
V <sub>SS</sub>	8	ground supply voltage
A1, A2	9, 6	external oscillator connection
Q18, Q19, Q20, Q21, Q22, Q23, Q24	10, 11, 12, 13, 14, 15, 1	output
V <sub>DD</sub>	16	supply voltage

## 6. Count capacity

**Table 3. Count capacity**

Output	Count capacity
Q18	$2^{18} = 262144$
Q19	$2^{19} = 524288$
Q20	$2^{20} = 1048576$
Q21	$2^{21} = 2097152$
Q22	$2^{22} = 4194304$
Q23	$2^{23} = 8388608$
Q24	$2^{24} = 16777216$

## 7. Functional test

A test function has been included to reduce the test time required to test all 24 counter stages. This test function divides the counter into three 8-stage sections by connecting  $V_{SS1}$  to  $V_{DD}$  and  $V_{DD1}$  to  $V_{SS}$ . 255 counts are loaded into each of the 8-stage sections in parallel via A2 (connected to Y2). All flip-flops are now at a HIGH level. The counter is now returned to the normal 24-stage in series configuration by connecting  $V_{SS1}$  to  $V_{SS}$  and  $V_{DD1}$  to  $V_{DD}$ . Entering one more pulse into input A2 causes the counter to ripple from an all HIGH state to an all LOW state.

**Table 4. Functional test sequence**

H = HIGH voltage level; L = LOW voltage level; ↓ = HIGH to LOW transition.

Inputs		Control terminals			Outputs	Remarks
MR	A2	Y2	$V_{SS1}$	$V_{DD1}$	Q18 to Q24	
H	L	L	$V_{DD}$	$V_{SS}$	L	Counter is in three 8-stage sections in parallel mode; A2 and Y2 are interconnected (Y2 is now input); counter is reset by MR.
L	[1]	[1]	$V_{DD}$	$V_{SS}$	H	
L	L	L	$V_{SS}$	$V_{SS}$	H	$V_{SS1}$ is connected to $V_{SS}$ .
L	H	L	$V_{SS}$	$V_{SS}$	H	The input A2 is made HIGH.
L	H	L	$V_{SS}$	$V_{DD}$	H	$V_{DD1}$ is connected to $V_{DD}$ ; Y2 is now made floating and becomes an output; the device is now in the $2^{24}$ mode.
L	↓		$V_{SS}$	$V_{DD}$	L	Counter ripples from an all HIGH state to an all LOW state.

[1] 255 pulses are clocked into A2, Y2. The counter advances on the LOW to HIGH transition.

## 8. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD}$	supply voltage		-0.5	+18	V
$I_{IK}$	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{DD} + 0.5\text{ V}$	-	±10	mA
$V_I$	input voltage		-0.5	$V_{DD} + 0.5$	V
$I_{OK}$	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{DD} + 0.5\text{ V}$	-	±10	mA
$I_{I/O}$	input/output current		-	±10	mA
$I_{DD}$	supply current	to any supply terminal	-	±100	mA
$T_{stg}$	storage temperature		-65	+150	°C
$T_{amb}$	ambient temperature		-40	+85	°C
$P_{tot}$	total power dissipation	$T_{amb} -40\text{ °C}$ to $+85\text{ °C}$	-	500	mW
P	power dissipation	per output	-	100	mW

## 9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD}$	supply voltage		3	-	15	V
$V_I$	input voltage		0	-	$V_{DD}$	V
$T_{amb}$	ambient temperature	in free air	-40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{DD} = 5\text{ V}$	-	-	3.75	$\mu\text{s/V}$
		$V_{DD} = 10\text{ V}$	-	-	0.5	$\mu\text{s/V}$
		$V_{DD} = 15\text{ V}$	-	-	0.08	$\mu\text{s/V}$

## 10. Static characteristics

Table 7. Static characteristics

$V_{SS} = 0\text{ V}$ ;  $V_I = V_{SS}$  or  $V_{DD}$  unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	$T_{amb} = -40\text{ °C}$		$T_{amb} = +25\text{ °C}$		$T_{amb} = +85\text{ °C}$		Unit
				Min	Max	Min	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	$ I_O  < 1\ \mu\text{A}$	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
$V_{IL}$	LOW-level input voltage	$ I_O  < 1\ \mu\text{A}$	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
$V_{OH}$	HIGH-level output voltage	$ I_O  < 1\ \mu\text{A}$	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
$V_{OL}$	LOW-level output voltage	$ I_O  < 1\ \mu\text{A}$	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
$I_{OH}$	HIGH-level output current	$V_O = 2.5\text{ V}$	5 V	-	-1.7	-	-1.4	-	-1.1	mA
		$V_O = 4.6\text{ V}$	5 V	-	-0.52	-	-0.44	-	-0.36	mA
		$V_O = 9.5\text{ V}$	10 V	-	-1.3	-	-1.1	-	-0.9	mA
		$V_O = 13.5\text{ V}$	15 V	-	-3.6	-	-3.0	-	-2.4	mA
$I_{OL}$	LOW-level output current	$V_O = 0.4\text{ V}$	5 V	0.52	-	0.44	-	0.36	-	mA
		$V_O = 0.5\text{ V}$	10 V	1.3	-	1.1	-	0.9	-	mA
		$V_O = 1.5\text{ V}$	15 V	3.6	-	3.0	-	2.4	-	mA
$I_I$	input leakage current		15 V	-	$\pm 0.3$	-	$\pm 0.3$	-	$\pm 1.0$	$\mu\text{A}$
$I_{DD}$	supply current	$I_O = 0\text{ A}$	5 V	-	20	-	20	-	150	$\mu\text{A}$
			10 V	-	40	-	40	-	300	$\mu\text{A}$
			15 V	-	80	-	80	-	600	$\mu\text{A}$
$C_I$	input capacitance		-	-	-	7.5	-	-	pF	

## 11. Dynamic characteristics

**Table 8. Dynamic characteristics**

$V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ °C}$  unless otherwise specified; for test circuit see Fig. 6.

Symbol	Parameter	Conditions	V <sub>DD</sub>	Extrapolation formula[1]	Min	Typ	Max	Unit		
t <sub>PHL</sub>	HIGH to LOW propagation delay	A2 to Q18; see Fig. 5	5 V	$923\text{ ns} + (0.55\text{ ns/pF})C_L$	-	950	1900	ns		
			10 V	$339\text{ ns} + (0.23\text{ ns/pF})C_L$	-	350	700	ns		
			15 V	$212\text{ ns} + (0.16\text{ ns/pF})C_L$	-	220	440	ns		
		Qn to Qn + 1; see Fig. 5	5 V	$13\text{ ns} + (0.55\text{ ns/pF})C_L$	-	40	80	ns		
			10 V	$4\text{ ns} + (0.23\text{ ns/pF})C_L$	-	15	30	ns		
			15 V	$2\text{ ns} + (0.16\text{ ns/pF})C_L$	-	10	20	ns		
		MR to Qn	5 V	$93\text{ ns} + (0.55\text{ ns/pF})C_L$	-	120	240	ns		
			10 V	$44\text{ ns} + (0.23\text{ ns/pF})C_L$	-	55	110	ns		
			15 V	$32\text{ ns} + (0.16\text{ ns/pF})C_L$	-	40	80	ns		
		A1 to Y1; see Fig. 5	5 V	$63\text{ ns} + (0.55\text{ ns/pF})C_L$	-	90	180	ns		
			10 V	$24\text{ ns} + (0.23\text{ ns/pF})C_L$	-	35	70	ns		
			15 V	$17\text{ ns} + (0.16\text{ ns/pF})C_L$	-	25	50	ns		
t <sub>PLH</sub>	LOW to HIGH propagation delay	A2 to Q18; see Fig. 5	5 V	$923\text{ ns} + (0.55\text{ ns/pF})C_L$	-	950	1900	ns		
			10 V	$339\text{ ns} + (0.23\text{ ns/pF})C_L$	-	350	700	ns		
			15 V	$212\text{ ns} + (0.16\text{ ns/pF})C_L$	-	220	440	ns		
		Qn to Qn + 1; see Fig. 5	5 V	$13\text{ ns} + (0.55\text{ ns/pF})C_L$	-	40	80	ns		
			10 V	$4\text{ ns} + (0.23\text{ ns/pF})C_L$	-	15	30	ns		
			15 V	$2\text{ ns} + (0.16\text{ ns/pF})C_L$	-	10	20	ns		
		A1 to Y1; see Fig. 5	5 V	$33\text{ ns} + (0.55\text{ ns/pF})C_L$	-	60	120	ns		
			10 V	$19\text{ ns} + (0.23\text{ ns/pF})C_L$	-	30	60	ns		
			15 V	$12\text{ ns} + (0.16\text{ ns/pF})C_L$	-	20	40	ns		
		t <sub>t</sub>	transition time	Qn; see Fig. 5	5 V	$10\text{ ns} + (1.00\text{ ns/pF})C_L$	-	60	120	ns
					10 V	$9\text{ ns} + (0.42\text{ ns/pF})C_L$	-	30	60	ns
					15 V	$6\text{ ns} + (0.28\text{ ns/pF})C_L$	-	20	40	ns
t <sub>w</sub>	pulse width	A2 HIGH; minimum width; see Fig. 5	5 V		80	40	-	ns		
			10 V		40	20	-	ns		
			15 V		30	15	-	ns		
		MR HIGH; minimum width; see Fig. 5	5 V		70	35	-	ns		
			10 V		40	20	-	ns		
			15 V		30	15	-	ns		
t <sub>rec</sub>	recovery time	MR; see Fig. 5	5 V		+20	-10	-	ns		
			10 V		+15	-5	-	ns		
			15 V		15	0	-	ns		
f <sub>max</sub>	maximum frequency	A1; see Fig. 5	5 V		6	12	-	MHz		
			10 V		12	25	-	MHz		
			15 V		17	35	-	MHz		

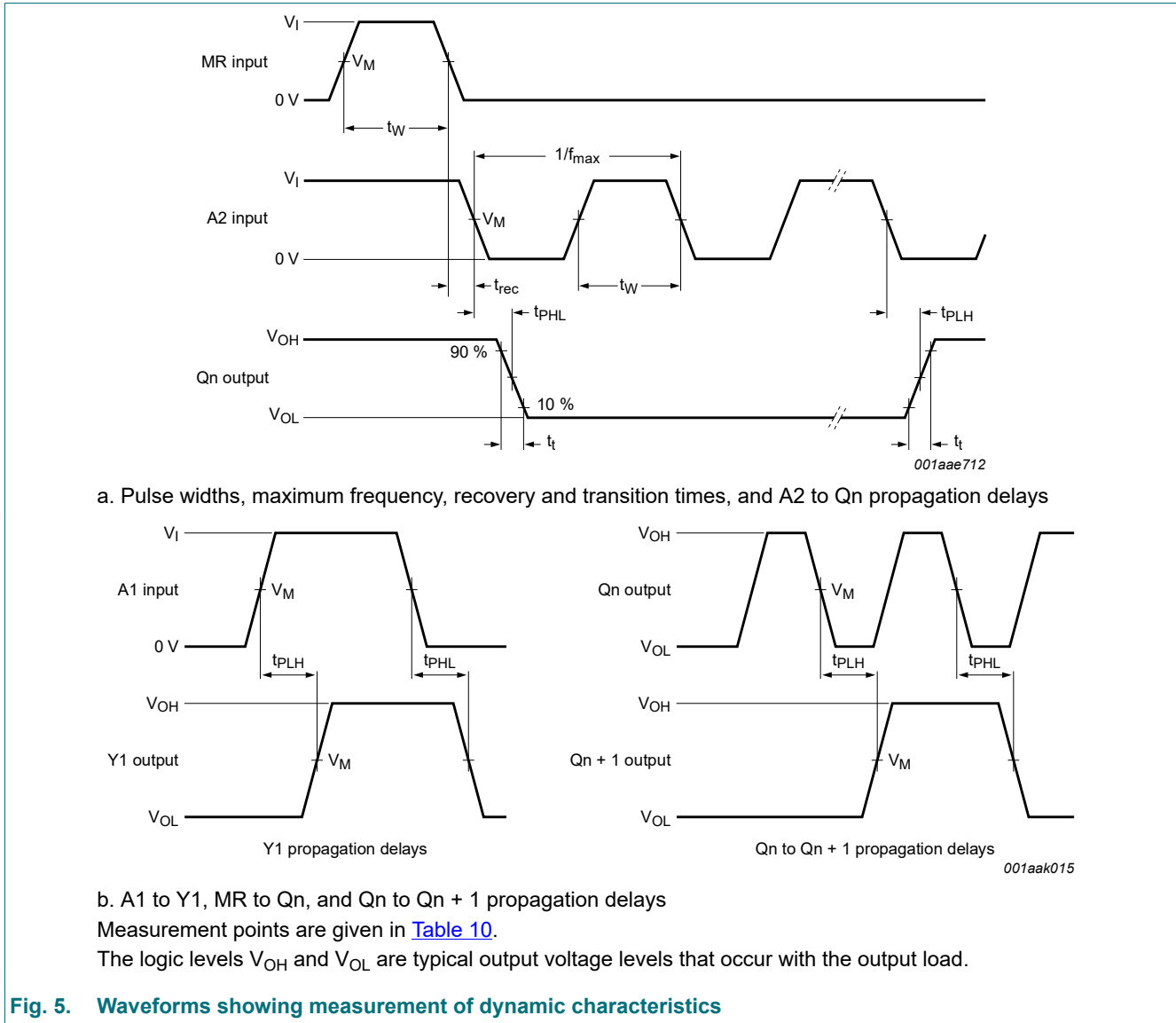
[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown ( $C_L$  in pF).

**Table 9. Dynamic power dissipation  $P_D$**

$P_D$  can be calculated from the formulas shown.  $V_{SS} = 0\text{ V}$ ;  $t_r = t_f \leq 20\text{ ns}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$ .

Symbol	Parameter	$V_{DD}$	Typical formula for $P_D$ ( $\mu\text{W}$ )	where:
$P_D$	dynamic power dissipation	5 V	$P_D = 1200 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	$f_i$ = input frequency in MHz, $f_o$ = output frequency in MHz, $C_L$ = output load capacitance in pF, $V_{DD}$ = supply voltage in V, $\Sigma(C_L \times f_o)$ = sum of the outputs.
		10 V	$P_D = 5100 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	
		15 V	$P_D = 13050 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	

**11.1. Waveforms and test circuit**



**Fig. 5. Waveforms showing measurement of dynamic characteristics**

**Table 10. Measurement points**

Supply voltage	Input	Output
$V_{DD}$	$V_M$	$V_M$
5 V to 15 V	$0.5V_{DD}$	$0.5V_{DD}$



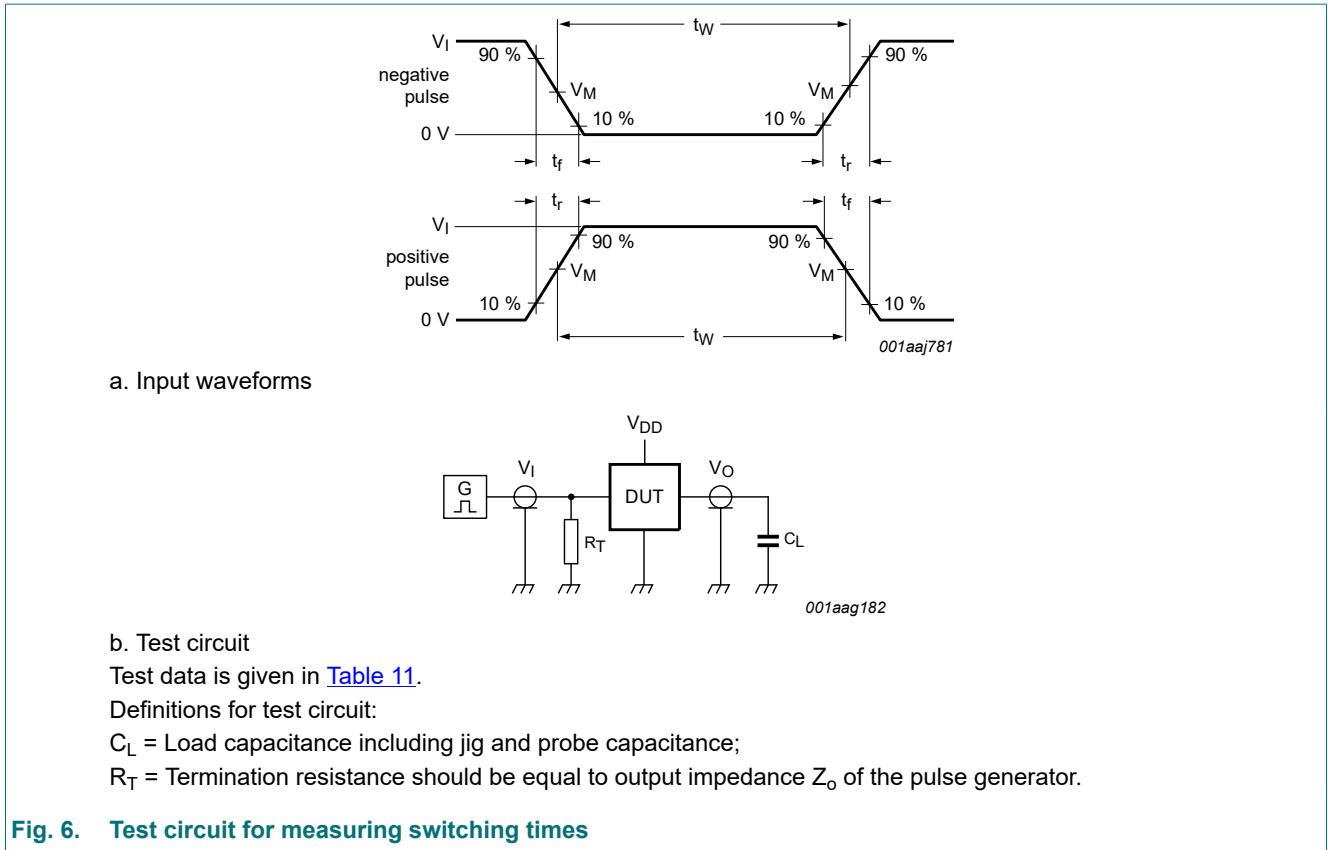


Table 11. Test data

Supply	Input	Load
$V_{DD}$	$V_I$	$C_L$
5 V to 15 V	$V_{SS}$ or $V_{DD}$	50 pF
	$t_r, t_f$	$\leq 20$ ns

## 12. Application information

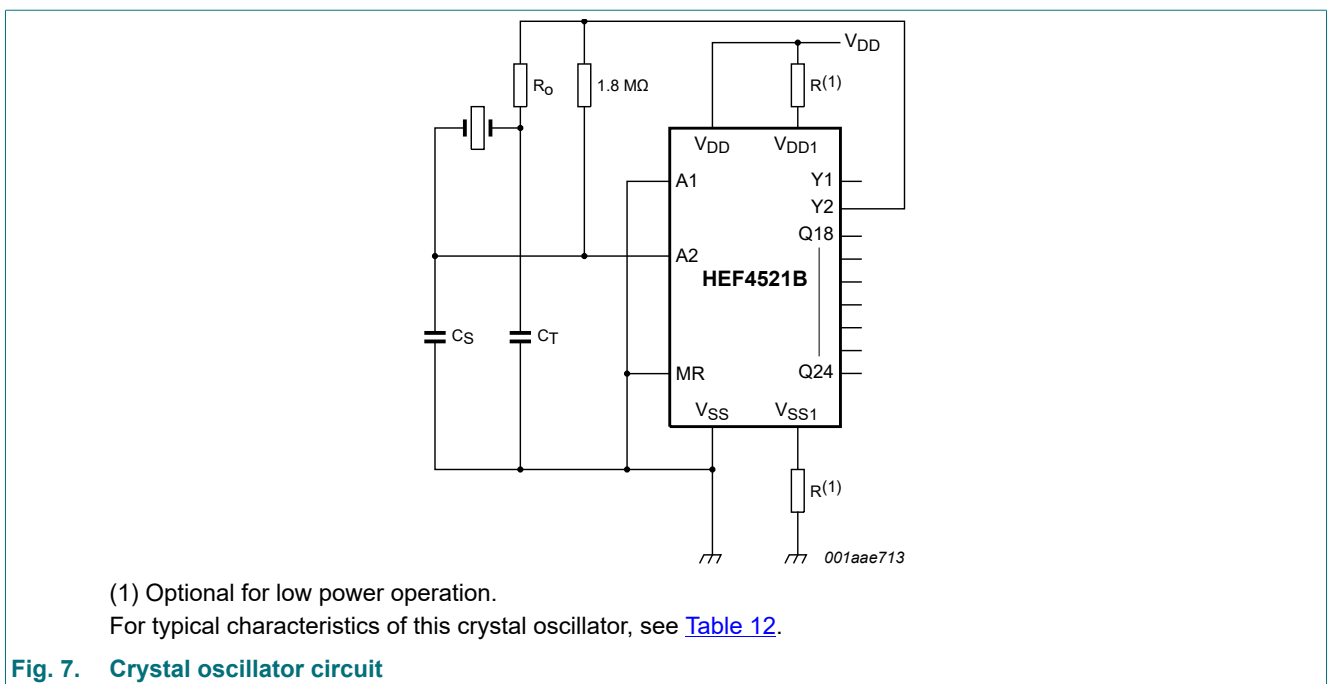


Table 12. Typical characteristics for crystal oscillator

Parameter	500 kHz circuit	50 kHz circuit	Unit
<b>Crystal characteristics</b>			
Resonance frequency	500	50	kHz
Crystal cut	S	N	-
Equivalent resistance; $R_S$	1	6.2	k $\Omega$
<b>External resistor/capacitor values</b>			
$R_o$	47	750	k $\Omega$
$C_T$	82	82	pF
$C_S$	20	20	pF

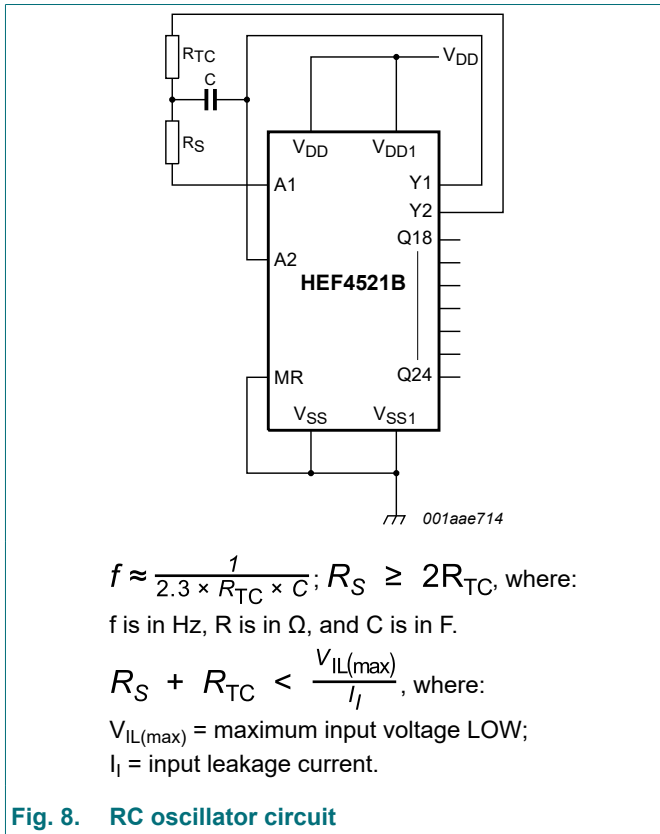


Fig. 8. RC oscillator circuit

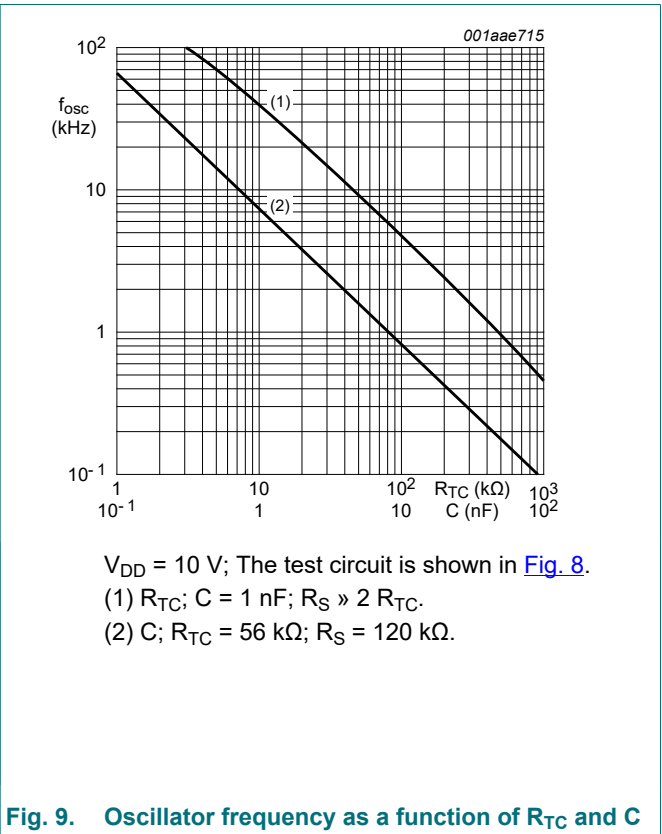
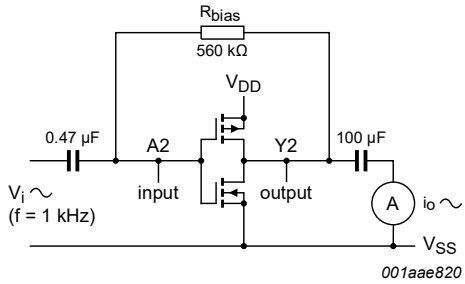
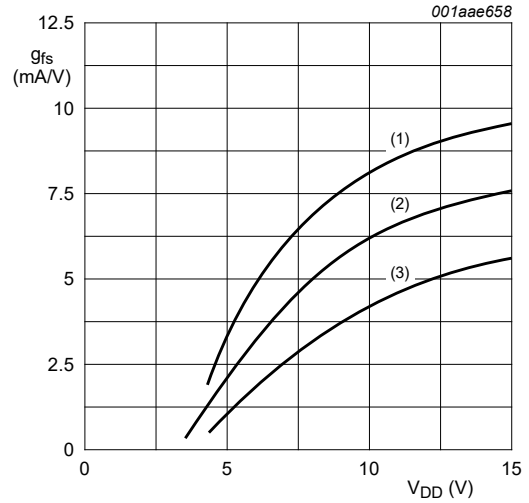


Fig. 9. Oscillator frequency as a function of  $R_{TC}$  and  $C$



$g_{fs} = d_{i_o}/d_{v_i}$  with  $v_o$  constant (see Fig. 11).

Fig. 10. Test setup for measuring forward transconductance

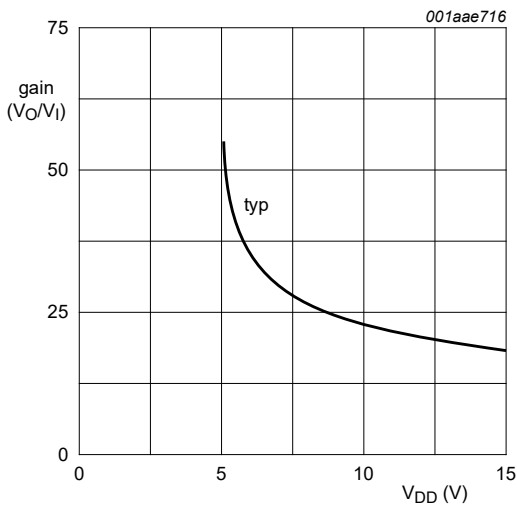


$T_{amb} = 25\text{ }^{\circ}\text{C}$ .

s = observed standard deviation.

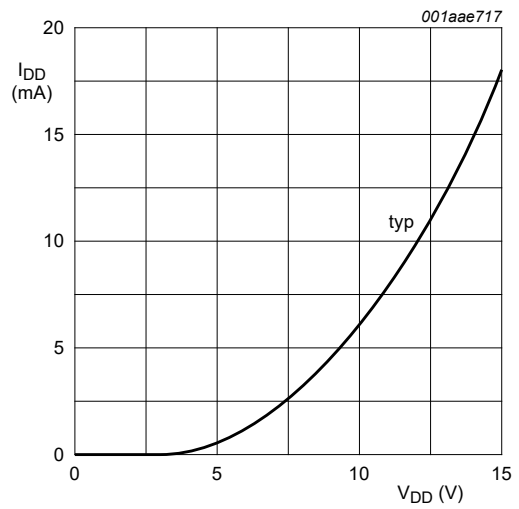
- (1) Average +2s
- (2) Average
- (3) Average -2s

Fig. 11. Typical forward transconductance  $g_{fs}$  as a function of the supply voltage



For test setup, see Fig. 14.

Fig. 12. Voltage gain  $V_o/V_i$  as a function of supply voltage



For test setup, see Fig. 14.

Fig. 13. Supply current as a function of supply voltage

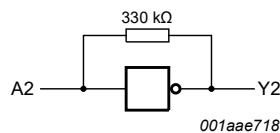


Fig. 14. Test setup for measuring the voltage gain and supply current graphs

13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

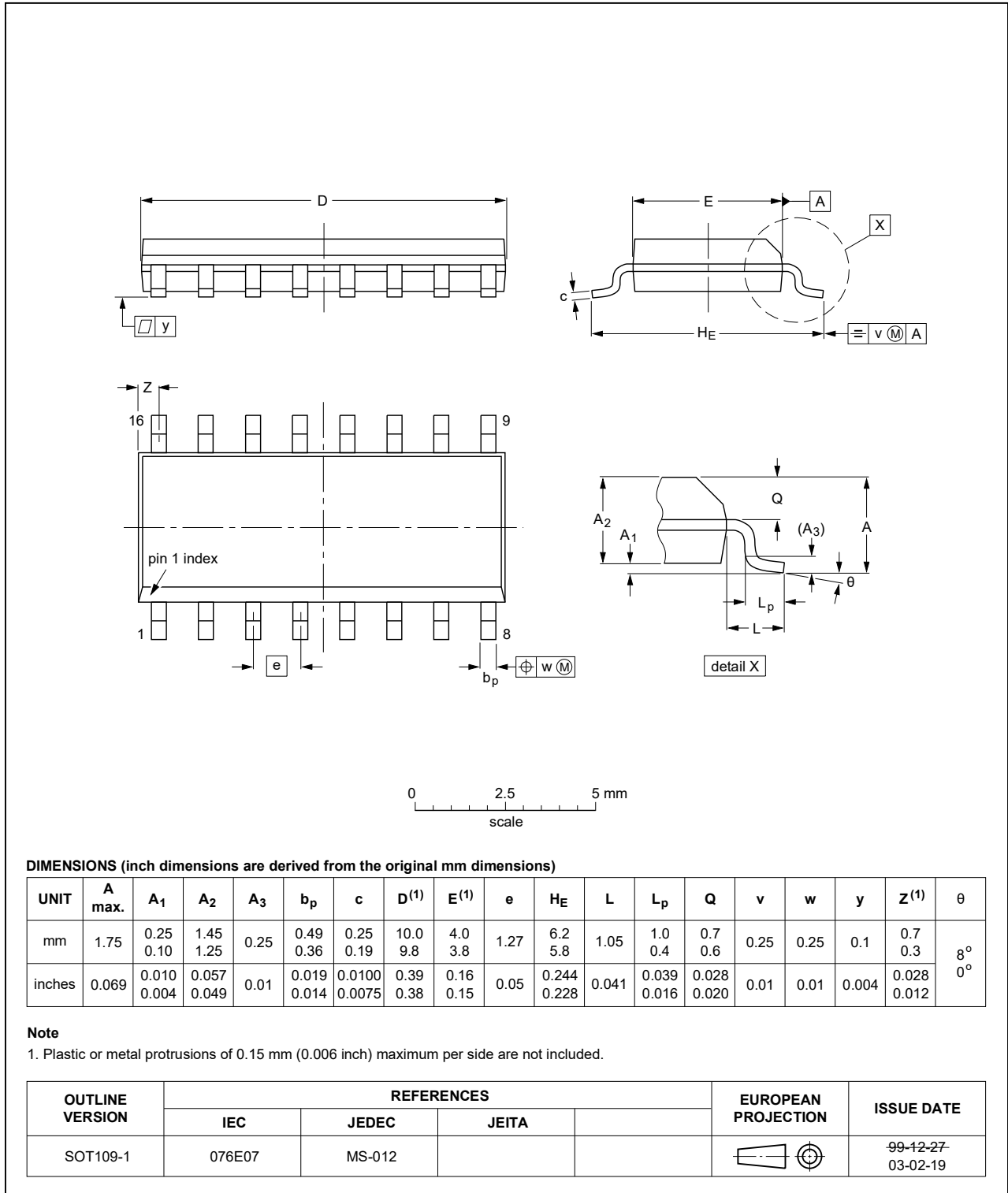


Fig. 15. Package outline SOT109-1 (SO16)

## 14. Abbreviations

Table 13. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

## 15. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4521B v.8	20211203	Product data sheet	-	HEF4521B v.7
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Section 2</a> updated.</li> <li><a href="#">Section 14</a> added.</li> </ul>			
HEF4521B v.7	20160330	Product data sheet	-	HEF4521B v.6
Modifications:	<ul style="list-style-type: none"> <li>Type number HEF4521BP (SOT38-4) removed.</li> </ul>			
HEF4521B v.6	20111121	Product data sheet	-	HEF4521B v.5
Modifications:	<ul style="list-style-type: none"> <li>Section Applications removed</li> <li><a href="#">Table 4</a>: added references to Table note [1] and [2]</li> <li><a href="#">Table 7</a>: I<sub>OH</sub> minimum values changed to maximum</li> <li><a href="#">Fig. 11</a>: space between "2" and "s" removed in figure notes [1] and [3]</li> </ul>			
HEF4521B v.5	20091105	Product data sheet	-	HEF4521B v.4
HEF4521B v.4	20090421	Product data sheet	-	HEF4521B_CNV v.3
HEF4521B_CNV v.3	19950101	Product specification	-	HEF4521B_CNV v.2
HEF4521B_CNV v.2	19950101	Product specification	-	-

## 16. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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