Non-Isolated, Buck PFC LED Driver with Digital Reference Control

Check for Samples: TPS92074

FEATURES

- **Controlled Reference Derived PFC**
- **Digital 50/60 Hz Synchronization**
- **Constant LED current operation**
- **Single Winding Magnetic Configurations**
- **Low Typical Operating Current**
- **Fast Start-up**
- **Overvoltage Protection**
- **Feedback Short-Circuit Protection**
- **Wide Temperature Operation Range**
- **Low BOM Cost and Small PCB Footprint**
- **Patent Pending Digital Architecture**
- **8-Pin SOIC and 6-Pin TSOT Available**

APPLICATIONS

- **Non Phase Dimmable LED Lamps**
- **Bulb Replacement**
- **Area Lighting**

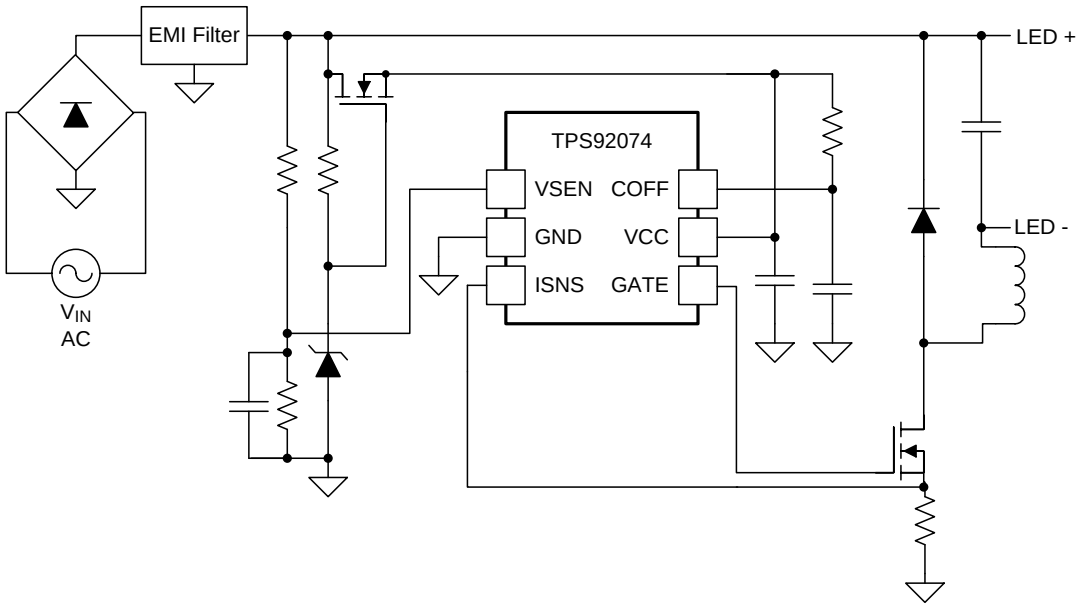
DESCRIPTION

The TPS92074 is a hybrid power factor controller (PFC) optimized for driving LED lighting solutions that do not require phase dimming compatibility. The device monitors the converter rectified AC waveform using an internal, low-power, digital controller. The controller and DAC generate a synchronized triangular reference to regulate the output current. By allowing for some variation in the LED current over a line cycle and maintaining a regulated overall average current, high power factor solutions can be achieved.

Using a constant off-time control, the solution achieves low component count, high efficiency and inherently provides variation in the switching frequency. This variation creates an emulated spread spectrum effect easing the converters EMI signature and allowing a smaller input filter.

The TPS92074 also includes standard features: current limit, overvoltage protection, thermal shut-down, and VCC undervoltage lockout, all in packages utilizing only 6 pins.

SIMPLIFIED APPLICATION DIAGRAM



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

All voltages are with respect to GND, –40°C < T_J = T_A < 125°C, all currents are positive into and negative out of the specified terminal (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Input voltage range	VCC	–0.3	22	V
	VSEN, COFF	–0.3	6.0	
Bias and ISNS	I_Q bias current (non-switching)		2.5	mA
	ISNS(2) to Ground	–0.3	2.5	V
Gate	GATE - continuous	–0.3	18	V
	GATE - 100 ns	–2.5	20.5	V
Continuous power dissipation		Internally Limited		
Electrostatic discharge	Human Body Model (HBM)		2	kV
	Field Induced Charged Device Model (FICDM)		750	V
Operating junction temperature, T_J(3)			160	°C
Storage temperature range, T_{stg}		–65	150	°C
Lead temperature, soldering, 10s			260	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) ISNS can sustain –2 V for 100 ns without damage.
(3) Maximum junction temperature is internally limited.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS92074		UNITS
		SOIC (D)	TSOT (DDC)	
		8 PINS	6 PINS	
θ_{JA}	Junction-to-ambient thermal resistance(2)	112.3	165.5	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	58.4	28.8	
θ_{JB}	Junction-to-board thermal resistance(4)	52.5	24.6	
ψ_{JT}	Junction-to-top characterization parameter(5)	12.5	0.3	
ψ_{JB}	Junction-to-board characterization parameter(6)	51.9	23.8	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	NA	NA	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS(1)

Unless otherwise noted, all voltages are with respect to GND, –40°C < T_J = T_A < 125°C.

	MIN	TYP	MAX	UNIT
Supply input voltage range VCC		11	18	V
Operating junction temperature	–40		125	°C

(1) Operating Ratings are conditions under which operation of the device is specified and do not imply assured performance limits. For specified performance limits and associated test conditions, see the Electrical Characteristics table.

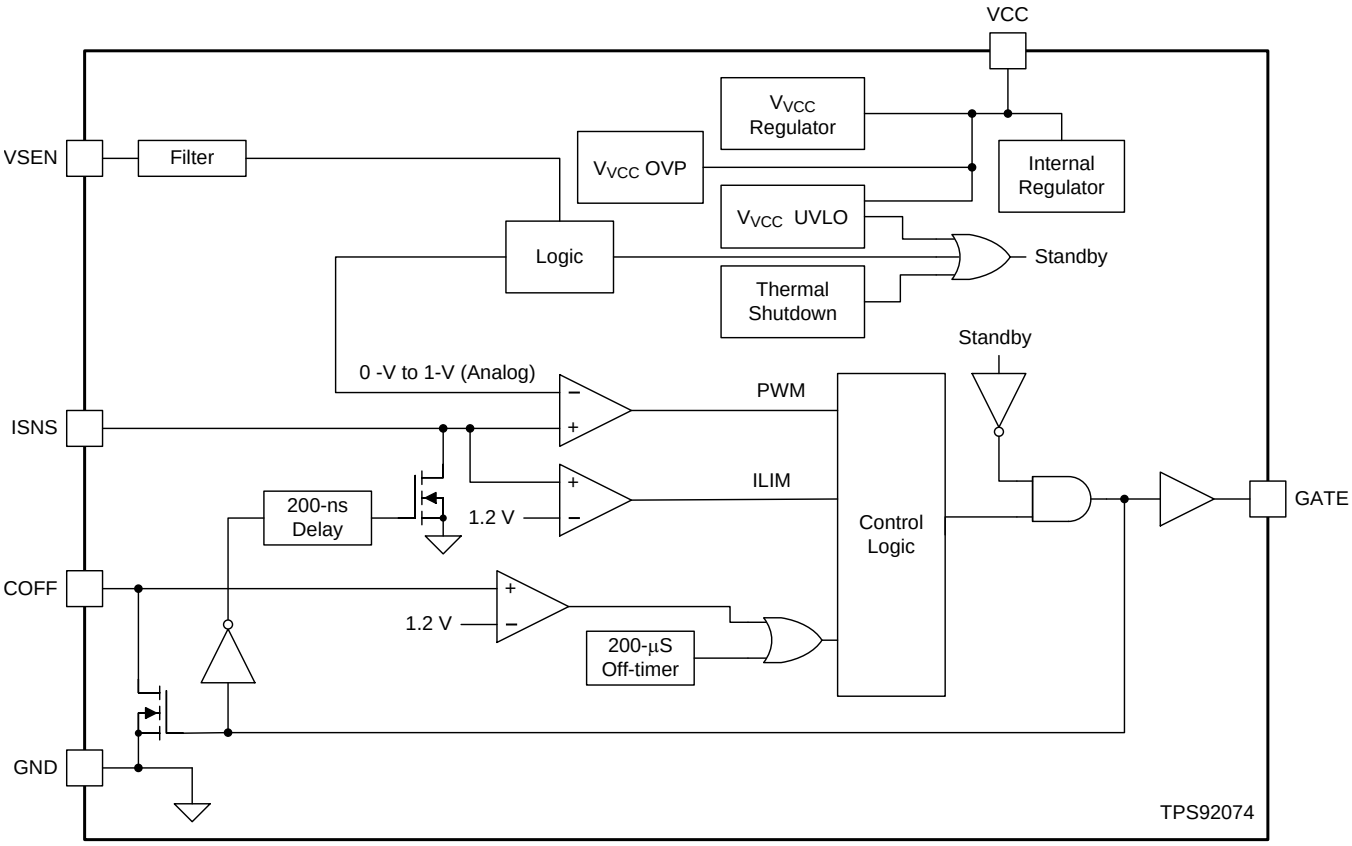
ELECTRICAL CHARACTERISTICS

Unless otherwise specified –40°C ≤ T_J = T_A ≤ 125°C, V_{CC} = 14 V, C_{VCC} = 10 µF C_{GATE} = 2.2 nF

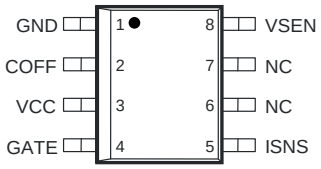
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE INPUT (VCC)						
I_Q	V_{VCC} quiescent current	Not switching		1.3	2.5	mA
I_{Q_SD}	V_{VCC} low power mode current	V_{CC} < $V_{CC(UVLO)}$		120	250	µA
V_{VCC}	Input range	V_{CC} ≤ $V_{CC(OVP)}$			18	V
$V_{VCC(OVP)}$	Overvoltage protection threshold	V_{CC} > $V_{CC(OVP)}$	18.0		20.0	V
$V_{VCC(UVLO)}$	V_{VCC} UVLO threshold	V_{CC} rising		9.8	10.5	V
		V_{CC} falling	5.75	6.40		V
$V_{VCC(HYS)}$	V_{VCC} UVLO hysteresis			3.3		V
LINE SYNCHRONIZATION						
$VSEN_{TH-Hi}$	VSEN line detect rising threshold		0.9	1.0	1.1	V
$VSEN_{TH-Low}$	VSEN line detect falling threshold		0.465	0.500	0.540	V
OFF-TIME CONTROL						
V_{COFF}	OFF capacitor threshold		1.14	1.20	1.285	V
R_{COFF}	OFF capacitor pull-down resistance			33	60	Ω
$t_{OFF(max)}$	Maximum off-time			280		µs
GATE DRIVER OUTPUT (GATE)						
$R_{GATE(H)}$	Gate sourcing resistance			3	8	Ω
$R_{GATE(L)}$	Gate sinking resistance			3	8	Ω
CURRENT SENSE						
V_{ISNS}	Average ISNS limit threshold	DAC: 63/127	445	500	555	mV
V_{CL}	Current limit			1.2		V
t_{ISNS}	Leading edge blanking			240		ns
	Current limit reset delay			280		µs
	ISNS limit to GATE delay			33		ns
t_{COFF_DLY}	OFF capacitor limit to GATE delay			33		ns
THERMAL SHUTDOWN						
T_{SD}	Thermal limit threshold			160		°C
T_{HYS}	Thermal limit hysteresis			20		°C

DEVICE INFORMATION

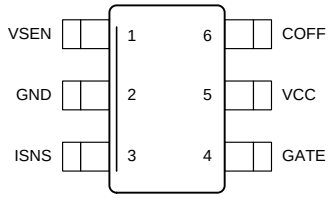
FUNCTIONAL BLOCK DIAGRAM



SOIC (D) PACKAGE
8 PINS
(TOP VIEW)



TSOT (DDC) PACKAGE
6 PINS
(TOP VIEW)



PIN DESCRIPTIONS

NAME	PIN NUMBERS		I/O	DESCRIPTION
	SIOC (D)	TSOT (DDC)		
COFF	2	6	I	Used to set the converter constant off-time. A current and capacitor connected from the output to this pin sets the constant off-time of the switching controller.
GATE	4	4	O	Power MOSFET driver pin. This output provides the gate drive for the power switching MOSFET.
GND	1	2	—	Circuit ground connection
ISNS	5	3	I	LED current sense pin. Connect a resistor from main switching MOSFET source to GND to set the maximum switching cycle LED current. Connect ISNS to the switching FET source.
VCC	3	5	—	Input voltage pin. This pin provides the power for the internal control circuitry and gate driver. V_{CC} undervoltage lockout has been implemented with a wide range: 10V rising, 6V falling to ensure operation with start-up methods that allow elimination of the linear pass device. This includes using a coupled inductor with resistive start-up.
VSEN	8	1	I	The line voltage and frequency are detected through this pin and fed to the digital decoder. Sensing thresholds are 1V rising and 0.5V falling – nominal.

TYPICAL CHARACTERISTICS

Unless otherwise stated, –40°C ≤ T_A = T_J ≤ 125°C, V_{VCC} = 14 V, C_{VCC} = 10 µF C_{GATE} = 2.2 nF

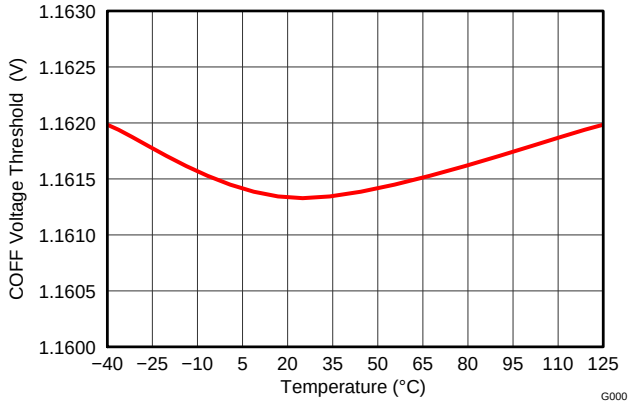


Figure 1. COFF Threshold Voltage vs Temperature

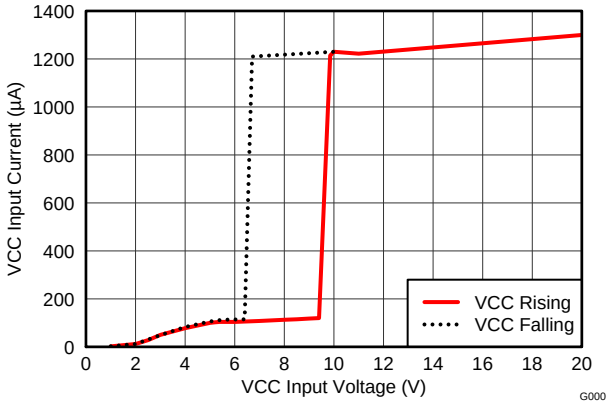


Figure 2. VCC Input Current vs Vcc Input Voltage

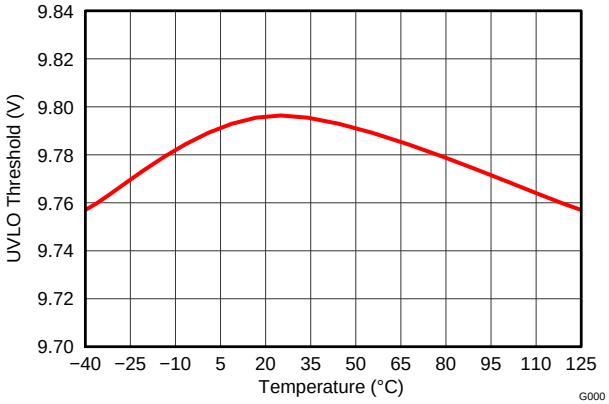


Figure 3. Input Voltage (UVLO Rising) vs Junction Temperature

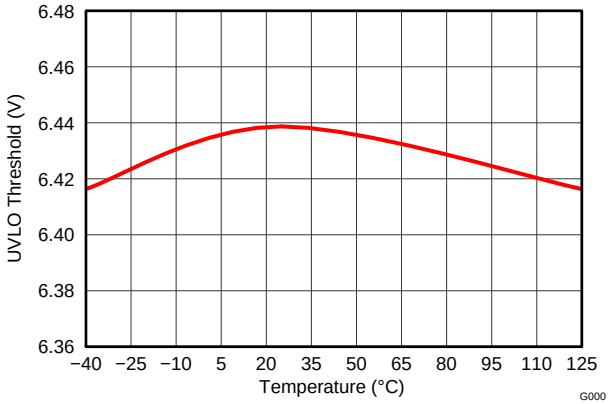


Figure 4. Input Voltage (UVLO Falling) vs Junction Temperature

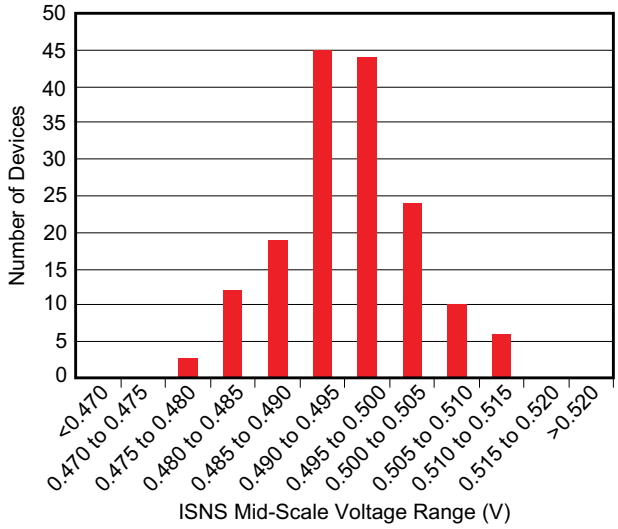


Figure 5. ISNS 0.5V Threshold Distribution

APPLICATION INFORMATION

The TPS92074 is an AC-DC power factor correction (PFC) controller for LED lighting applications. A hysteretic, peak current, constant off-time approach implements the conversion.

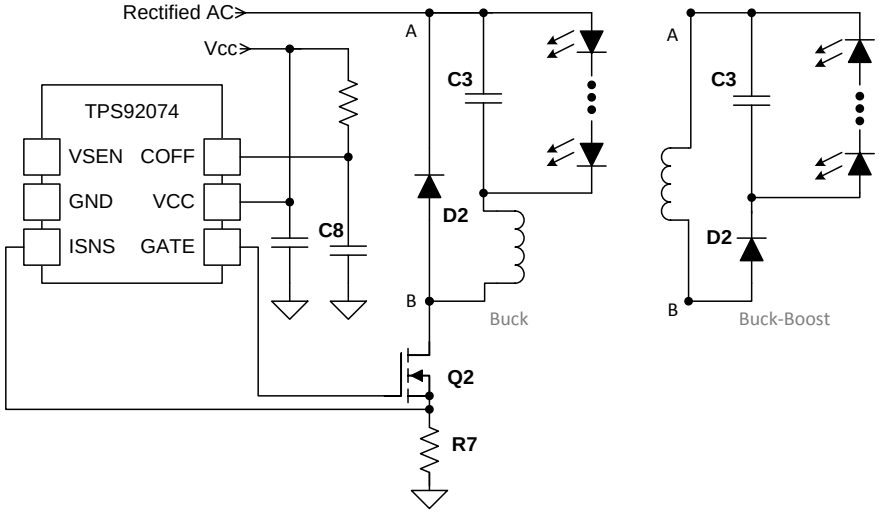


Figure 6. Simplified TPS92074 Schematic

The TPS92074 controls the inductor current by controlling two features: (A) The peak inductor current, and (B) The cycle off-time. The following items summarize the basics of the switch operation in this hysteretic controller.

- The main switch Q2 turns on and current ramps in the inductor.
- The Q2 current flows through the sense resistor R7. The R7 voltage is compared to a reference voltage at ISNS. The Q2 on-time ends when the voltage on R7 is equal to a controlled reference voltage and the inductor current has reached its set peak current level for that switching cycle.
- Q2 is turned off and a constant off-time timer begins. Voltage begins ramping on C8.
- The next cycle begins when the voltage on C8 reaches 1.2 V. This ends the constant off-time and discharges C8.
- Capacitor C3 eliminates most of the ripple current seen in the LEDs.

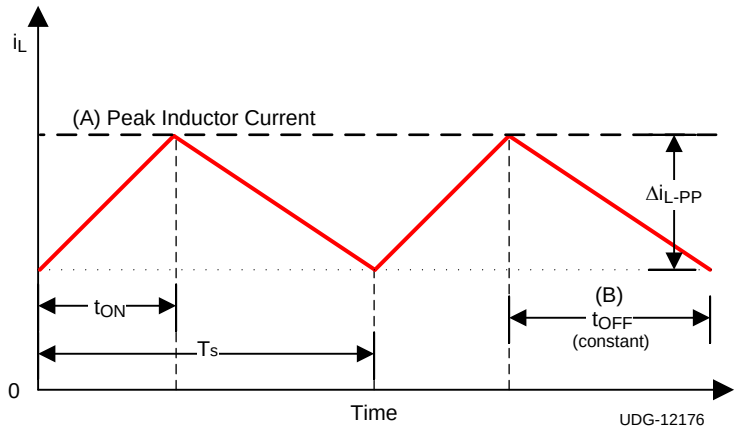


Figure 7. Current Regulation Method

The TPS92074 incorporates a patent-pending control methodology to generate the reference for the conversion stage.

Initial Start-Up

The TPS92074 is designed to achieve instant turn-on using an external linear regulator circuit. The start-up sequence is internally controlled by a V_{CC} under-voltage lockout (UVLO) circuit. Sufficient headroom has been incorporated to support the use of an auxiliary winding with start-up linear, resistive or coupled capacitor start-up methods.

VCC Bias Supply

The TPS92074 can be configured to use a linear regulator with or without the use of an auxiliary winding. Using a linear regulator to provide V_{CC} incurs more losses than an auxiliary winding, but has several advantages:

- allows the use of inexpensive off-the-shelf inductors as the main magnetic
- can reduce the size of the required VCC capacitor to as low as 0.1uF

Another consideration when selecting a bias method involves the OVP configuration. Because the feature is enabled via the VCC pin, an auxiliary winding provides the simplest implementation of output over-voltage protection.

A typical start-up sequence begins with V_{VCC} input voltage below the UVLO threshold and the device operating in low-power, shut-down mode. The V_{VCC} input voltage increases to the UVLO threshold of 9.8V typical. At this point all of the device features are enabled. The device loads the initial start-up value as the output reference and switching begins. The device operates until the V_{VCC} level falls below the $V_{CC(UVLO)}$ falling threshold. (6.4V typical) When V_{VCC} is below this threshold, the device enters low-power shut-down mode.

Voltage Sense Operation

The VSEN (voltage sense) pin is the only input to the digital controller. The time between the rising edge and the falling edge of the signal determines converter functions. The pin incorporates internal analog and digital filtering so that any transition that remains beyond the threshold for more than approximately 150 µs will cause the device to record a change-of-state.

Controller

Basic Operation

The controller continuously monitors the line cycle period. Control algorithms use a normalized line period of 256 samples from VSEN fall to VSEN fall and a normalized converter reference control of 127 levels over a range of 0V to 1V .

The two main controller states are:

- Start-Up
- Normal Operation

After the initial start-up period where the reference is a DC level, the reference is changed to a triangular ramp to achieve a high power factor. The ramp generates gradually over several cycles ensuring the change is undetectable. The controller maintains the ramp between the rising and falling VSEN signals.

Table 1. Control States and Controlled Reference Values

MODE	LINE DUTY CYCLE	CONTROLLED REFERENCE VALUE (value / 127) X 1 V = reference
Start-up	Any	50
Normal Operation	Typical Average	55
	Typical Ramp Range	22 to 127
No VSEN	Any	42

Initial Start-up

Line Synchronization

When the device reaches the turn-on UVLO threshold, the output current reference resets to 0.393 V (50/127) and switching begins. The controller samples the line for approximately 80 ms (t_1 to t_2 , Figure 8) to determine the line frequency and establish the present state of operation. After determining the line frequency, the controller uses the information to calibrate the internal oscillator. The controller supports line frequencies from 45 Hz to 65 Hz. After determining frequency and duty cycle, the controller enters normal operation.

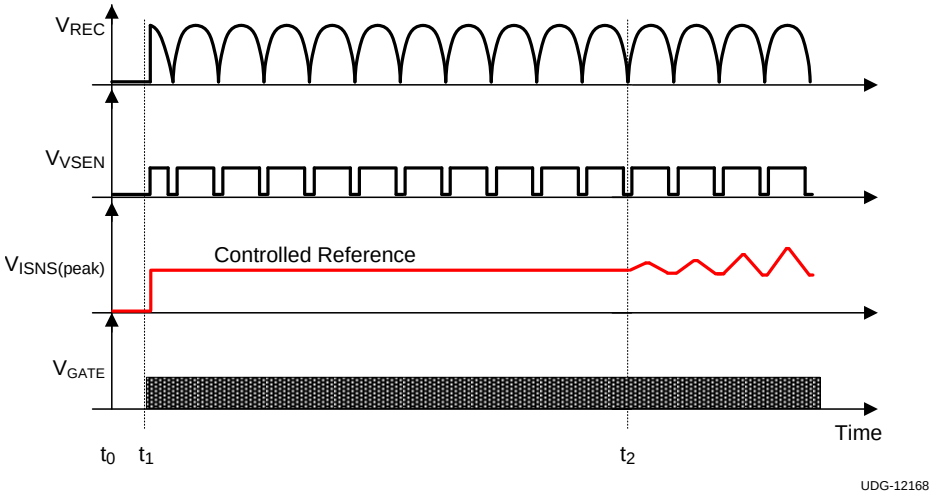


Figure 8. Line Synchronization

Triangular Ramp Creation

After the start-up period, the controller creates a triangular ramp that is synchronized to the line and is centered between rising and falling edges of the VSEN signal as shown in Figure 9.

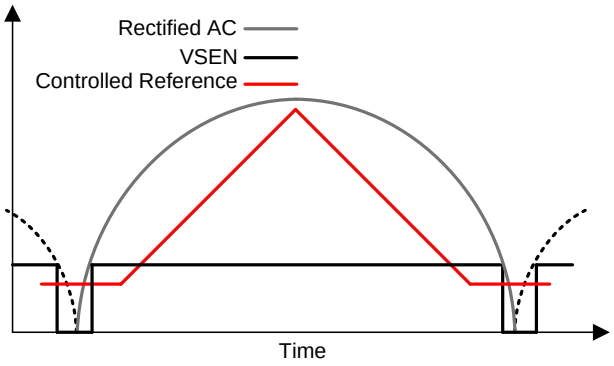


Figure 9. Controlled Reference Output

At start-up the ramp is created over 127 line cycles (see Figure 10) or approximately 1 second (t_2 to t_3 ≈ 1 second). Because the output level before and after the change is very similar and the change very gradual, it is impossible for the user to perceive a change in output level. The ramp converts from a DC level to a ramp using a method that further ensures transparency to the user.

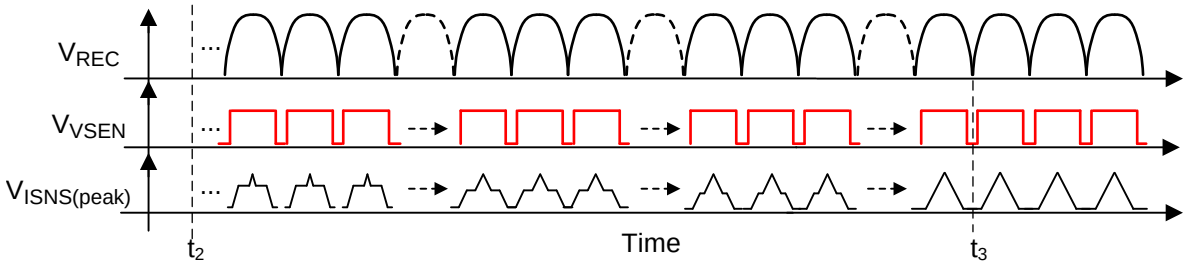


Figure 10. Transition Stages of the Controlled Reference during Start-Up

Loss of Voltage Sense

If a circuit malfunction or failure occurs causing the VSEN singal to become too narrow or to be lost completely, the controller simply sets the reference to a default value 0.33 V (42/127) and waits for the VSEN signal to return.

Not Using Voltage Sense

A simplified version of the TPS92074 circuit can be implemented by grounding the VSEN signal if minimum component count and size are essential design criteria. In this configuration, the triangular ramp reference is not implemented. The output is controlled with a default, static reference of 0.394 V (50/127). If used in conjunction with an on-time clamp and the appropriate LED stack voltage, power factors (> 0.9) can still be achieved, but THD is higher without the ramp waveform.

Thermal Shutdown

The TPS92074 includes thermal shutdown protection. If the die temperature reaches approximately 160°C the device stops switching (GATE pin low). When the die temperature cools to approximately 140°C, the device resumes normal operation.

If thermal foldback is desired at levels below the device thermal shut down limit, application circuit design features implement this protection. The most simple of these design features is the addition of a thermistor in the off-time circuitry.

Thermal Foldback

To implement thermal foldback, adjust the resistance of an existing circuit resistor with the use of an NTC (negative temperature coefficient) thermistor.

For example, a resistor combination creating a dominant effect when the thermistor reaches the desired temperature and resistance can be incorporated by paralleling a thermistor and another resistor like R10 with the suggested On-Time clamp (see Figure 12.). This circuit option creates a shorter on-time as the temperature increases, reducing the output current. The use of a thermistor (NTC or PTC) in these types of circuit implementations is simple and saves costly added circuitry and additional device pins.

Overvoltage Protection (OVP)

The implementation of overvoltage protection is simple and built-in if using a two-coil magnetic (coupled inductor) to derive V_{CC}. If the LED string is opened the auxiliary V_{CC} rises and reaches the $V_{CC(OVP)}$ trip point. This action disables and grounds the gate pin, preventing the converter from switching. The converter remains disabled until V_{CC} drops 0.5 V after a 1 second time-out. If an inductor is used, implement other discrete circuits to disable the converter.

Output Bulk Capacitor

The required output bulk capacitor, C_{BULK}, stores energy during the input voltage zero crossing interval and limits twice the line frequency ripple component flowing through the LEDs. Equation 1 describes the calculation of the of output capacitor value.

$$C_{BULK} \geq \frac{P_{IN}}{4\pi \times f_L \times R_{LED} \times V_{LED} \times I_{LED(ripple)}} \quad (1)$$

where

- R_{LED} is the dynamic resistance of LED string
- $I_{LED(ripple)}$ is the peak to peak LED ripple current
- and f_L is line frequency

Compute R_{LED} as the difference in LED forward voltage divided by the difference in LED current for a given LED using the manufacturer's V_F vs. I_F curve. For an initial estimate, a typical value of 0.25 Ω per LED can be used. More detail can be found in the Application Report Design Challenges of Switching LED Drivers (AN-1656).

In typical applications, the solution size becomes a limiting factor and dictates the maximum dimensions of the bulk capacitor. When selecting an electrolytic capacitor, manufacturer recommended de-rating factors should be applied based on the worst case capacitor ripple current, output voltage and operating temperature to achieve the desired operating lifetime. It should also be a consideration to provide a minimum load at the output of the driver to discharge the capacitor after the power is switched off or during LED open circuit failures.

Design Guidelines

This TPS92074 application design requires the selection of components for the power conversion stage and line sensing. Output inductor, sense resistor and switching frequency are the key aspects of the power stage design. Another important consideration is the inclusion of an on-time clamp. The combination of the line voltage going to zero at each cycle and the hysteretic control method can lead to large increases in current draw at the start and end of each cycle. The components required for the on-time clamp are very inexpensive and they return results that make their inclusion a common choice for LED driver designers. This simplified design procedure assumes the use of an on-time clamp in the design.

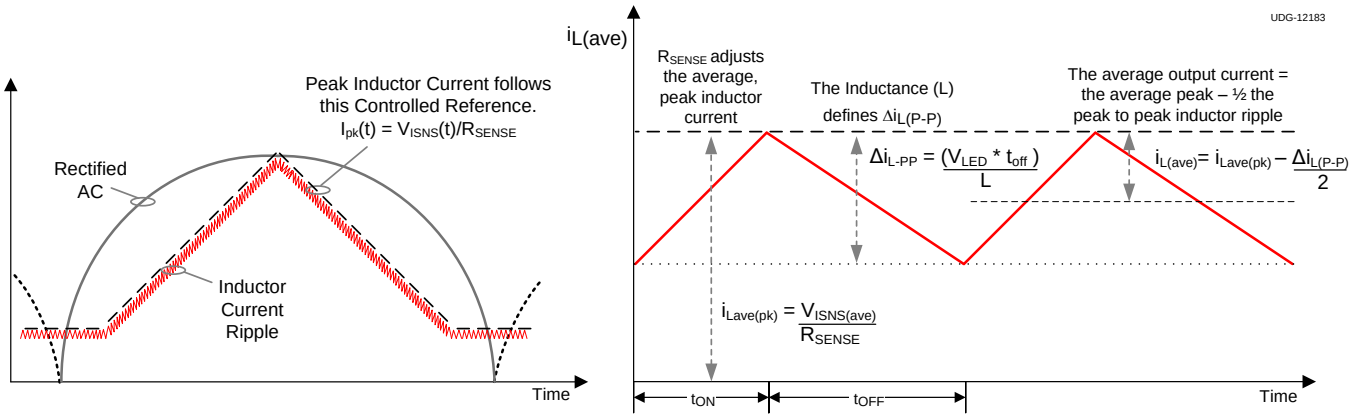


Figure 11. TPS92074 Output Current Control

The device uses the controller reference during every switching cycle. This controller reference sets the peak current through the main switch and sense resistor. The average value of this reference and the inductor ripple current can be used to calculate the average output current. Also consider the length of time the converter provides power to the LEDs based on the LED stack voltage. A conversion factor (CF) that accounts for a lower level of power conversion at the ends of each cycle is used to provide a more accurate sense resistor value. The lower level of power conversion in these areas also helps to increase the power factor. For the R_{SENSE} calculation use $V_{ISNS\ (ave)}$ = 0.433 V (55/127). The CF calculation involves computing the normalized time length of the voltage sense pulse using a formula shown in Equation 3. See the simplified design expressions in Equation 2 through Equation 6. For a more comprehensive approach refer to the TPS92074 Design Spreadsheet.

To calculate R_{SENSE}, use Equation 2.

$$R_{SENSE} = \left(\frac{V_{ISNS(ave)}}{I_{LED} + \frac{\Delta i_{L(P-P)}}{2}} \right) \times CF \tag{2}$$

To calculate the conversion factor, use Equation 3.

$$CF = 1 - \left(\frac{\sin^{-1}\left(\frac{V_{LED}}{\sqrt{2} \times V_{RMS}} \right)}{90} \times \frac{3}{2} \right) \tag{3}$$

To calculate inductance ripple, use Equation 4.

$$\Delta i_{L(P-P)} = \left(\frac{V_{LED} \times t_{OFF}}{L} \right) \tag{4}$$

To calculate the constant off-time, use Equation 5

$$t_{OFF} = \left(\ln\left(-\left(\frac{1.2}{V_{VCC}} - 1 \right) \right) \right) \times \left(-C_{TOFF} \times R_{COFF} \right) \quad (5)$$

To calculate the average switching frequency, use Equation 6.

$$f_{SW} = \left(\frac{1}{t_{OFF} + \left(t_{OFF} \times CF \right)} \right) \quad (6)$$

General Approach to Buck and Buck-Boost PFC Design

To maintain a high power factor and low THD, create an input current waveform equivalent to what would be seen in a purely resistive load. A resistive load (like an incandescent light bulb) can draw power until the line zero cross. A buck converter driving an LED load can provide power only while the input line is greater than the LED stack voltage. This situation creates a limitation in the selection of LED stack voltage. Currently in non-LED load, buck PFC applications, a commonly accepted output voltage that maintains acceptable THD and PFC levels is one that maintains a 50% conduction angle each line cycle. See the TI Application Report *Power Factor Correction Using the Buck Topology*(SLUP264) In practical terms this equates to 90 VDC for a 90 VAC minimum input. For LED driver solutions this rule can be followed if the goal is simply a power factor ≥0.9. If the goal is also THD less than 20% then stricter requirements must be followed. In general, designs with an LED stack voltage beyond 45 V have difficulty achieving < 20% THD. For these solutions, a buck-boost topology should be used so that the circuit has the capability to draw current from the line below the LED stack voltage.

On-Time Clamp

The use of an on-time clamp (see Figure 12) provides soft-start and soft-stop functionality to the conversion during each line cycle. The clamp also allows an opportunity to control the energy in these conversion areas to optimize THD. For example, reducing the energy conversion in these areas helps to create an input current that is more sinusoidal in shape. Without it, the current can rise quickly at the start and end of each cycle as the converter goes in and out of drop-out. Solutions having a power factor ≥0.9 are still achievable, but the design must use the on-time clamp to obtain very low THD.

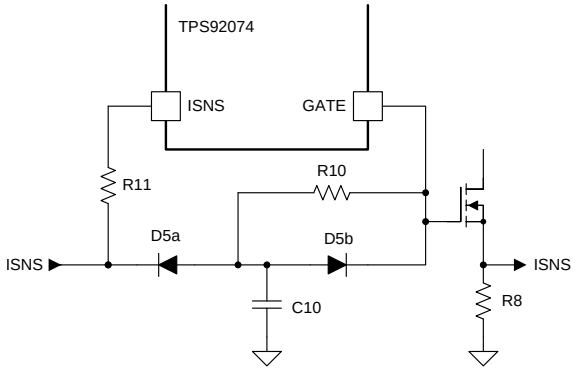


Figure 12. On-time Clamp Circuitry

The circuit uses the gate drive output to generate a ramp. The ramp increases at a rate to reach the current sense trip point at the desired maximum conduction time. The gate signal, resistor R10 and capacitor C10 create the ramp. Diode D5b resets the ramp for each switching cycle. Resistor R11 provides an impedance so this signal can override ISNS.

In the regions at the start and end of a line cycle the current sense reference is controlled to 0.173 V (22/127). To select an R-C to reach this point in the desired time use Equation 7. A good starting estimate for the maximum on-time clamp is approximately one-half of t_{OFF} . For example, choosing 33 nF as the value of capacitor C10, and assuming $V_{GATE} \approx V_{CC}$, R10 ($R_{ton(max)}$) is calculated in Equation 7.

$$R_{ton(max)} = \frac{t_{OFF}}{2 \times \left[\ln\left(-\left(\frac{0.173}{V_{GATE}} - 1 \right) \right) \right] \times -C_{ton(max)}} \quad (7)$$

Voltage Sense Circuitry and Minimum VSEN Signal Length

If the design topology is a buck converter, select the divider so the falling 0.5-V VSEN threshold is reached when the rectified AC voltage is at the LED stack voltage. For example, if the LED stack is 20 V and the top resistor is 400 kΩ, the bottom resistor should be 10.25 kΩ to provide a falling VSEN signal at 0.5 V when the rectified AC reaches 20 V. A 20-V VSEN falling signal corresponds to a 40-V VSEN rising threshold because of the 2:1 hysteresis. These thresholds provide a VSEN signal length of approximately 7.4 ms. This length is adequate to activate the ramp mode. Regardless of the VSEN connection method used, the divider must ensure an adequate voltage sense time (t_{VSEN} > 5.9 ms) to activate the creation of the triangular reference. For example, if a straight resistor divider (as shown in Figure 13) is implemented and the design LED stack is more than 42 V, the VSEN conduction time may not be adequate to ensure use of the ramp reference by the controller.

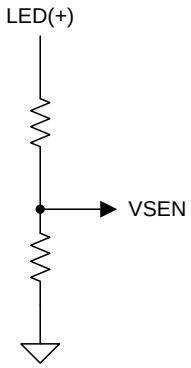


Figure 13. Voltage Sense for Low Voltage Buck Applications

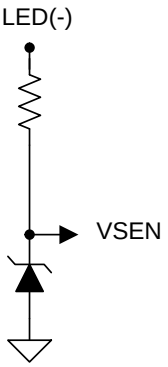


Figure 14. Voltage Sense for Buck Applications up to 65V

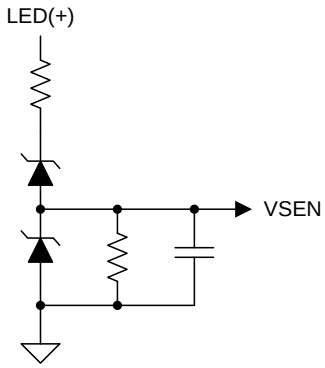


Figure 15. Voltage Sense for Buck-Boost Applications

For LED stack voltages between 3 V and 65 V, use an alternate method that senses from LED(–). Because LED(–) reaches ground each line cycle, the absolute VSEN comparison limits of 0.5 V and 1 V can be used, providing extra conduction time for the VSEN signal as shown in Figure 14. When using an LED stack, with an approximate voltage of more than 65-V, use an alternate VSEN methods such as a bridge tap. For buck-boost applications, implement the circuit shown in Figure 15.

A capacitor on the VSEN pin may be required, depending on operating conditions.

EMI Filtering: AC versus DC side of the rectifier bridge

The TPS92074 requires a minimal amount of EMI filtering to pass conducted and radiated emissions levels to comply with agency requirements. Applications have been tested with the filter on the AC or DC side of the diode bridge and have obtained passing results. The use of an R-C snubber to damp filter resonances is strongly recommended. The EMI filter design involves optimizing several factors and design considerations, including:

- the use of ‘X’ versus non-X rated filter capacitors
- the use of ceramic versus film capacitors
- component rating requirements when on the AC or DC side of the diode bridge
- snubber time constant and position in the design schematic
- filter design choices and audible noise

Application Circuits

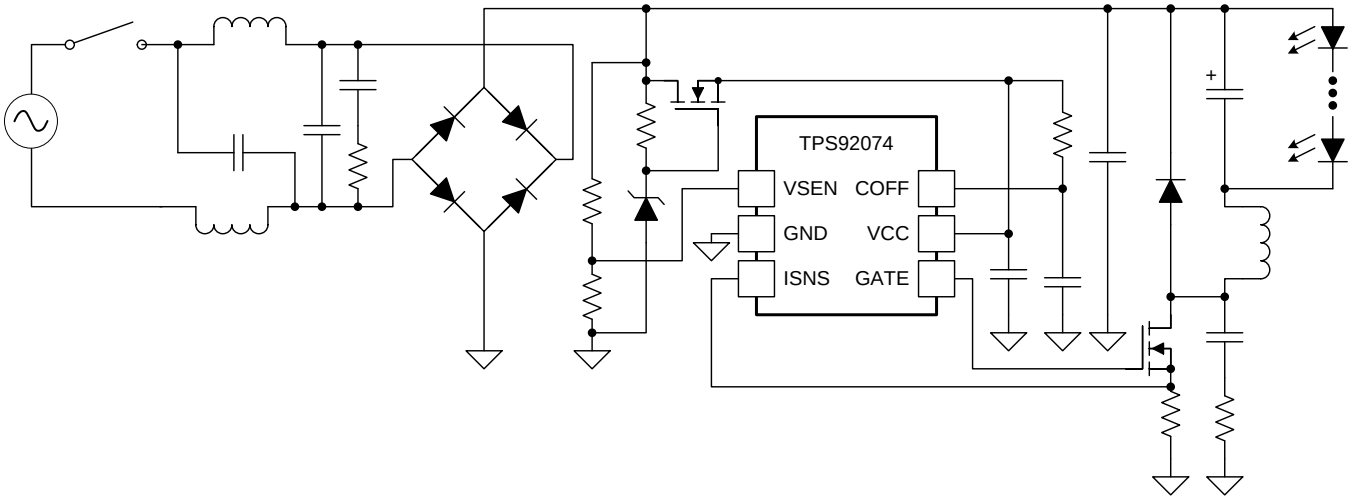


Figure 16. TPS92074 Buck Topology with AC Side Filter

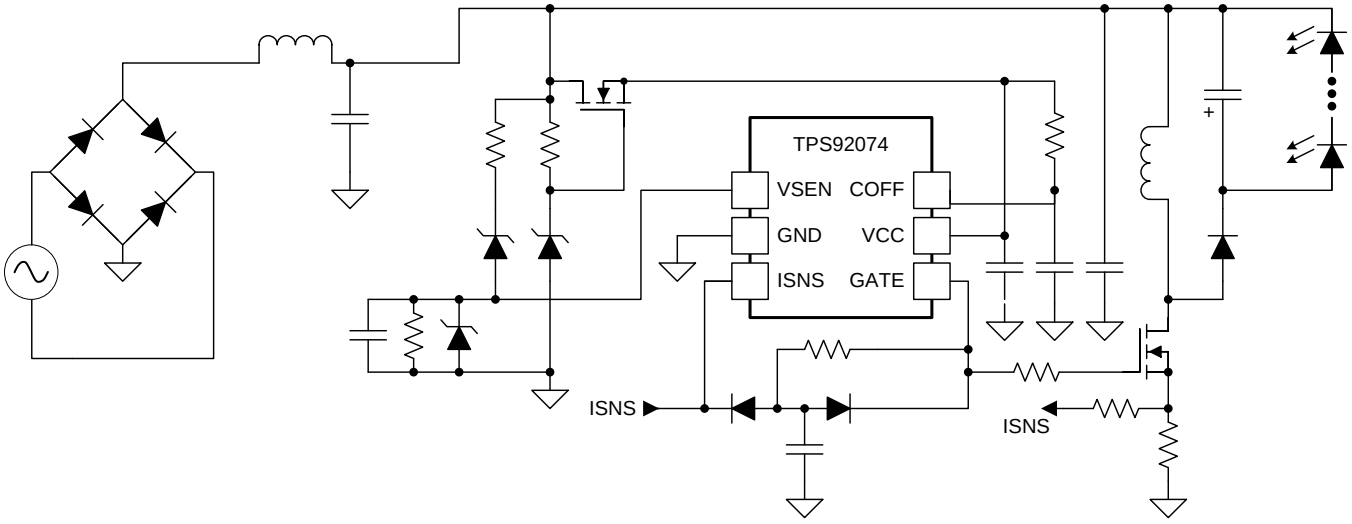


Figure 17. TPS92074 Buck-Boost Topology with DC Side Filter

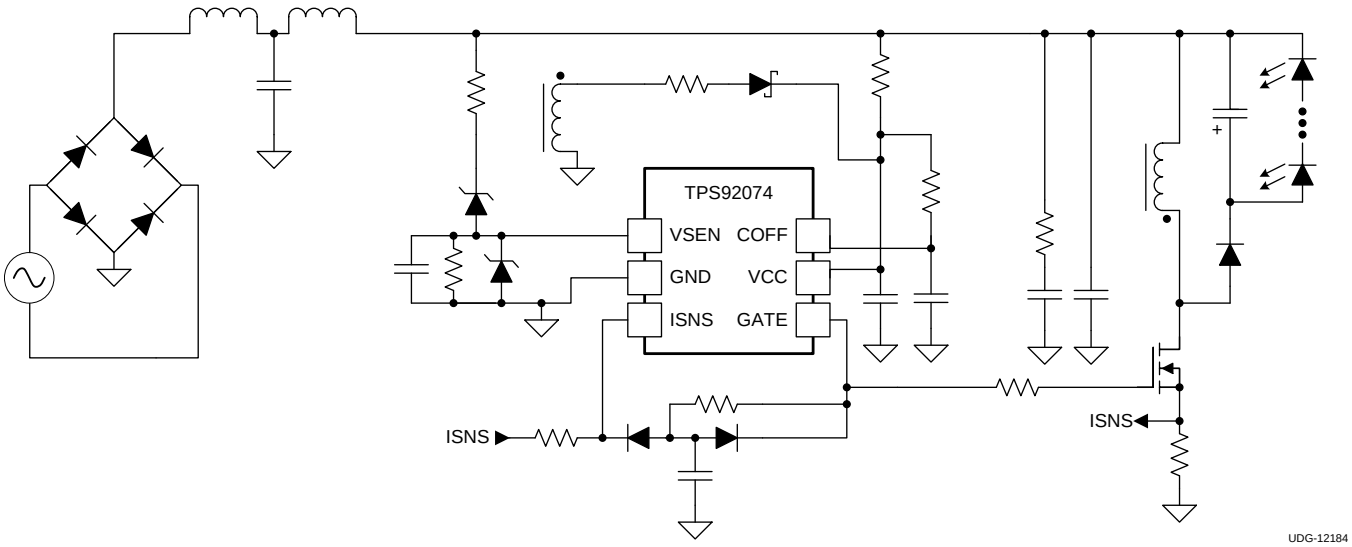


Figure 18. TPS92074 Buck-Boost Topology with Resistive Start-up and AUX Supply

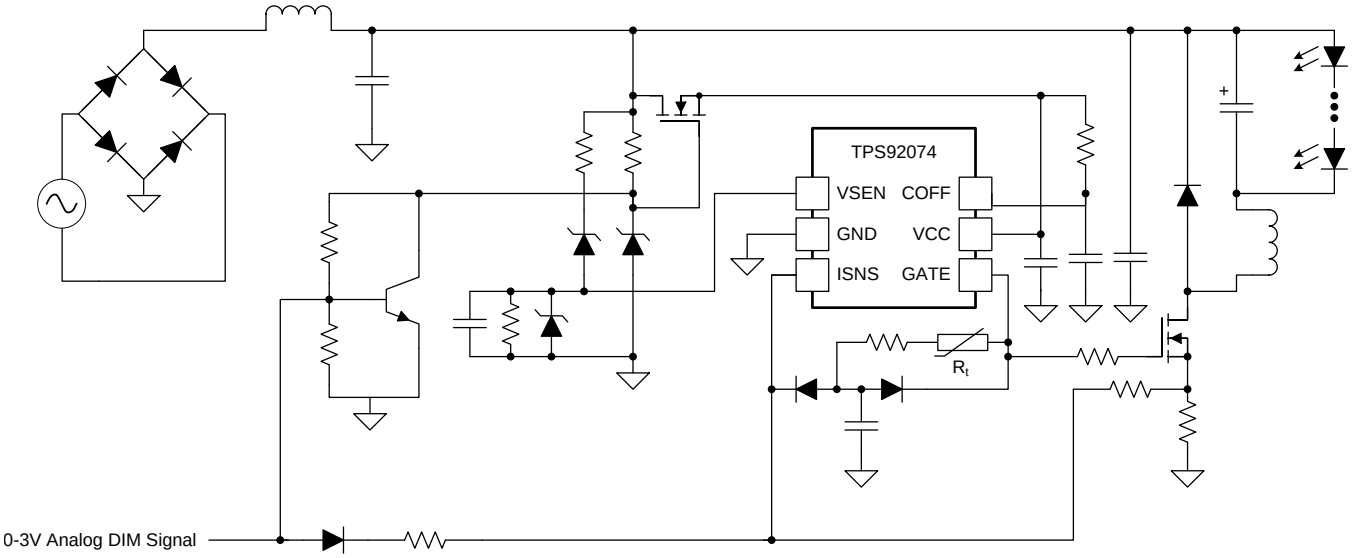


Figure 19. TPS92074 Buck Topology with Thermal Foldback and Analog Dimming (0 to 100%)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS92074D	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	T92074	Samples
TPS92074DDCR	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PC5Q	Samples
TPS92074DDCT	ACTIVE	SOT-23-THIN	DDC	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PC5Q	Samples
TPS92074DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	T92074	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

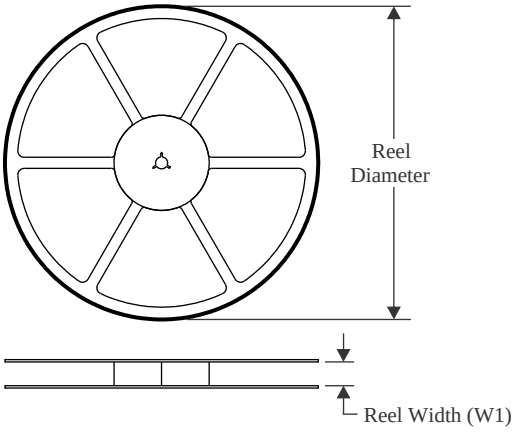
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

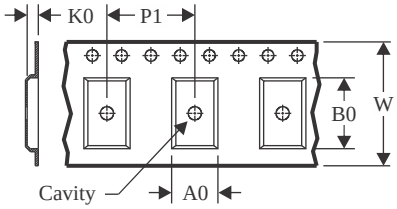
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

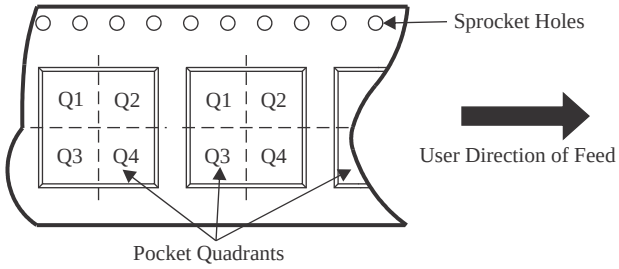


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

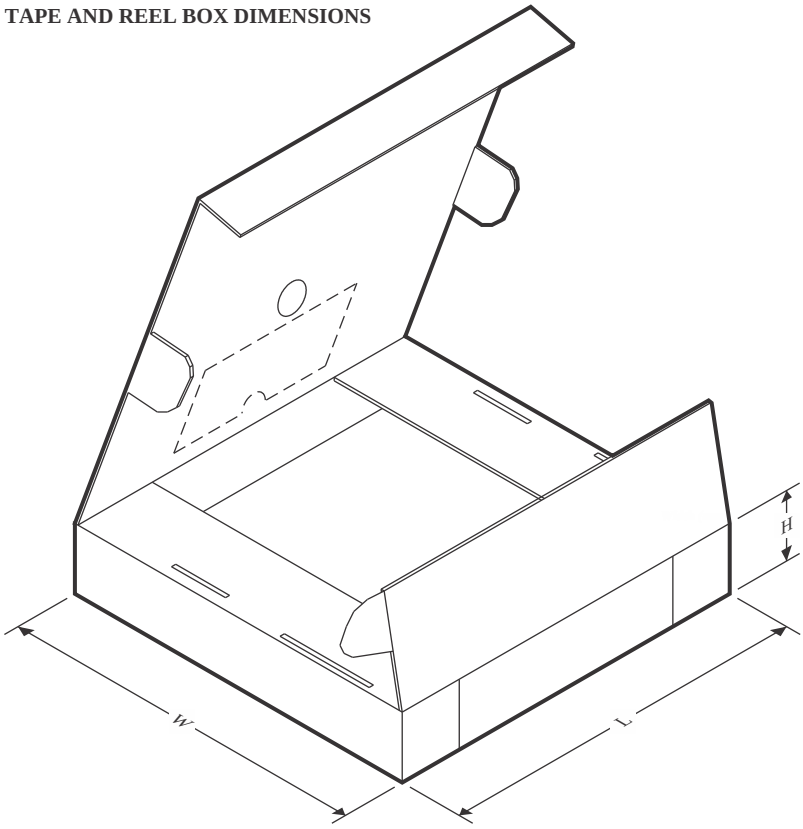
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS92074DDCR	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS92074DDCT	SOT-23-THIN	DDC	6	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS92074DR	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

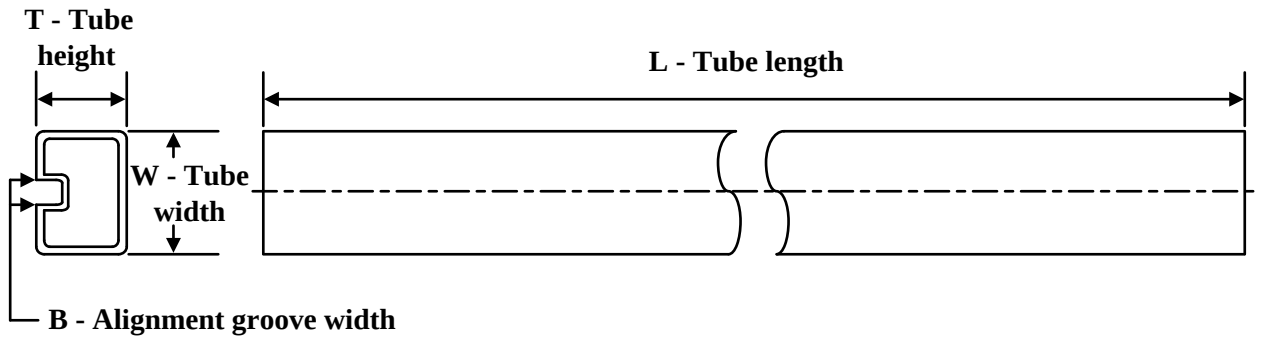
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

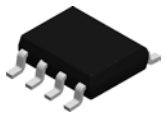
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS92074DDCR	SOT-23-THIN	DDC	6	3000	208.0	191.0	35.0
TPS92074DDCT	SOT-23-THIN	DDC	6	250	208.0	191.0	35.0
TPS92074DR	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS92074D	D	SOIC	8	95	495	8	4064	3.05

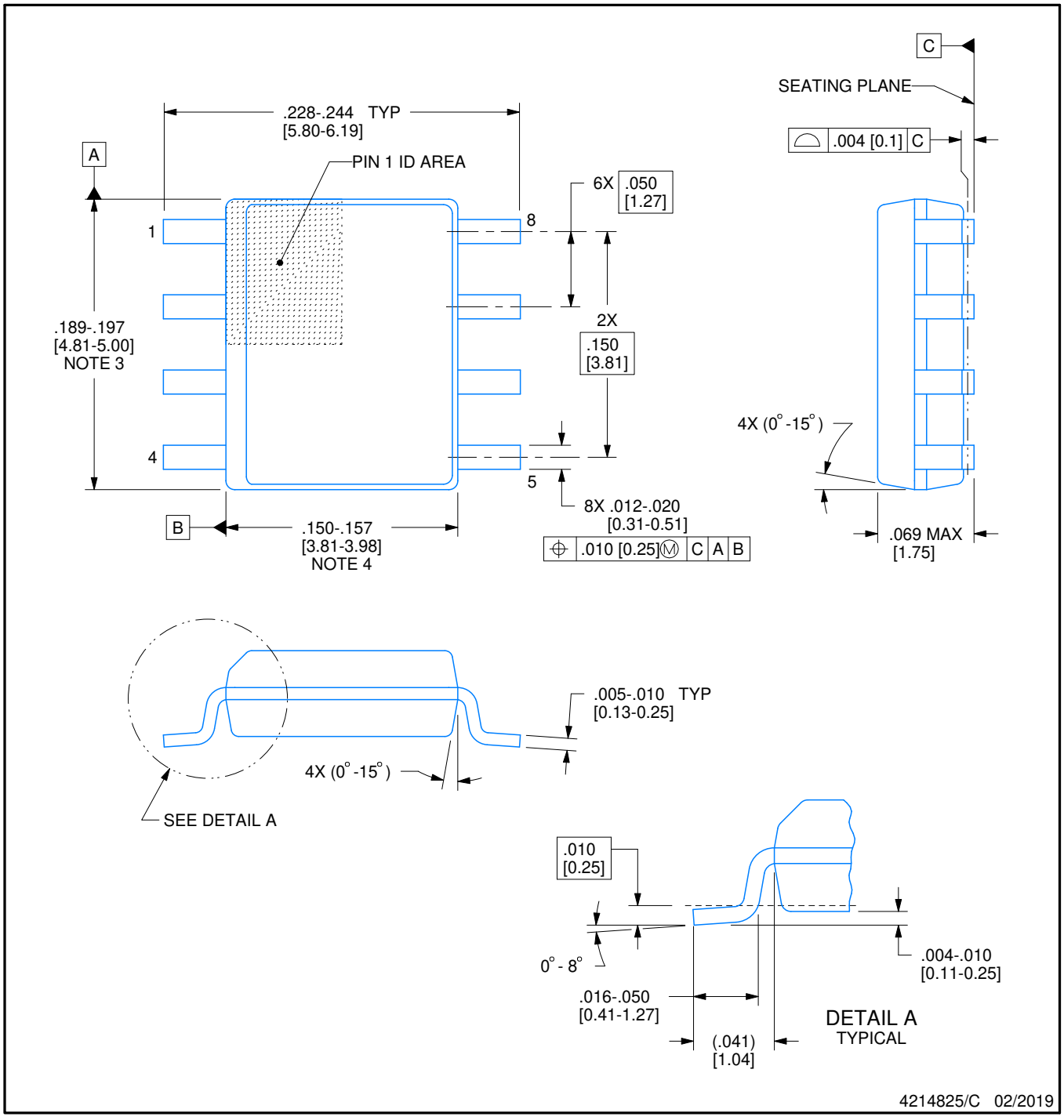


PACKAGE OUTLINE

D0008A

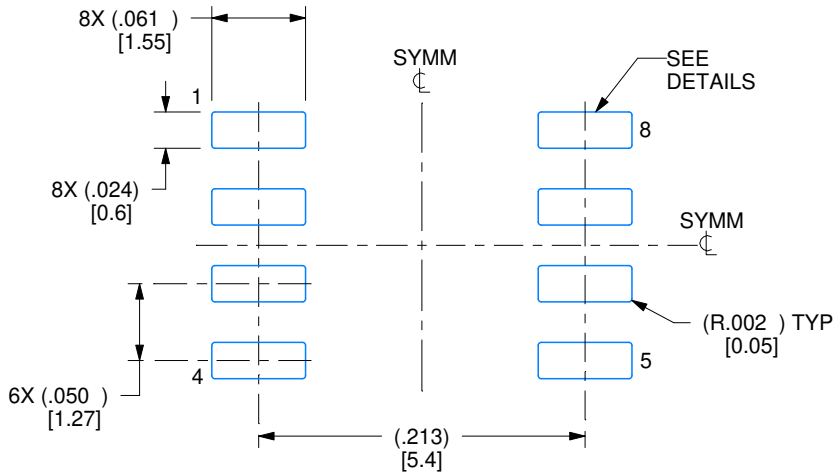
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

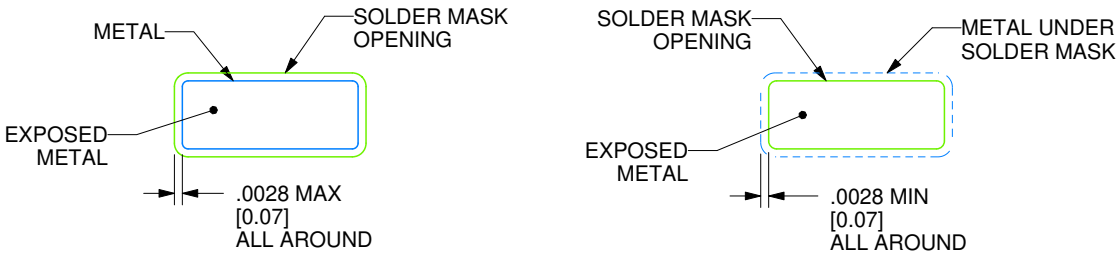


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

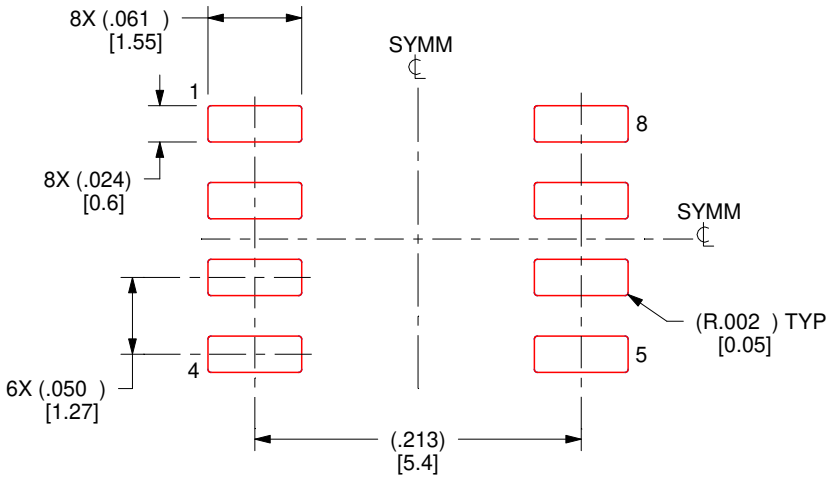
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

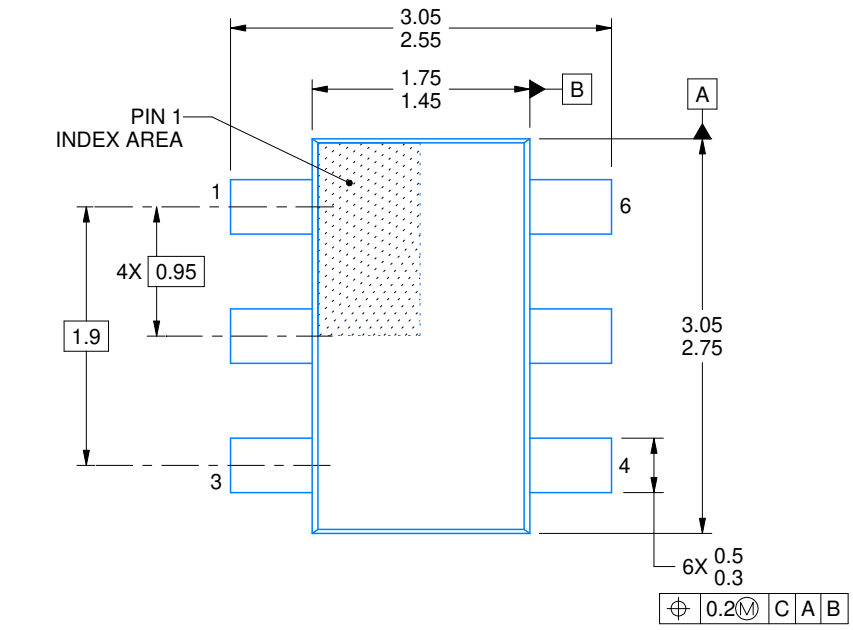
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

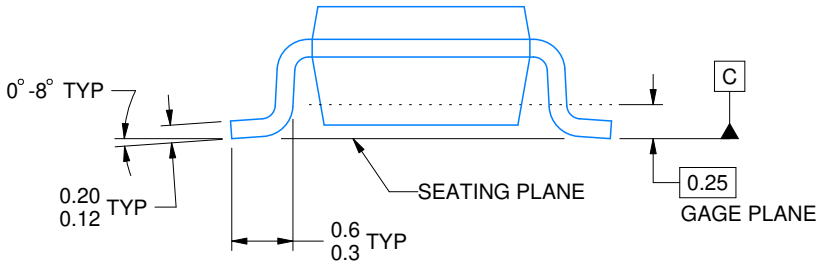
PACKAGE OUTLINE

DDC0006A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR

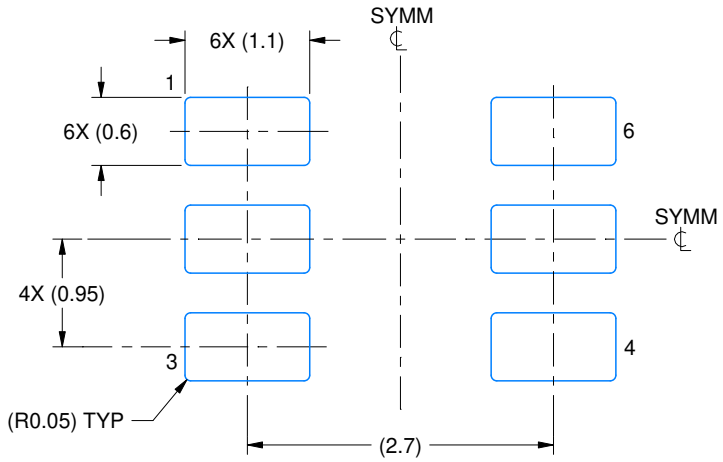




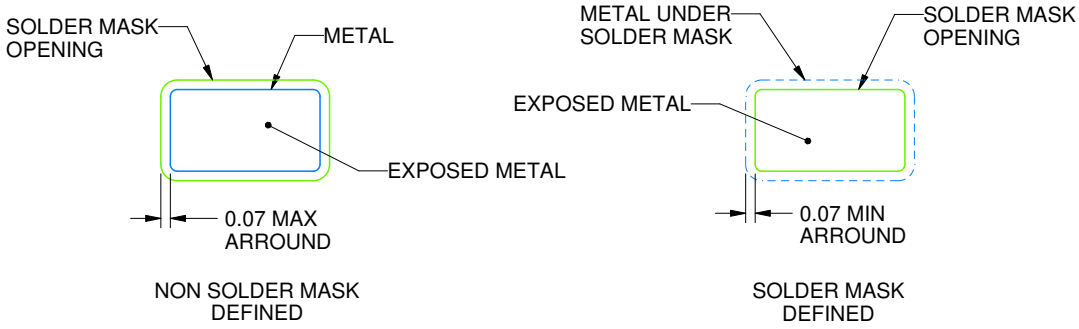
4214841/C 04/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X

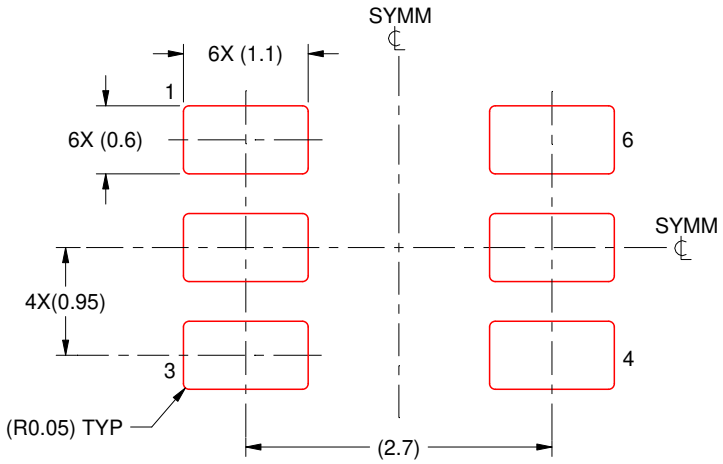


SOLDERMASK DETAILS

4214841/C 04/2022

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214841/C 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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