MIC2168A

1MHz PWM Synchronous Buck-Control IC

General Description

The MIC2168A is a high-efficiency, simple to use 1MHz PWM synchronous buck-control IC housed in a small MSOP-10 package. The MIC2168A allows compact DC/DC solutions with a minimal external component count and cost.

The MIC2168A operates from a 3V to 14.5V input, without the need of any additional bias voltage. The output voltage can be precisely regulated down to 0.8V. The adaptive all N-Channel MOSFET drive scheme allows efficiencies over 95% across a wide load range.

The MIC2168A senses current across the high-side N-Channel MOSFET, eliminating the need for an expensive and lossy current-sense resistor. Current limit accuracy is maintained by a positive temperature coefficient that tracks the increasing $R_{DS(ON)}$ of the external MOSFET. Further cost and space are saved by the internal in-rush-current limiting and digital soft-start.

The MIC2168A is identical to the MIC2168 with the exception that the MIC2168A increases the overcurrent blanking time from 80ns (typ.) to 120ns (typ.)

The MIC2168A is available in a 10-pin MSOP package, with a wide junction operating range of –40°C to +125°C.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

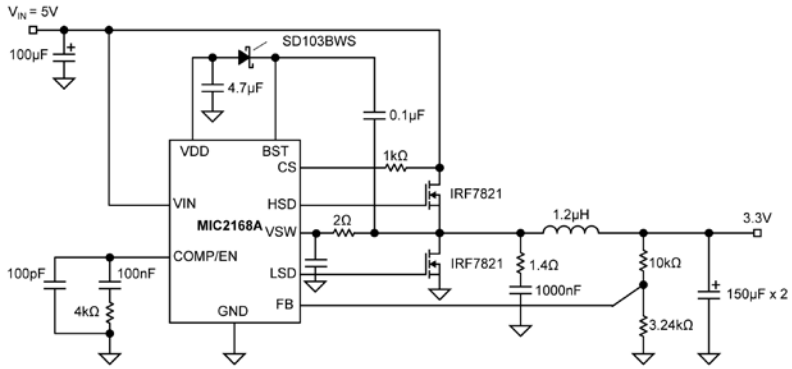
Features

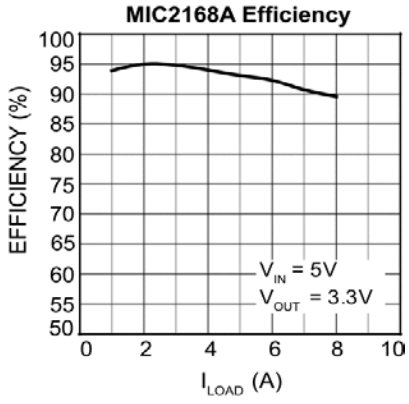
- 3V to 14.5V input voltage range
- Adjustable output voltage down to 0.8V
- Up to 95% efficiency
- 1MHz PWM operation
- Adjustable current-limit senses high-side N-Channel MOSFET current
- No external current sense resistor
- Adaptive gate drive increases efficiency
- Ultra-fast response with hysteretic transient recovery mode
- Overvoltage protection protects the load in fault conditions
- Dual mode current limit speeds up recovery time
- Hiccup mode short-circuit protection
- Internal soft-start
- Small-size MSOP 10-pin package

Applications

- Point-of-load DC/DC conversion
- Set-top boxes
- Graphic cards
- LCD power supplies
- Telecom power supplies
- Networking power supplies
- Cable modems and routers

Typical Application

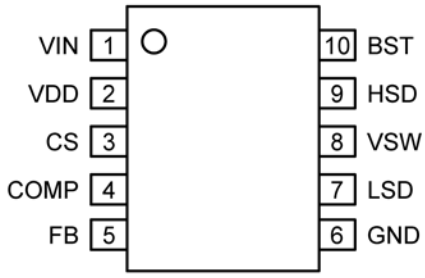




Ordering Information

Part Number	Frequency	Junction Temperature Range	Package
MIC2168AYMM	1MHz	–40° to +125°C	10-Pin MSOP Pb-Free

Pin Configuration



10-Pin MSOP (MM)
(Top View)

Pin Description

Pin Number	Pin Name	Pin Function
1	VIN	Supply Voltage (Input): 3V to 14.5V.
2	VDD	5V Internal Linear Regulator (Output): VDD is the external MOSFET gate drive supply voltage and an internal supply bus for the IC. When VIN is <5V, this regulator operates in dropout mode.
3	CS	Current Sense / Enable (Input): Current-limit comparator noninverting input. The current limit is sensed across the MOSFET during the ON time. The current can be set by the resistor in series with the CS pin.
4	COMP	Compensation (Input): Dual function pin. Pin for external compensation. If this pin is pulled below 0.2V, with the reference fully up, the device shuts down (50µA typical current draw).
5	FB	Feedback (Input): Input to error amplifier. Regulates error amplifier to 0.8V.
6	GND	Ground (Return).
7	LSD	Low-Side Drive (Output): High-current driver output for external synchronous MOSFET.
8	VSW	Switch (Return): High-side MOSFET driver return.
9	HSD	High-Side Drive (Output): High-current output-driver for the high-side MOSFET. When VIN is between 3.0V to 5V, 2.5V threshold-rated MOSFETs should be used. At VIN > 5V, 5V threshold MOSFETs should be used.
10	BST	Boost (Input): Provides the drive voltage for the high-side MOSFET driver. The gate-drive voltage is higher than the source voltage by VIN minus a diode drop.

Absolute Maximum Ratings[1]

Supply Voltage (V_{IN}) ..... +15.5V
Bootstrapped Voltage (V_{BST}) ..... V_{IN} +5V
Junction Temperature (T_J) ..... –40°C ≤ T_J ≤ +125°C
Storage Temperature (T_S) ..... –65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{IN}) ..... +3V to +14.5V
Output Voltage Range ..... 0.8V to V_{IN} × D_{MAX}
Package Thermal Resistance
10-Pin MSOP (θ_{JA}) ..... 180°C/W

Electrical Characteristics[3]

T_J = 25°C, V_{IN} = 5V, unless otherwise specified. Bold values indicate –40°C < T_J < +125°C.

Parameter	Condition	Min.	Typ.	Max.	Units
Feedback Voltage Reference	(± 1%)	0.792	0.8	0.808	V
Feedback Voltage Reference	(± 2% over temp)	**0.784**	0.8	**0.816**	V
Feedback Bias Current			30	**100**	nA
Output Voltage Line Regulation			0.03		%/V
Output Voltage Load Regulation			0.5		%
Output Voltage Total Regulation	3V ≤ V_{IN} ≤ 14.5V; 1A ≤ I_{OUT} ≤ 10A; (V_{OUT} = 2.5V)[4]		0.6		%
Oscillator Section					
Oscillator Frequency		900	1000	1100	kHz
Maximum Duty Cycle (D_{MAX})		90			
Minimum On-Time[4]			30	**60**	ns
Input and V_{DD} Supply					
PWM Mode Supply Current	V_{CS} = V_{IN} –0.25V; V_{FB} = 0.7V (output switching but excluding external MOSFET gate current.)		1.6	**3**	mA
Shutdown Quiescent Current	$V_{COMP/EN}$=0V		50	**150**	µA
VCOMP Shutdown Threshold		0.1	0.25	0.4	V
VCOMP Shutdown Blanking Period	C_{COMP} = 100nF		4		ms
Digital Supply Voltage (V_{DD})	V_{IN} ≥ 6V	4.7	5	5.3	V
Error Amplifier					
DC Gain			70		dB
Transconductance			1		ms
Soft Start					
Soft-Start Current	After timeout of internal timer. (See “Soft-Start” section.)		8.5		µA
Current Sense					
CS Overcurrent Trip Point	V_{CS} = V_{IN} –0.25V	160	200	240	µA
Temperature Coefficient			+1800		ppm/°C

Notes:

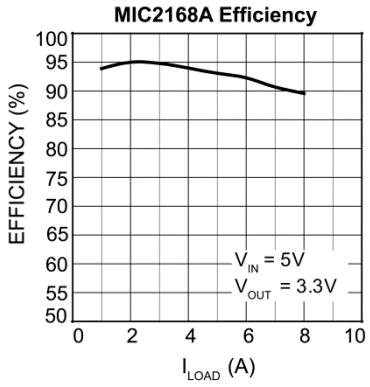
1. Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside of its operating ratings. The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(max)}$, the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown.
2. Devices are ESD sensitive, handling precautions required.
3. Specification for packaged product only.
4. Guaranteed by design.

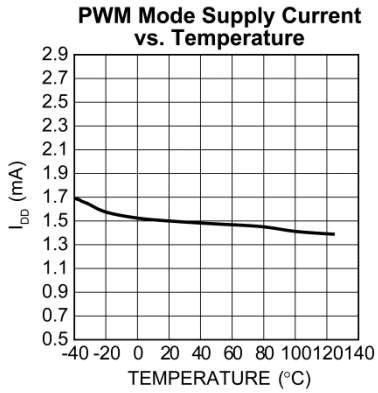
Electrical Characteristics (Continued)

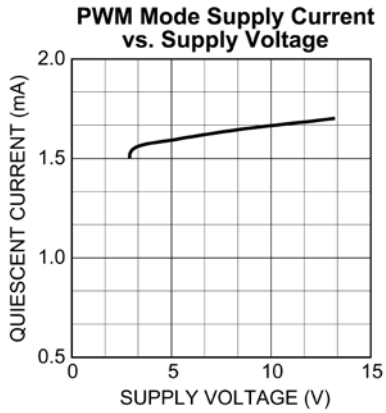
T_J = 25°C, V_{IN} = 5V, unless otherwise specified. **Bold** values indicate –40°C < T_J < +125°C.

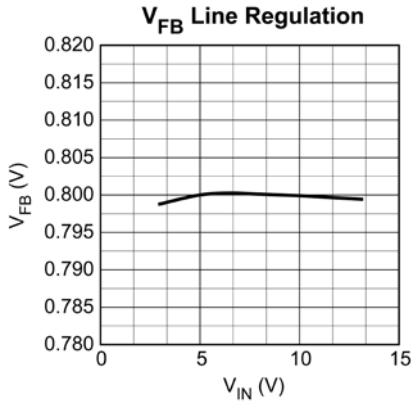
Parameter	Condition	Min.	Typ.	Max.	Units
Output Fault Correction Thresholds					
Upper Threshold, V_{FB_OVT}	(relative to V_{FB})		+3		%
Lower Threshold, V_{FB_UVT}	(relative to V_{FB})		-3		%
Gate Drivers					
Rise/Fall Time	Into 3000pF at V_{IN} > 5V		30		ns
Output Driver Impedance	Source, V_{IN} = 5V			6	Ω
	Sink, V_{IN} = 5V			6	Ω
	Source, V_{IN} = 3V			10	Ω
	Sink, V_{IN} = 3V			10	Ω
Driver Non-Overlap Time	Note 4	10	20		ns

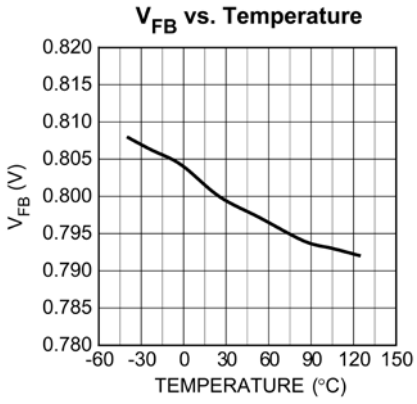
Typical Characteristics

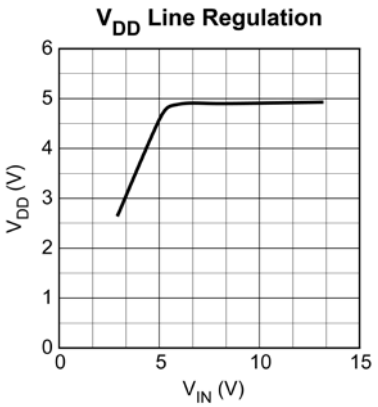


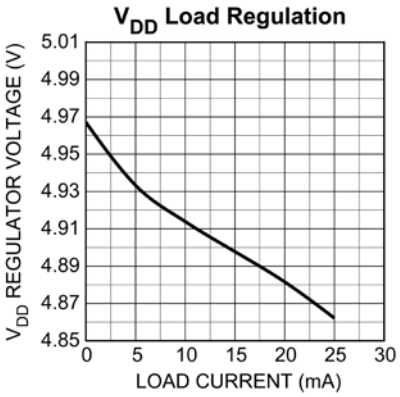


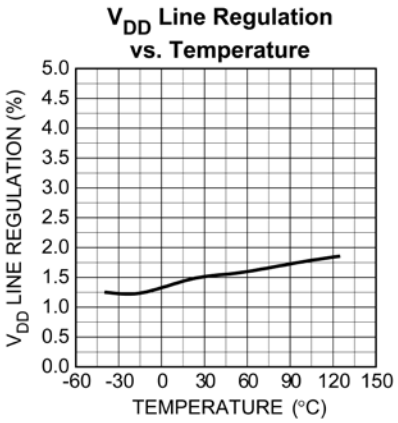


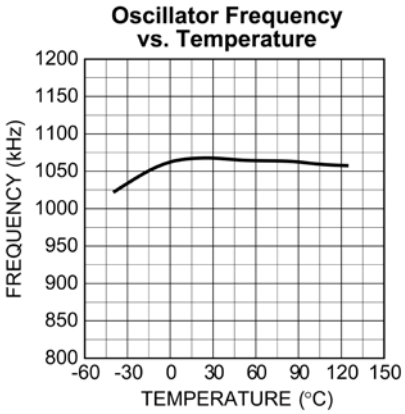




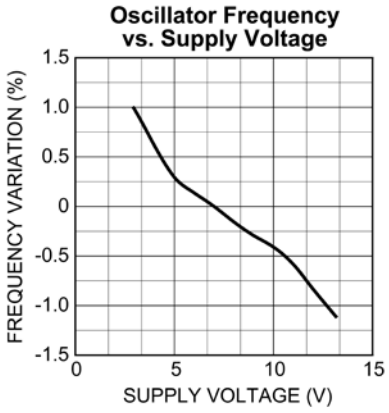


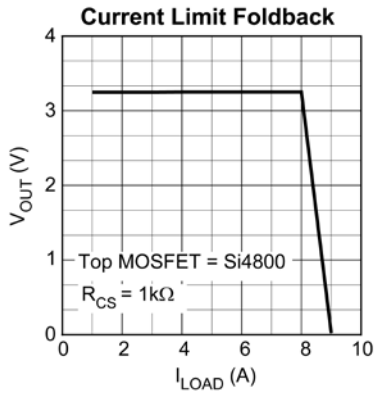


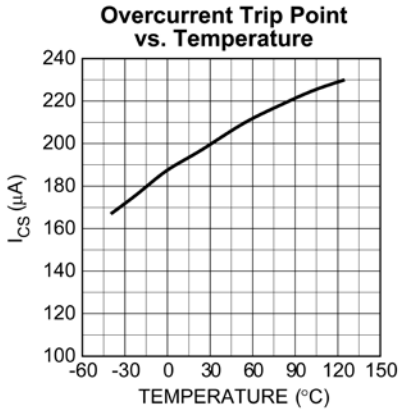




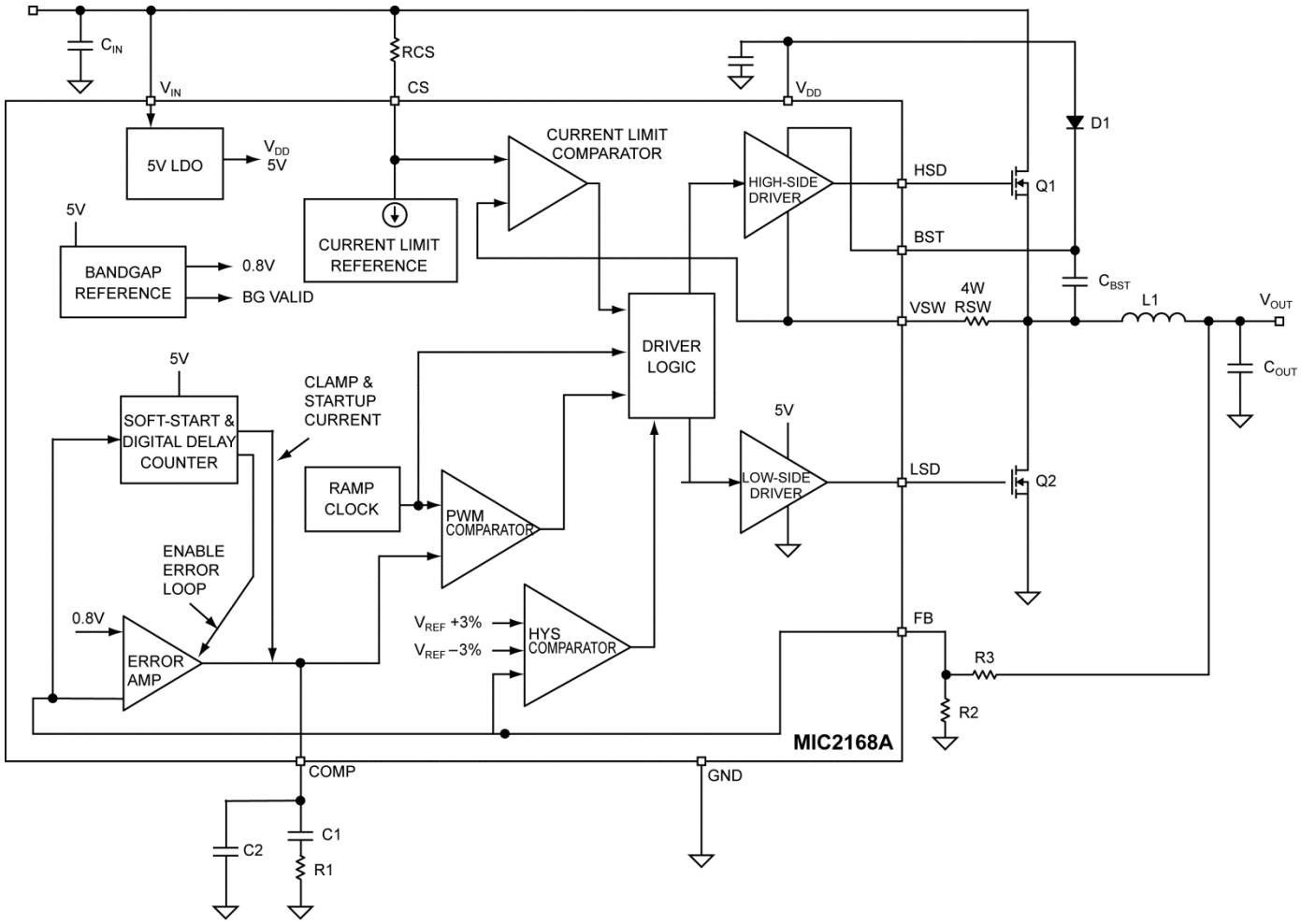
Typical Characteristics (Continued)







Functional Diagram



MIC2168A Block Diagram

Functional Description

The MIC2168A is a voltage mode, synchronous step-down switching regulator controller designed for high output power without the use of an external sense resistor. It includes an internal soft-start function which reduces the power supply input surge current at start-up by controlling the output voltage rise time, a PWM generator, a reference voltage, two MOSFET drivers, and short-circuit current limiting circuitry to form a complete 1MHz switching regulator.

Theory of Operation

The MIC2168A is a voltage mode step-down regulator. The block diagram illustrates the voltage control loop. The output voltage variation due to load or line changes will be sensed by the inverting input of the transconductance error amplifier via the feedback resistors R3, and R2 and compared to a reference voltage at the non-inverting input. This will cause a small change in the DC voltage level at the output of the error amplifier which is the input to the PWM comparator. The other input to the comparator is a 0 to 1V triangular waveform. The comparator generates a rectangular waveform whose width t_{ON} is equal to the time from the start of the clock cycle t0 until t_1, the time the triangle crosses the output waveform of the error amplifier. To illustrate the control loop, let us assume the output voltage drops due to sudden load turn-on, this would cause the inverting input of the error amplifier which is divided down version of V_{OUT} to be slightly less than the reference voltage causing the output voltage of the error amplifier to go high. This will cause the PWM comparator to increase t_{ON} time of the top side MOSFET, causing the output voltage to go up and bringing V_{OUT} back in regulation.

Soft-Start

The COMP pin on the MIC2168A is used for the following three functions:

1. Disables the part by grounding this pin
2. External compensation to stabilize the voltage control loop
3. Soft-start

For better understanding of the soft-start feature, let's assume VIN = 12V, and the MIC2168A is allowed to power-up. The COMP pin has an internal 8.5µA current source that charges the external compensation capacitor. As soon as this voltage rises to 180mV (t = Cap_COMP × 0.18V/8.5µA), the MIC2168A allows the internal VDD linear regulator to power up and as soon as it crosses the undervoltage lockout of 2.6V, the chip's internal oscillator starts switching. At this point in time, the COMP pin current source increases to 40µA and an internal 11-bit counter starts counting which takes approximately 2ms to complete. During counting, the COMP voltage is clamped at 0.65V. After this counting cycle the COMP current source is reduced to 8.5µA and the COMP pin voltage rises from 0.65V to 0.95V, the bottom edge of the saw-tooth oscillator. This is the beginning of 0% duty cycle and it increases slowly causing the output voltage to rise slowly. The MIC2168A has two hysteretic comparators that are enabled when VOUT is within ±3% of steady state. When the output voltage reaches 97% of programmed output voltage, then the gm error amplifier is enabled along with the hysteretic comparator. This point onwards, the voltage control loop (gm error amplifier) is fully in control and will regulate the output voltage.

Soft-start time can be calculated approximately by adding the following four time frames:

t1 = Cap_COMP × 0.18V/8.5µA

t2 = 12 bit counter, approx 2ms

t3 = Cap_COMP × 0.3V/8.5µA

$$t4\left(\frac{V_{OUT}}{V_{IN}}\right)\times 0.5\times\frac{Cap\_COMP}{8.5\mu.}$$

Soft-Start Time(Cap_COMP = 100nF) = t1 + t2 + t3 + t4 = 2.1ms + 2ms + 3.5ms + 1.8ms = 10ms

Current Limit

The MIC2168A uses the $R_{DS(ON)}$ of the top power MOSFET to measure output current. Since it uses the drain to source resistance of the power MOSFET, it is not very accurate. This scheme is adequate to protect the power supply and external components during a fault condition by cutting back the time the top MOSFET is on if the feedback voltage is greater than 0.67V. In case of a hard short when feedback voltage is less than 0.67V, the MIC2168A discharges the COMP capacitor to 0.65V, resets the digital counter and automatically shuts off the top gate drive, and the gm error amplifier and the –3% hysteretic comparators are completely disabled and the soft-start cycles restarts. This mode of operation is called the "hiccup mode" and its purpose is to protect the downstream load in case of a hard short. The circuit in Figure 1 illustrates the MIC2168A current limiting circuit.

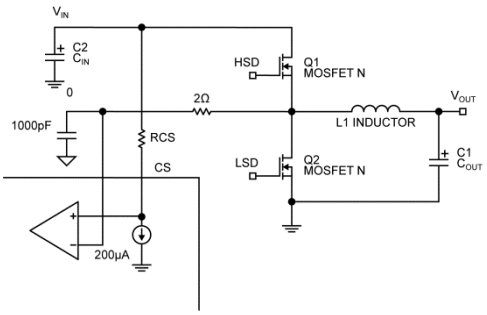


Figure 1. MIC2168A Current Limiting Circuit

The current limiting resistor R_{CS} is calculated by the following equation:

$$R_{CS} = \frac{R_{DS(ON)Q1} \times I_L}{200\mu A}$$

$$I_L = I_{LOAD} + \frac{1}{2} \times I_{PP}$$

where:

I_{PP} = Inductor Ripple Current =

$$\frac{V_{OUT}}{V_{IN}} \times \frac{V_{IN} - V_{OUT}}{F_{SWITCHING} \times L}$$

$F_{SWITCHING}$ = 1MHz

200µA is the internal sink current to program the MIC2168A current limit.

The MOSFET $R_{DS(ON)}$ varies 30% to 40% with temperature; therefore, it is recommended to add a 50% margin to the load current (I_{LOAD}) in the above equation to avoid false current limiting due to increased MOSFET junction temperature rise. It is also recommended to connect R_{CS} resistor directly to the drain of the top MOSFET Q1, and the R_{SW} resistor to the source of Q1 to accurately sense the MOSFETs $R_{DS(ON)}$. To make the MIC2168A insensitive to board layout and noise, a 1.4Ω resistor and a 1000pF capacitor is recommended below the switch node and ground. A 0.1µF capacitor in parallel with R_{CS} should be connected to filter some of the switching noise.

Internal V_{DD} Supply

The MIC2168A controller internally generates V_{DD} for self biasing and to provide power to the gate drives. This V_{DD} supply is generated through a low-dropout regulator and generates 5V from V_{IN} supply greater than 5V. For supply voltage less than 5V, the V_{DD} linear regulator is approximately 200mV in dropout. Therefore, it is recommended to short the V_{DD} supply to the input supply through a 10Ω resistor for input supplies between 2.9V to 5V.

MOSFET Gate Drive

The MIC2168A high-side drive circuit is designed to switch an N-Channel MOSFET. The Functional Diagram shows a bootstrap circuit, consisting of D1 and CBST, supplies energy to the high-side drive circuit. Capacitor CBST is charged while the low-side MOSFET is on and the voltage on the VSW pin is approximately 0V. When the high-side MOSFET driver is turned on, energy from CBST is used to turn the MOSFET on. As the MOSFET turns on, the voltage on the VSW pin increases to approximately V_{IN}. Diode D1 is reversed biased and CBST floats high while continuing to keep the high-side MOSFET on. When the low-side switch is turned back on, CBST is recharged through D1. The drive voltage is derived from the internal 5V V_{DD} bias supply. The nominal low-side gate drive voltage is 5V and the nominal high-side gate drive voltage is approximately 4.5V due the voltage drop across D1. An approximate 20ns delay between the high- and low-side driver transitions is used to prevent current from simultaneously flowing unimpeded through both MOSFETs.

MOSFET Selection

The MIC2168A controller works from input voltages of 3V to 13.2V and has an internal 5V regulator to provide power to turn the external N-Channel power MOSFETs for high- and low-side switches. For applications where V_{IN} < 5V, the internal V_{DD} regulator operates in dropout mode, and it is necessary that the power MOSFETs used are low threshold and are in full conduction mode for V_{GS} of 2.5V. For applications when V_{IN} > 5V; logic-level MOSFETs, whose operation is specified at V_{GS} = 4.5V must be used.

It is important to note the on-resistance of a MOSFET increases with increasing temperature. A 75°C rise in junction temperature will increase the channel resistance of the MOSFET by 50% to 75% of the resistance specified at 25°C. This change in resistance must be accounted for when calculating MOSFET power dissipation and in calculating the value of current-sense (CS) resistor.

Total gate charge is the charge required to turn the MOSFET on and off under specified operating conditions (V_{DS} and V_{GS}). The gate charge is supplied by the MIC2168A gate-drive circuit. At 1MHz switching frequency and above, the gate charge can be a significant source of power dissipation in the MIC2168A. At low output load, this power dissipation is noticeable as a reduction in efficiency.

The average current required to drive the high-side MOSFET is:

$$I_{G[high-side](avg)} = Q_G \times f_S$$

where:

$I_{G[high-side](avg)}$ = average high-side MOSFET gate current.

Q_G = total gate charge for the high-side MOSFET taken from manufacturer's data sheet for V_{GS} = 5V.

The low-side MOSFET is turned on and off at V_{DS} = 0 because the freewheeling diode is conducting during this time. The switching loss for the low-side MOSFET is usually negligible. Also, the gate-drive current for the low-side MOSFET is more accurately calculated using CISS at V_{DS} = 0 instead of gate charge.

For the low-side MOSFET:

$$I_{G[low-side](avg)} = C_{ISS} \times V_{GS} \times f_S$$

Since the current from the gate drive comes from the input voltage, the power dissipated in the MIC2168A due to gate drive is:

$$P_{GATEDRIVE} = V_{IN}\left(I_{G[high-side](avg)} + I_{G[low-side](avg)}\right)$$

A convenient figure of merit for switching MOSFETs is the on resistance times the total gate charge $R_{DS(ON)} \times Q_G$. Lower numbers translate into higher efficiency. Low gate-charge logic-level MOSFETs are a good choice for use with the MIC2168A.

Parameters that are important to MOSFET switch selection are:

- Voltage rating
- On-resistance
- Total gate charge

The voltage ratings for the top and bottom MOSFET are essentially equal to the input voltage. A safety factor of 20% should be added to the V_{DS}(max) of the MOSFETs to account for voltage spikes due to circuit parasitics.

The power dissipated in the switching transistor is the sum of the conduction losses during the on-time ($P_{CONDUCTION}$) and the switching losses that occur during the period of time when the MOSFETs turn on and off (P_{AC}).

$$P_{SW} = P_{CONDUCTION} + P_{AC}$$

where:

$$P_{CONDUCTION} = I_{SW(rms)}^{2} \times R_{SW}$$

$$P_{AC} = P_{AC(off)} + P_{AC(on)}$$

$$R_{SW} = \text{on-resistance of the MOSFET switch}$$

$$D = \text{duty cycle} = \left(\frac{V_{OUT}}{V_{IN}}\right)$$

Making the assumption the turn-on and turn-off transition times are equal; the transition times can be approximated by:

$$t_T = \frac{C_{ISS} \times V_{GS} + C_{OSS} \times V_{IN}}{I_G}$$

where:

C_{ISS} and C_{OSS} are measured at V_{DS} = 0

I_G = gate-drive current (1A for the MIC2168A)

The total high-side MOSFET switching loss is:

$$P_{AC} = (V_{IN} + V_D) \times I_{PK} \times t_T \times f_S$$

where:

t_T = switching transition time (typically 20ns to 50ns)

V_D = freewheeling diode drop, typically 0.5V

f_S it the switching frequency, nominally 1MHz

The low-side MOSFET switching losses are negligible and can be ignored for these calculations.

Inductor Selection

Values for inductance, peak, and RMS currents are required to select the output inductor. The input and output voltages and the inductance value determine the peak-to-peak inductor ripple current. Generally, higher inductance values are used with higher input voltages. Larger peak-to-peak ripple currents will increase the power dissipation in the inductor and MOSFETs. Larger output ripple currents will also require more output capacitance to smooth out the larger ripple current. Smaller peak-to-peak ripple currents require a larger inductance value and therefore a larger and more expensive inductor. A good compromise between size, loss and cost is to set the inductor ripple current to be equal to 20% of the maximum output current. The inductance value is calculated by:

$$L = \frac{V_{OUT} \times (V_{IN}(max) - V_{OUT})}{V_{IN}(max) \times f_S \times 0.2 \times I_{OUT}(max)}$$

where:

f_S = switching frequency, 1MHz

0.2 = ratio of AC ripple current to DC output current

V_{IN}(max) = maximum input voltage

The peak-to-peak inductor current (AC ripple current) is:

$$I_{PP} = \frac{V_{OUT} \times (V_{IN}(max) - V_{OUT})}{V_{IN}(max) \times f_S \times L}$$

The peak inductor current is equal to the average output current plus one half of the peak-to-peak inductor ripple current.

$$I_{PK} = I_{OUT}(max) + 0.5 \times I_{PP}$$

The RMS inductor current is used to calculate the I2 × R losses in the inductor.

$$I_{INDUCTOR}(rms) = I_{OUT}(max) \times \sqrt{1 + \frac{1}{3}\left(\frac{I_P}{I_{OUT}(max)}\right)^2}$$

Maximizing efficiency requires the proper selection of core material and minimizing the winding resistance. The high frequency operation of the MIC2168A requires the use of ferrite materials for all but the most cost sensitive applications. Lower cost iron powder cores may be used but the increase in core loss will reduce the efficiency of the power supply. This is especially noticeable at low output power. The winding resistance decreases efficiency at the higher output current levels. The winding resistance must be minimized although this usually comes at the expense of a larger inductor. The power dissipated in the inductor is equal to the sum of the core and copper losses. At higher output loads, the core losses are usually insignificant and can be ignored. At lower output currents, the core losses can be a significant contributor. Core loss information is usually available from the magnetics vendor. Copper loss in the inductor is calculated by the equation below:

$$P_{INDUCTOR}\ Cu = I_{INDUCTOR}(rms)^2 \times R_{WINDING}$$

The resistance of the copper wire, $R_{WINDING}$, increases with temperature. The value of the winding resistance used should be at the operating temperature.

$$R_{WINDING(hot)} = R_{WINDING(20°C)} \times (1 + 0.0042 \times (T_{HOT} - T_{20°C}))$$

where:

T_{HOT} = temperature of the wire under operating load
$T_{20°C}$ = ambient temperature

$R_{WINDING(20°C)}$ is room temperature winding resistance (usually specified by the manufacturer)

Output Capacitor Selection

The output capacitor values are usually determined capacitors ESR (equivalent series resistance). Voltage and RMS current capability are two other important factors selecting the output capacitor. Recommended capacitors are tantalum, low-ESR aluminum electrolytics, and POSCAPS. The output capacitor's ESR is usually the main cause of output ripple. The output capacitor ESR also affects the overall voltage feedback loop from stability point of view. See "Feedback Loop Compensation" section for more information.

The maximum value of ESR is calculated:

$$R_{ESR} \leq \frac{\Delta V_{OUT}}{I_{PP}}$$

where:

V_{OUT} = peak-to-peak output voltage ripple

I_{PP} = peak-to-peak inductor ripple current

The total output ripple is a combination of the ESR output capacitance. The total ripple is calculated below:

$$\Delta V_{OUT} = \sqrt{\left(\frac{I_{PP} \times (1-D)}{C_{OUT} \times f_S}\right)^2 + (I_{PP} \times R_{ESR})^2}$$

where:

D = duty cycle

C_{OUT} = output capacitance value

f_S = switching frequency

The voltage rating of capacitor should be twice the voltage for a tantalum and 20% greater for an aluminum electrolytic. The output capacitor RMS current is calculated below:

$$I_{C_{OUT(rms)}} = \frac{I_{PP}}{\sqrt{12}}$$

The power dissipated in the output capacitor is:

$$P_{DISS(C_{OUT})} = I_{C_{OUT(rms)}}{}^2 \times R_{ESR(C_{OUT})}$$

Input Capacitor Selection

The input capacitor should be selected for ripple current rating and voltage rating. Tantalum input capacitors may fail when subjected to high inrush currents, caused by turning the input supply on. Tantalum input capacitor voltage rating should be at least 2 times the maximum input voltage to maximize reliability. Aluminum electrolytic, OS-CON, and multilayer polymer film capacitors can handle the higher inrush currents without voltage derating. The input voltage ripple will primarily depend on the input capacitor's ESR.

The peak input current is equal to the peak inductor current, so:

$$\Delta V_{IN} = I_{INDUCTOR(peak)} \times R_{ESR(C_{IN})}$$

The input capacitor must be rated for the input current ripple. The RMS value of input capacitor current is determined at the maximum output current. Assuming the peak-to-peak inductor ripple current is low:

$$I_{C_{IN}}(rms) \approx I_{OUT}(max) \times \sqrt{D \times (1-D)}$$

The power dissipated in the input capacitor is:

$$P_{DISS(C_{IN})} = I_{C_{IN}}(rms)^2 \times R_{ESR(C_{IN})}$$

Voltage Setting Components

The MIC2168A requires two resistors to set the output voltage as shown in Figure 2.

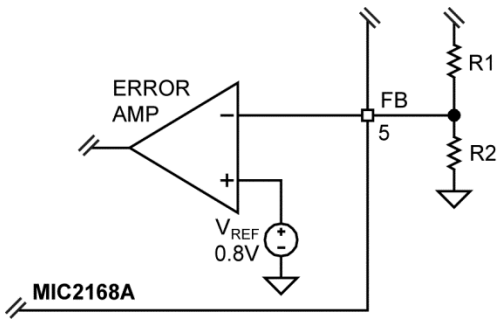


Figure 2. Voltage-Divider Configuration

where:

V_{REF} for the MIC2168A is typically 0.8V

The output voltage is determined by the equation:

$$V_O = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

A typical value of R1 can be between 3kΩ and 10kΩ. If R1 is too large, it may allow noise to be introduced into the voltage feedback loop. If R1 is too small, in value, it will decrease the efficiency of the power supply, especially at light loads. Once R1 is selected, R2 can be calculated using:

$$R2 = \frac{V_{REF} \times R1}{V_O - V_{REF}}$$

External Schottky Diode

An external freewheeling diode is used to keep the inductor current flow continuous while both MOSFETs are turned off. This dead time prevents current from flowing unimpeded through both MOSFETs and is typically 15ns. The diode conducts twice during each switching cycle. Although the average current through this diode is small, the diode must be able to handle the peak current.

The reverse voltage requirement of the diode is:

$$V_{DIODE(rms)} = V_{IN}$$

The power dissipated by the Schottky diode is:

$$P_{DIODE} = I_{D(avg)} \times V_F$$

where:

V_F = forward voltage at the peak diode current

The external Schottky diode, D1, is not necessary for circuit operation since the low-side MOSFET contains a parasitic body diode. The external diode will improve efficiency and decrease high frequency noise. If the MOSFET body diode is used, it must be rated to handle the peak and average current. The body diode has a relatively slow reverse recovery time and a relatively high forward voltage drop. The power lost in the diode is proportional to the forward voltage drop of the diode. As the high-side MOSFET starts to turn on, the body diode becomes a short circuit for the reverse recovery period, dissipating additional power. The diode recovery and the circuit inductance will cause ringing during the high-side MOSFET turn-on. An external Schottky diode conducts at a lower forward voltage preventing the body diode in the MOSFET from turning on. The lower forward voltage drop dissipates less power than the body diode. The lack of a reverse recovery mechanism in a Schottky diode causes less ringing and less power loss. Depending on the circuit components and operating conditions, an external Schottky diode will give a $^1/_2$% to 1% improvement in efficiency.

Feedback Loop Compensation

The MIC2168A controller comes with an internal transconductance error amplifier used for compensating the voltage feedback loop by placing a capacitor (C1) in series with a resistor (R1) and another capacitor C2 in parallel from the COMP pin to ground. See "Functional Diagram."

Power Stage

The power stage of a voltage mode controller has an inductor, L1, with its winding resistance (DCR) connected to the output capacitor, C_{OUT}, with its electrical series resistance (ESR) as shown in Figure 3.

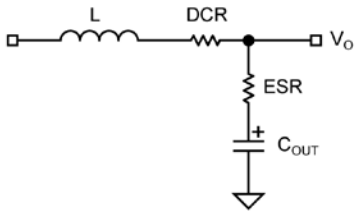


Figure 3. The Output LC Filter in a Voltage-Mode Buck Converter

The transfer function G(s), for such a system is:

$$G_{(S)} - \left(\frac{(1 + ESR \times s \times C}{DCR \times s \times C + s^2 \times L \times C + 1 + ESR \times s \times C} \right)$$

Plotting this transfer function with the following assumed values (L = 2µH, DCR = 0.009Ω, C_{OUT} = 1000µF, ESR = 0.025Ω) gives lot of insight as to why one needs to compensate the loop by adding resistor and capacitors on the COMP pin. Figures 4 and 5 show the gain curve and phase curve for the above transfer function.

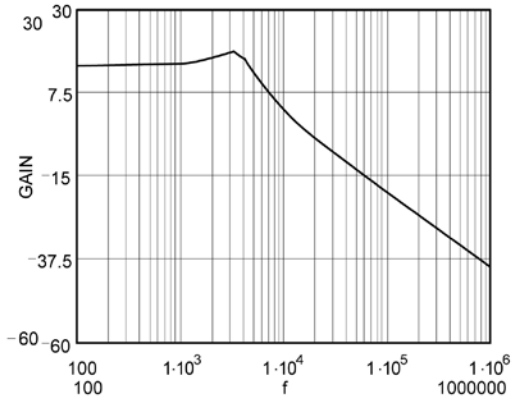


Figure 4. The Gain Curve for G(s)

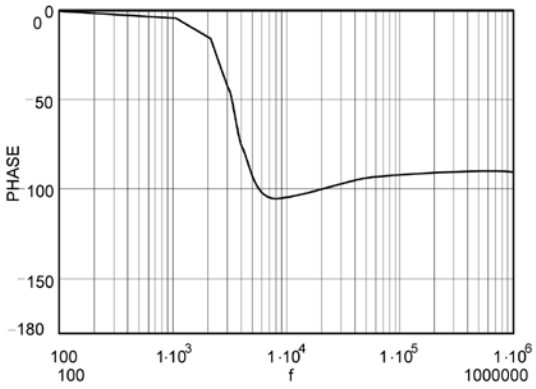


Figure 5. Phase Curve for G(s)

It can be seen from the transfer function G(s) and the gain curve that the output inductor and capacitor create a two pole system with a break frequency at:

$$f_C = \frac{1}{2 \times \pi \sqrt{L \times C_{OUT}}}$$

Therefore, f_{LC} = 3.6kHz.
By looking at the phase curve, it can be seen that the output capacitor ESR (0.050Ω) cancels one of the two poles (LCOUT) system by introducing a zero at:

$$f_{ZERO} = \frac{1}{2 \times \pi \times ESR \times C_{OUT}}$$

Therefore, F_{ZERO} = 6.36kHz.

From the point of view of compensating the voltage loop, it is recommended to use higher ESR output capacitors since they provide a 90° phase gain in the power path. For comparison purposes, Figure 6, shows the same phase curve with an ESR value of 0.002Ω.

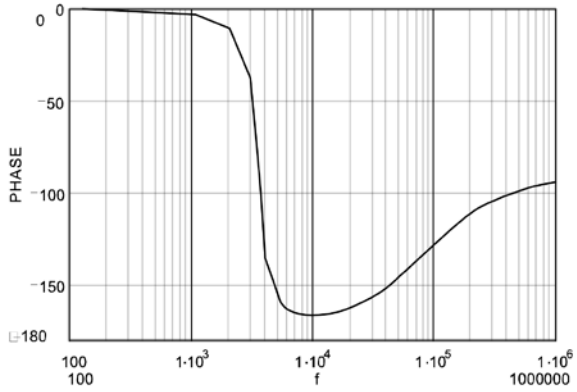


Figure 6. The Phase Curve with ESR = 0.002Ω

It can be seen from Figure 5 that at 50kHz, the phase is approximately –90° versus Figure 6 where the number is –150°. This means that the transconductance error amplifier has to provide a phase boost of about 45° to achieve a closed loop phase margin of 45° at a crossover frequency of 50kHz for Figure 4, versus 105° for Figure 6. The simple RC and C2 compensation scheme allows a maximum error amplifier phase boost of about 90°. Therefore, it is easier to stabilize the MIC2168A voltage control loop by using high ESR value output capacitors.

g_m Error Amplifier

It is undesirable to have high error amplifier gain at high frequencies because high-frequency noise spikes would be picked up and transmitted at large amplitude to the output, thus, gain should be permitted to fall off at high frequencies. At low frequency, it is desired to have high open-loop gain to attenuate the power line ripple. Thus, the error amplifier gain should be allowed to increase rapidly at low frequencies.

The transfer function with R1, C1, and C2 for the internal g_m error amplifier can be approximated by the following equation:

$$\text{Error Amplifier}(s) = g_m \times \left[\frac{1 + R1 \times S \times C1}{s \times (C1 + C2)\left(1 + R1 \times \frac{C1 \times C2 \times S}{C1 + C2}\right)} \right]$$

The above equation can be simplified by assuming C2<<C1,

$$\text{Error Amplifier}(s) = g_m \times \left(\frac{1 + R1 \times S \times C1}{s \times (C1)(1 + R1 \times C2 \times S)} \right)$$

From the above transfer function, one can see that R1 and C1 introduce a zero and R1 and C2 a pole at the following frequencies:

$$F_{ZERO} = \frac{1}{2 \times \pi \times R1 \times C1}$$

$$F_{POLE} = \frac{1}{2 \times \pi \times C2 \times R1}$$

$$F_{POLE}\ @\text{origin} = \frac{1}{2 \times \pi \times C1}$$

Figures 7 and 8 show the gain and phase curves for the above transfer function with R1 = 9.3k, C1 = 1000pF, C2 = 100pF, and gm = .005Ω^{-1}. It can be seen that at 50kHz, the error amplifier exhibits approximately 45° of phase margin.

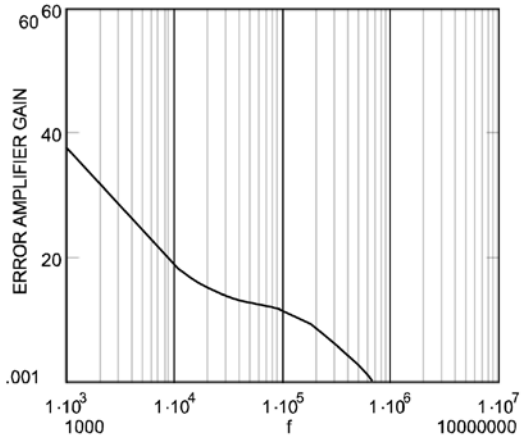


Figure 7. Error Amplifier Gain Curve

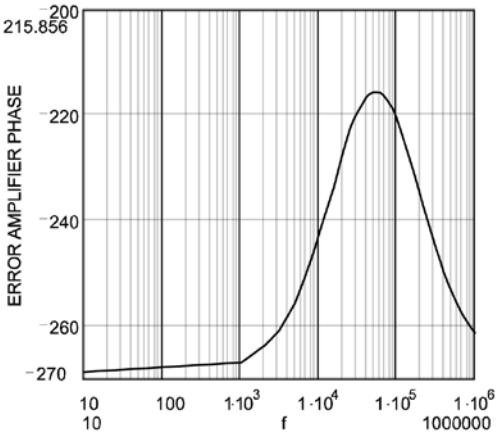


Figure 8. Error Amplifier Phase Curve

Total Open-Loop Response

The open-loop response for the MIC2168A controller is easily obtained by adding the power path and the error amplifier gains together, since they already are in Log scale. It is desirable to have the gain curve intersect zero dB at tens of kilohertz, this is commonly called crossover frequency; the phase margin at crossover frequency should be at least 45°. Phase margins of 30° or less cause the power supply to have substantial ringing when subjected to transients, and have little tolerance for component or environmental variations. Figure 9 and Figure 10 show the open-loop gain and phase margin. It can be seen from Figure 9 that the gain curve intersects the 0dB at approximately 50kHz, and from Figure 10 that at 50kHz, the phase shows approximately 50° of margin.

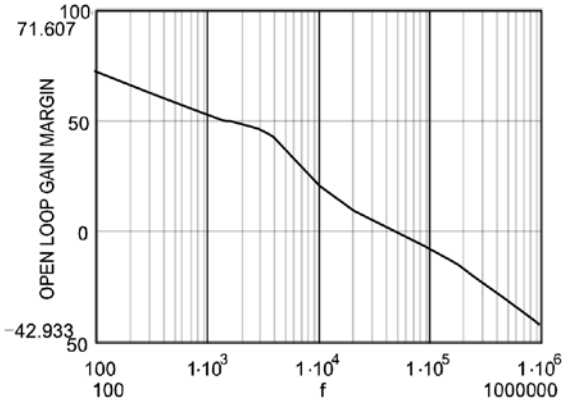


Figure 9. Open-Loop Gain Margin

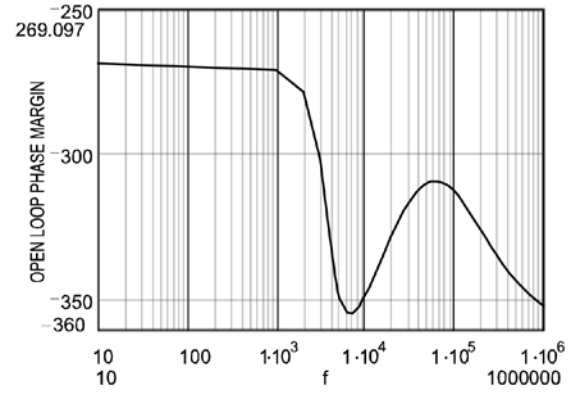


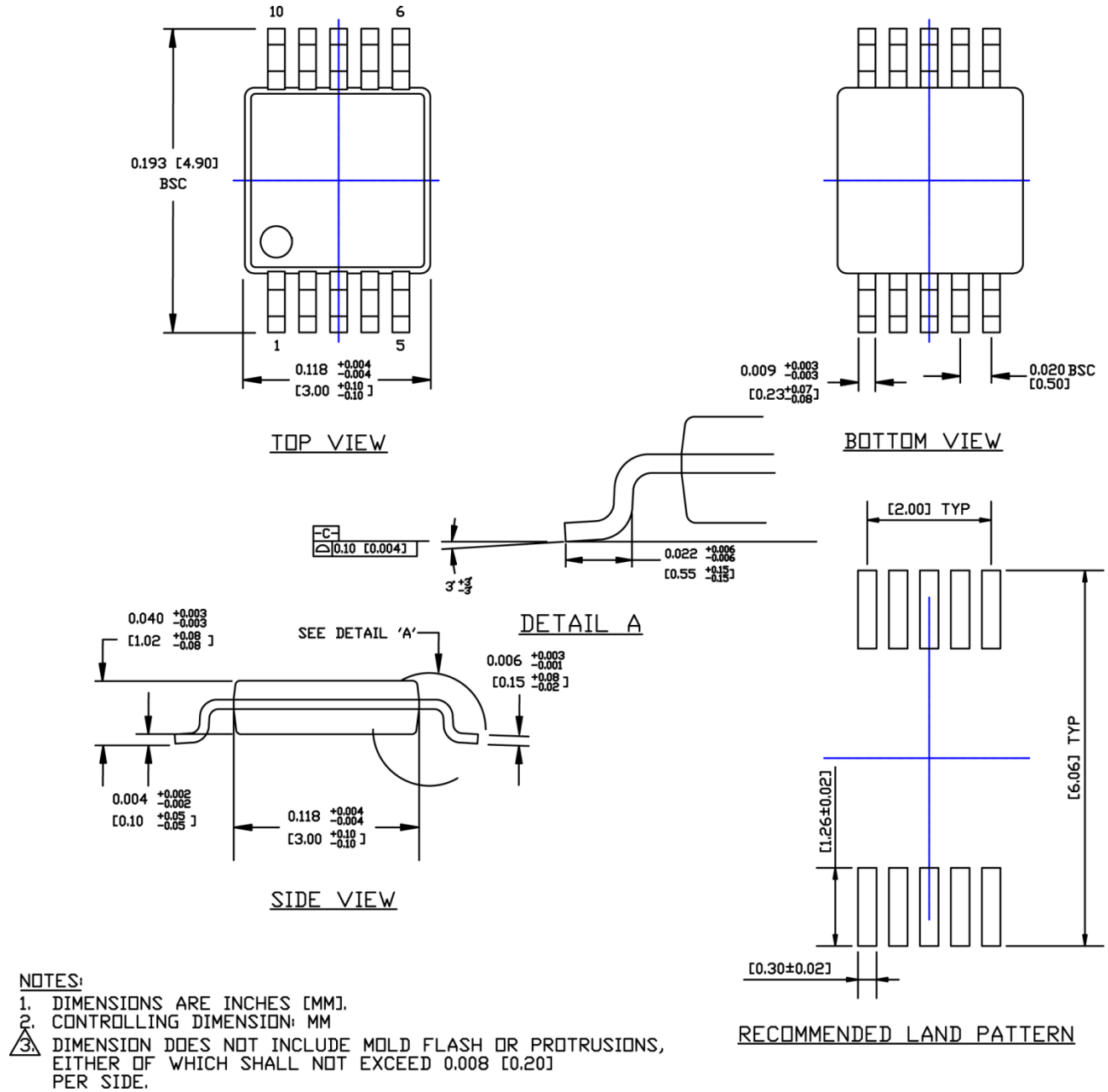
Figure 10. Open-Loop Phase Margin

Design Example

Layout and Checklist:

1. Connect the current limiting (CS) resistor directly to the drain of top MOSFET Q1.
2. Use a 10Ω resistor from the input supply to the V_{IN} pin on the MIC2168A. Also, place a 1µF ceramic capacitor from this pin to GND not through via.
3. The feedback resistors R1 and R2 should be placed close to the FB pin. The top side of R1 should connect directly to the output node. Run this trace away from the switch node (junction of Q1, Q2, and L1). The bottom side of R1 should connect to the GND pin on the MIC2168A.
4. The compensation resistor and capacitors should be placed right next to the COMP pin and the other side should connect directly to the GND pin on the MIC2168A rather than going to the plane.
5. Add a snubber circuit (resistor and a capacitor) from the switch node to GND. A good starting point is 1000pF and 1.4Ω.
6. Add a place holder for a gate resistor on the top MOSFET gate drive. A gate resistors of 10Ω or less should be used. No gate resistor should be used on the low side MOSFET.
7. Low gate charge MOSFETs should be used to maximize efficiency, such as Si4800, Si4804BDY, IRF7821, IRF8910, FDS6680A, and FDS6912A to mention a few.
8. Add a 1Ω to 4Ω resistor from the SW pin on the MIC2168A to the switch node on the circuit (junction of MOSFETs and inductor).
9. Compensation component GND, feedback resistor ground, chip ground, 1µF V_{IN} ceramic capacitor ground, and 10µF V_{DD} capacitor ground should all run together and connect to the output capacitor ground. See demo board layout, top layer.
10. The 10µF ceramic input capacitor should be placed between the drain of top MOSFET and source of bottom MOSFET.
11. The 10µF ceramic capacitor should be placed right on the V_{DD} pin without any vias.
12. 12. The source of the bottom MOSFET should connect directly to the input capacitor GND with a thick trace. The output capacitor and the input capacitor should connect directly to the GND plane.
13. 13. Place a 0.1µF ceramic capacitor in parallel with the CS resistor to filter any switching noise.

Package Information



NOTES:
1. DIMENSIONS ARE INCHES [MM].
2. CONTROLLING DIMENSION: MM
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008 [0.20] PER SIDE.

10-Pin MSOP (MM)

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