



**AOI452A**

**N-Channel SDMOS™ Power Transistor**

**General Description**

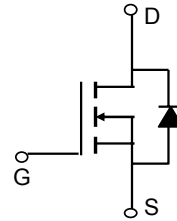
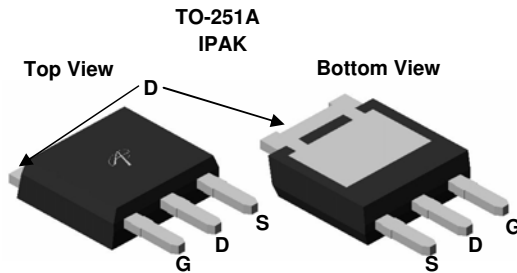
The AOI452A is fabricated with SDMOS™ trench technology that combines excellent  $R_{DS(ON)}$  with low gate charge. The result is outstanding efficiency with controlled switching behavior. This universal technology is well suited for PWM, load switching and general purpose applications.

- RoHS Compliant
- Halogen Free

**Features**

$V_{DS}$  (V) =25V  
 $I_D$  = 55A ( $V_{GS}$  = 10V)  
 $R_{DS(ON)}$  < 7.3m $\Omega$  ( $V_{GS}$  = 10V)  
 $R_{DS(ON)}$  < 14m $\Omega$  ( $V_{GS}$  = 4.5V)

**100% UIS Tested!**  
**100%  $R_g$  Tested!**



**Absolute Maximum Ratings  $T_A=25^\circ\text{C}$  unless otherwise noted**

| Parameter   | Symbol         | Maximum                 | Units            |
|---|----------------|-------------------------|------------------|
| Drain-Source Voltage                                      | $V_{DS}$       | 25                      | V                |
| Gate-Source Voltage                                       | $V_{GS}$       | $\pm 20$                | V                |
| Continuous Drain Current <sup>G</sup>                     | $I_D$          | $T_C=25^\circ\text{C}$  | A                |
|   |                | $T_C=100^\circ\text{C}$ |                  |
| Pulsed Drain Current <sup>C</sup>                         | $I_{DM}$       | 120                     |                  |
| Continuous Drain Current                                  | $I_{DSM}$      | $T_A=25^\circ\text{C}$  | A                |
|   |                | $T_A=70^\circ\text{C}$  | 13               |
| Avalanche Current <sup>C</sup>                            | $I_{AR}$       | 27                      | A                |
| Repetitive avalanche energy $L=0.1\text{mH}$ <sup>C</sup> | $E_{AR}$       | 36                      | mJ               |
| Power Dissipation <sup>B</sup>                            | $P_D$          | $T_C=25^\circ\text{C}$  | W                |
|   |                | $T_C=100^\circ\text{C}$ |                  |
| Power Dissipation <sup>A</sup>                            | $P_{DSM}$      | $T_A=25^\circ\text{C}$  | W                |
|   |                | $T_A=70^\circ\text{C}$  |                  |
| Junction and Storage Temperature Range                    | $T_J, T_{STG}$ | -55 to 175              | $^\circ\text{C}$ |

**Thermal Characteristics**

| Parameter                                  | Symbol          | Typ                 | Max  | Units                     |
|--|-----------------|---------------------|------|---------------------------|
| Maximum Junction-to-Ambient <sup>A</sup>   | $R_{\theta JA}$ | $t \leq 10\text{s}$ | 14.2 | $^\circ\text{C}/\text{W}$ |
| Maximum Junction-to-Ambient <sup>A D</sup> |                 | Steady-State        | 39   | $^\circ\text{C}/\text{W}$ |
| Maximum Junction-to-Case                   | $R_{\theta JC}$ | 2.5                 | 3    | $^\circ\text{C}/\text{W}$ |

Electrical Characteristics ( $T_J=25^\circ\text{C}$  unless otherwise noted)

| Symbol                      | Parameter                             | Conditions  | Min | Typ    | Max         | Units            |
|-----------------------------|---------------------------------------|---|-----|--------|-------------|------------------|
| <b>STATIC PARAMETERS</b>    |                                       |   |     |        |             |                  |
| $BV_{DSS}$                  | Drain-Source Breakdown Voltage        | $I_D=250\mu\text{A}$ , $V_{GS}=0\text{V}$   | 25  |        |             | V                |
| $I_{DSS}$                   | Zero Gate Voltage Drain Current       | $V_{DS}=25\text{V}$ , $V_{GS}=0\text{V}$<br>$T_J=55^\circ\text{C}$                    |     |        | 10<br>50    | $\mu\text{A}$    |
| $I_{GSS}$                   | Gate-Body leakage current             | $V_{DS}=0\text{V}$ , $V_{GS}=\pm 20\text{V}$  |     |        | 100         | nA               |
| $V_{GS(th)}$                | Gate Threshold Voltage                | $V_{DS}=V_{GS}$ , $I_D=250\mu\text{A}$  | 1.5 | 2      | 2.5         | V                |
| $I_{D(ON)}$                 | On state drain current                | $V_{GS}=10\text{V}$ , $V_{DS}=5\text{V}$  | 120 |        |             | A                |
| $R_{DS(ON)}$                | Static Drain-Source On-Resistance     | $V_{GS}=10\text{V}$ , $I_D=20\text{A}$<br>$T_J=125^\circ\text{C}$                     |     | 6<br>9 | 7.3<br>10.8 | $\text{m}\Omega$ |
|                             |                                       | $V_{GS}=4.5\text{V}$ , $I_D=20\text{A}$   |     | 11.1   | 14          | $\text{m}\Omega$ |
| $g_{FS}$                    | Forward Transconductance              | $V_{DS}=5\text{V}$ , $I_D=20\text{A}$   |     | 50     |             | S                |
| $V_{SD}$                    | Diode Forward Voltage                 | $I_S=1\text{A}$ , $V_{GS}=0\text{V}$  |     | 0.7    | 1           | V                |
| $I_S$                       | Maximum Body-Diode Continuous Current |   |     |        | 55          | A                |
| <b>DYNAMIC PARAMETERS</b>   |                                       |   |     |        |             |                  |
| $C_{iss}$                   | Input Capacitance                     |   | 990 | 1180   | 1450        | pF               |
| $C_{oss}$                   | Output Capacitance                    | $V_{GS}=0\text{V}$ , $V_{DS}=12.5\text{V}$ , $f=1\text{MHz}$                          | 210 | 275    | 350         | pF               |
| $C_{rss}$                   | Reverse Transfer Capacitance          |   | 125 | 175    | 245         | pF               |
| $R_g$                       | Gate resistance                       | $V_{GS}=0\text{V}$ , $V_{DS}=0\text{V}$ , $f=1\text{MHz}$                             | 1.1 | 1.7    | 2.5         | $\Omega$         |
| <b>SWITCHING PARAMETERS</b> |                                       |   |     |        |             |                  |
| $Q_g(10\text{V})$           | Total Gate Charge                     | $V_{GS}=10\text{V}$ , $V_{DS}=12.5\text{V}$ , $I_D=20\text{A}$                        | 17  | 21.7   | 26          | nC               |
| $Q_g(4.5\text{V})$          | Total Gate Charge                     |   | 35  | 11     | 13          | nC               |
| $Q_{gs}$                    | Gate Source Charge                    |   | 3   | 4      | 5           | nC               |
| $Q_{gd}$                    | Gate Drain Charge                     |   | 4   | 6.4    | 9           | nC               |
| $t_{D(on)}$                 | Turn-On Delay Time                    | $V_{GS}=10\text{V}$ , $V_{DS}=12.5\text{V}$ , $R_L=0.42\Omega$ ,<br>$R_{GEN}=3\Omega$ |     | 6.8    |             | ns               |
| $t_r$                       | Turn-On Rise Time                     |   |     | 13.8   |             | ns               |
| $t_{D(off)}$                | Turn-Off Delay Time                   |   |     | 21.5   |             | ns               |
| $t_f$                       | Turn-Off Fall Time                    |   |     | 8.7    |             | ns               |
| $t_{rr}$                    | Body Diode Reverse Recovery Time      | $I_F=20\text{A}$ , $dI/dt=500\text{A}/\mu\text{s}$                                    | 8.5 | 10.6   | 13          | ns               |
| $Q_{rr}$                    | Body Diode Reverse Recovery Charge    | $I_F=20\text{A}$ , $dI/dt=500\text{A}/\mu\text{s}$                                    | 13  | 16     | 20          | nC               |

A. The value of  $R_{\theta JA}$  is measured with the device mounted on  $1\text{in}^2$  FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ . The Power dissipation  $P_{DSM}$  is based on  $R_{\theta JA}$  and the maximum allowed junction temperature of  $150^\circ\text{C}$ . The value in any given application depends on the user's specific board design, and the maximum temperature of  $175^\circ\text{C}$  may be used if the PCB allows it.

B. The power dissipation  $P_D$  is based on  $T_{J(MAX)}=175^\circ\text{C}$ , using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature  $T_{J(MAX)}=175^\circ\text{C}$ . Ratings are based on low frequency and duty cycles to keep initial  $T_J=25^\circ\text{C}$ .

D. The  $R_{\theta JA}$  is the sum of the thermal impedance from junction to case  $R_{\theta JC}$  and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using  $<300\mu\text{s}$  pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of  $T_{J(MAX)}=175^\circ\text{C}$ . The SOA curve provides a single pulse rating.

G. The maximum current rating is limited by bond-wires.

H. These tests are performed with the device mounted on  $1\text{in}^2$  FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ .

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

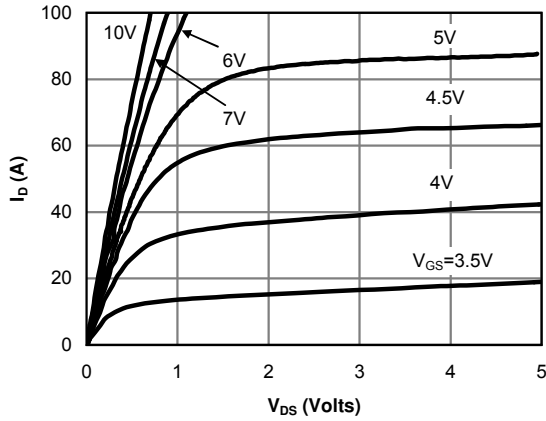


Fig 1: On-Region Characteristics (Note E)

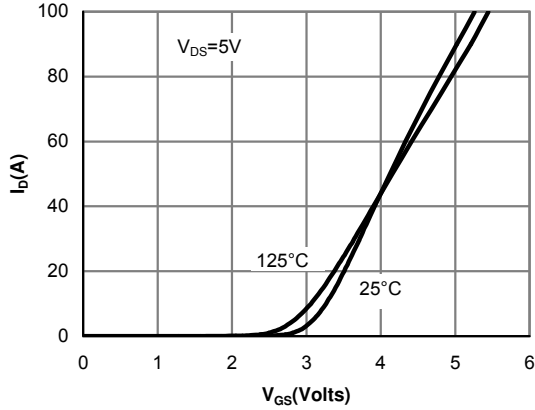


Figure 2: Transfer Characteristics (Note E)

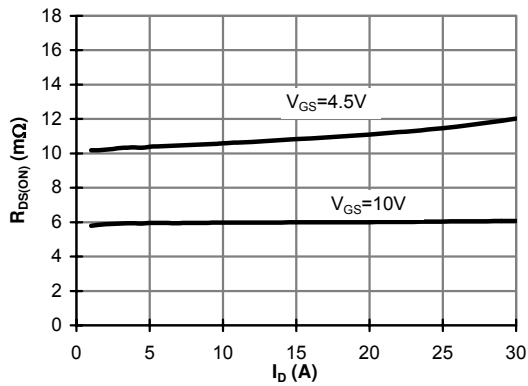


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

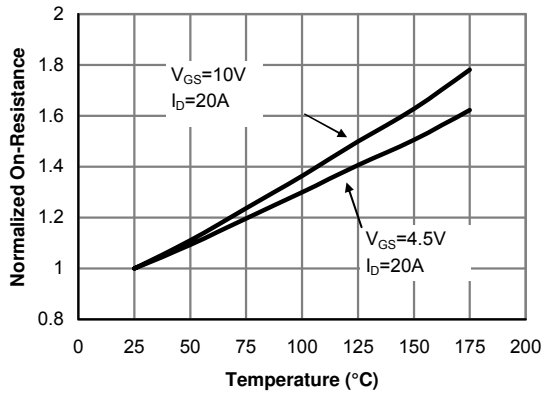


Figure 4: On-Resistance vs. Junction Temperature (Note E)

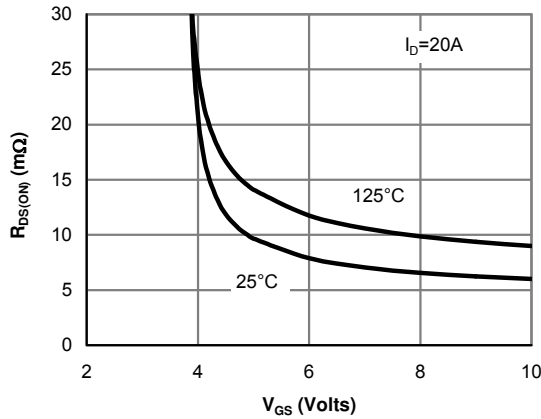


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

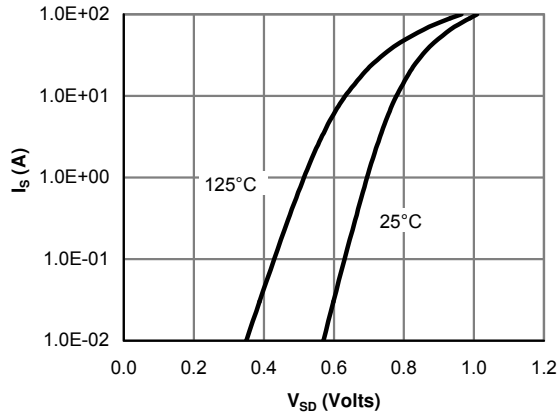


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

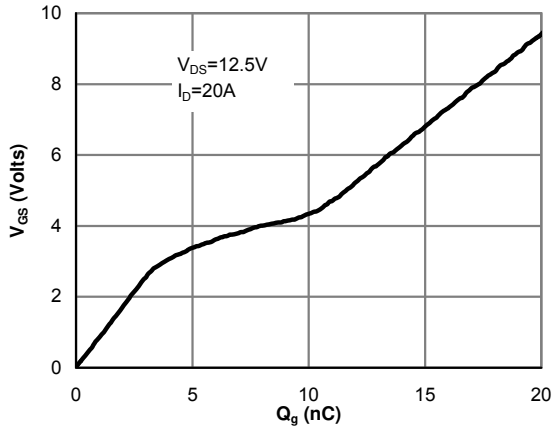


Figure 7: Gate-Charge Characteristics

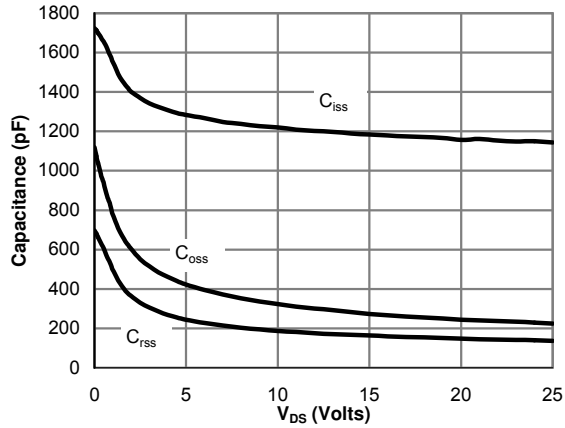


Figure 8: Capacitance Characteristics

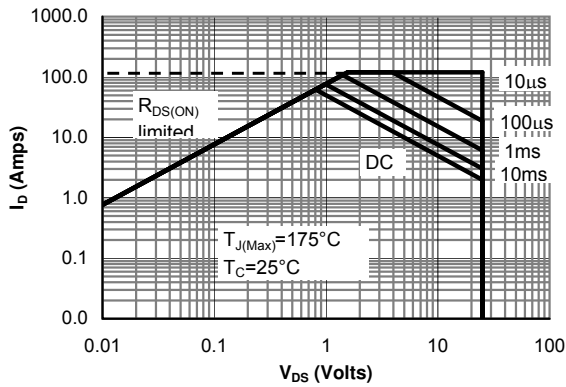


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

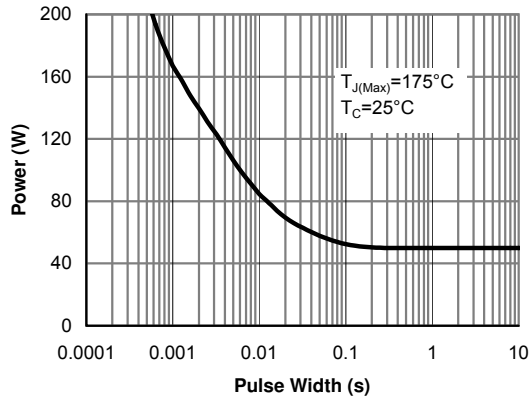


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

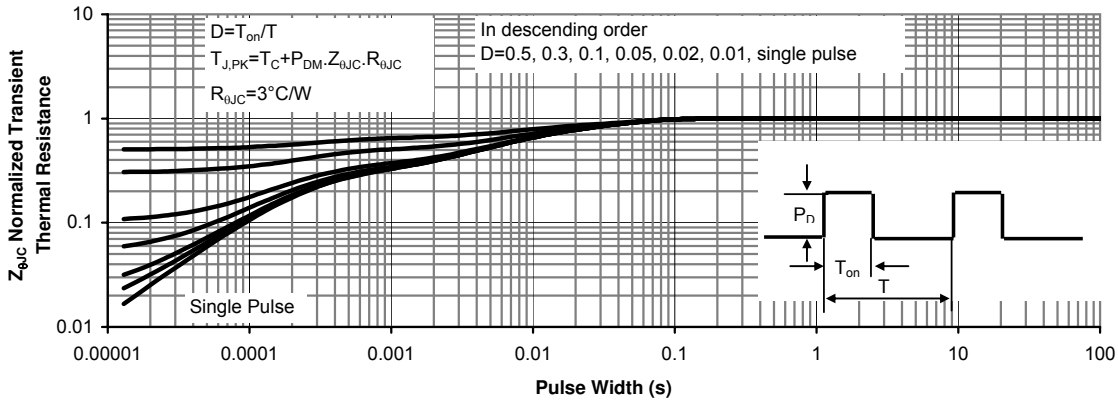


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

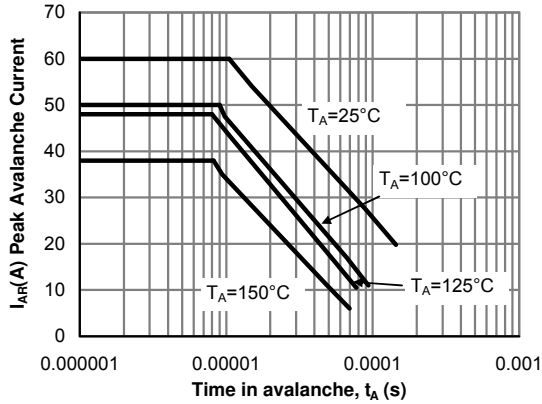


Figure 12: Single Pulse Avalanche capability (Note C)

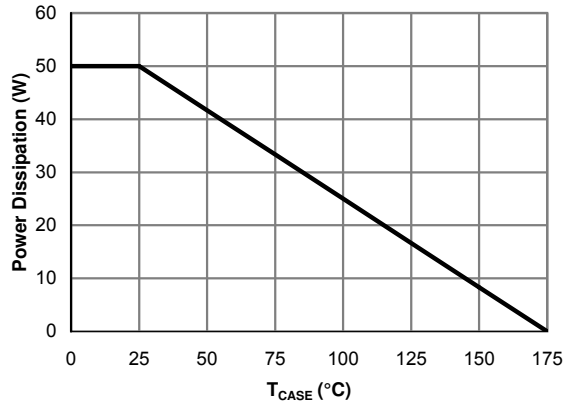


Figure 13: Power De-rating (Note F)

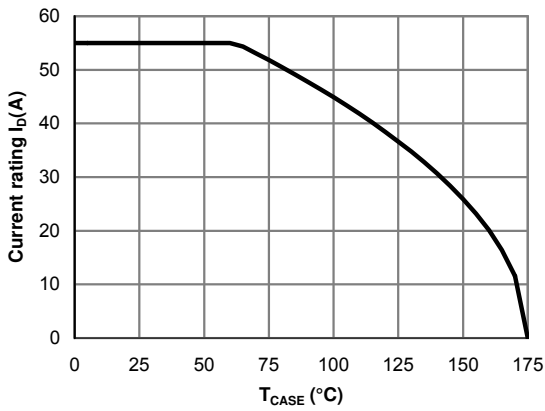


Figure 14: Current De-rating (Note F)

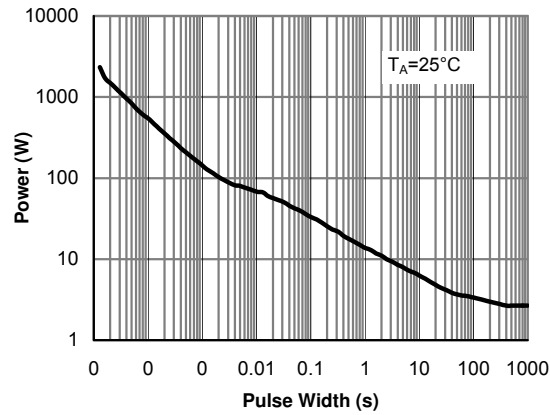


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

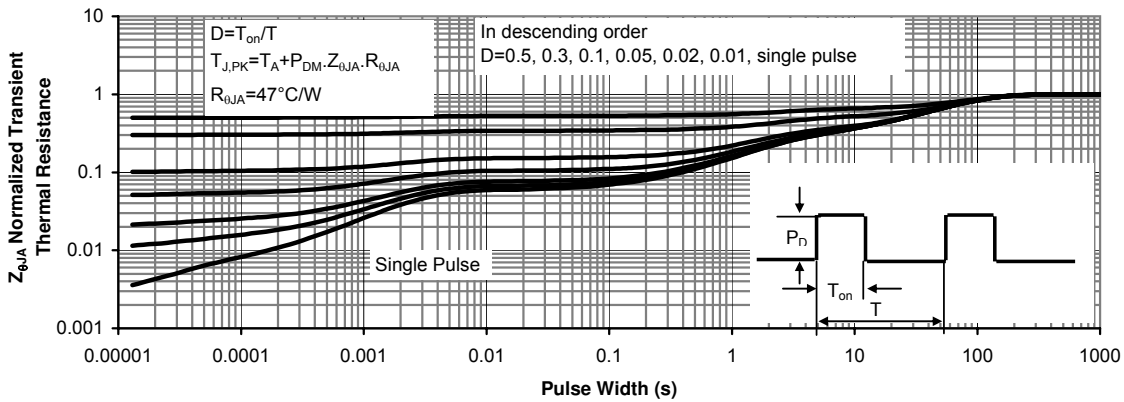


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

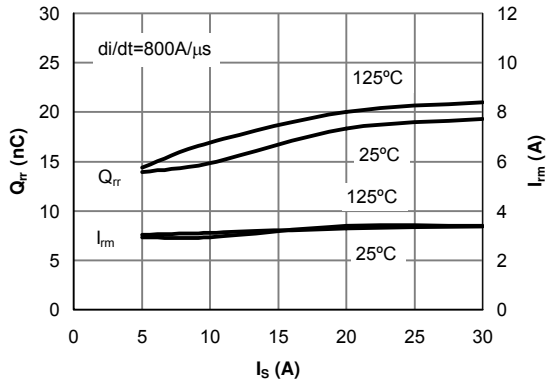


Figure 17: Diode Reverse Recovery Charge and Peak Current vs. Conduction Current

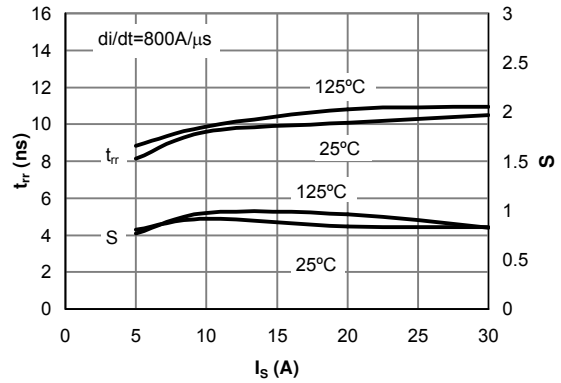


Figure 18: Diode Reverse Recovery Time and Softness Factor vs. Conduction Current

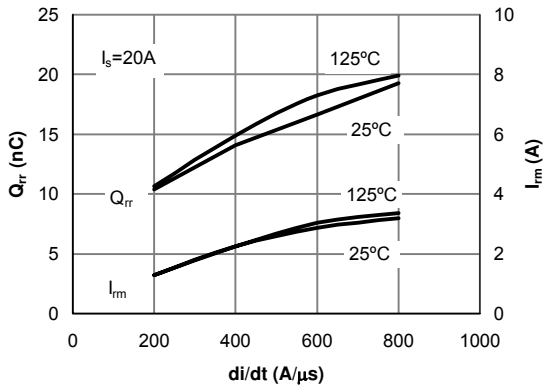


Figure 19: Diode Reverse Recovery Charge and Peak Current vs. di/dt

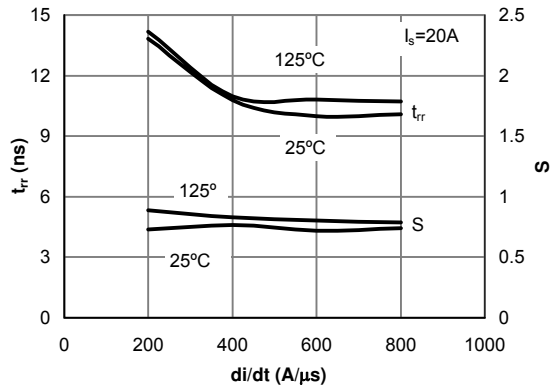
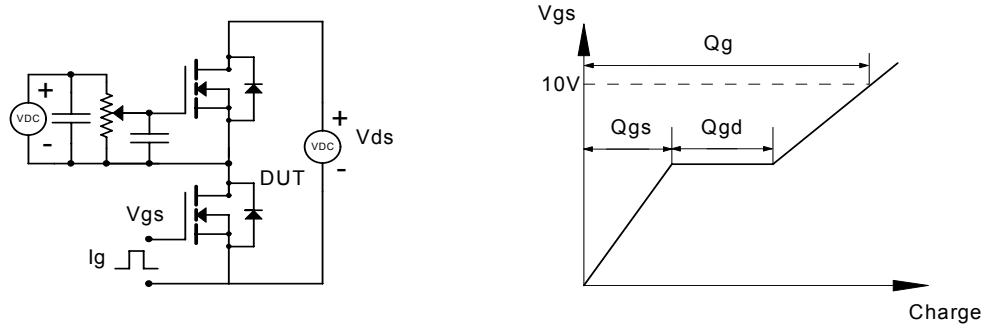
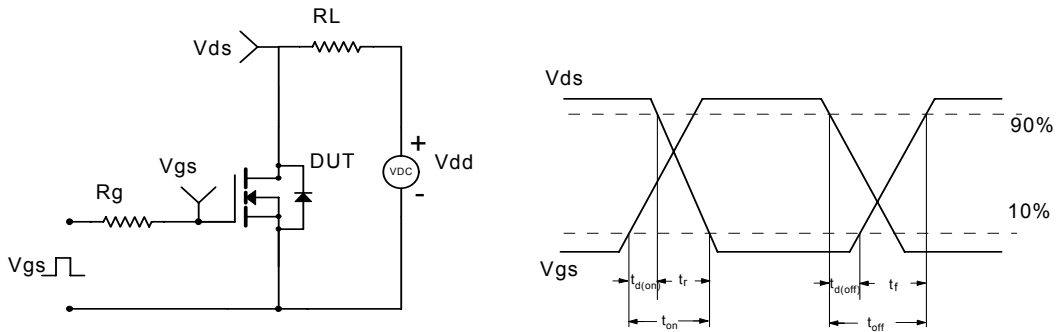


Figure 20: Diode Reverse Recovery Time and Softness Factor vs. di/dt

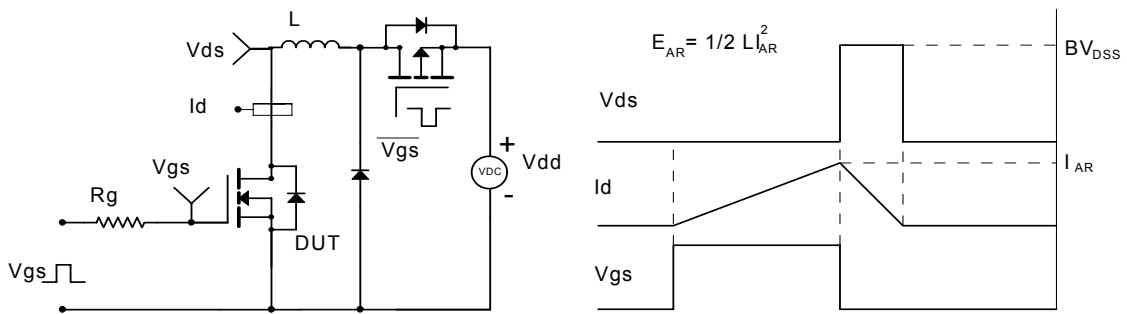
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

