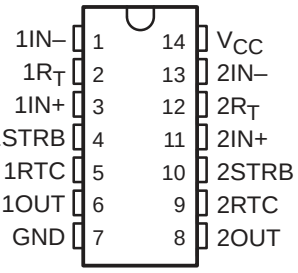
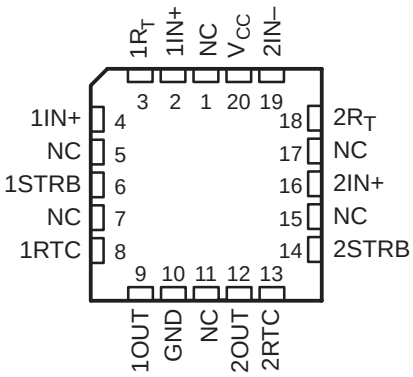
SLLS092D – OCTOBER 1972 – REVISED APRIL 1998

- **Single 5-V Supply**
- **Differential Line Operation**
- **Dual Channels**
- **TTL Compatibility**
- **±15-V Common-Mode Input Voltage Range**
- **±15-V Differential Input Voltage Range**
- **Individual Channel Strobes**
- **Built-In Optional Line-Termination Resistor**
- **Individual Frequency Response Controls**
- **Designed for Use With Dual Differential Drivers SN55183 and SN75183**
- **Designed to Be Interchangeable With National Semiconductor DS7820A and DS8820A**

SN55182 . . . J OR W PACKAGE
SN75182 . . . N PACKAGE
(TOP VIEW)



SN55182 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

THE SN55182 IS NOT RECOMMENDED FOR NEW DESIGNS

description

The SN55182 and SN75182 dual differential line receivers are designed to sense small differential signals in the presence of large common-mode noise. These devices give TTL-compatible output signals as a function of the polarity of the differential input voltage. The frequency response of each channel can be easily controlled by a single external capacitor to provide immunity to differential noise spikes. The output goes to a high level when the inputs are open circuited. A strobe input (STRB) is provided that, when in the low level, disables the receiver and forces the output to a high level.

The receiver is of monolithic single-chip construction, and both halves of the dual circuits use common power-supply and ground terminals.

The SN55182 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN75182 is characterized for operation from 0°C to 70°C.

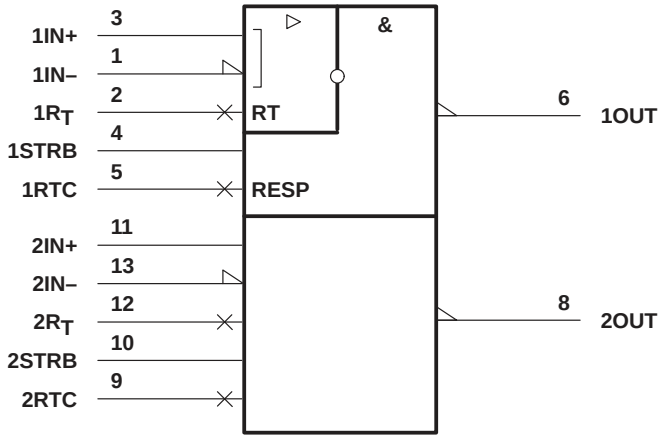
FUNCTION TABLE

INPUTS		OUTPUT OUT
STRB	V_{ID}	
L	X	H
H	H	H
H	L	L

H = $V_I \geq V_{IH}$ min or V_{ID} more positive than V_{TH} max
L = $V_I \leq V_{IL}$ max or V_{ID} more negative than V_{TL} max
X = irrelevant

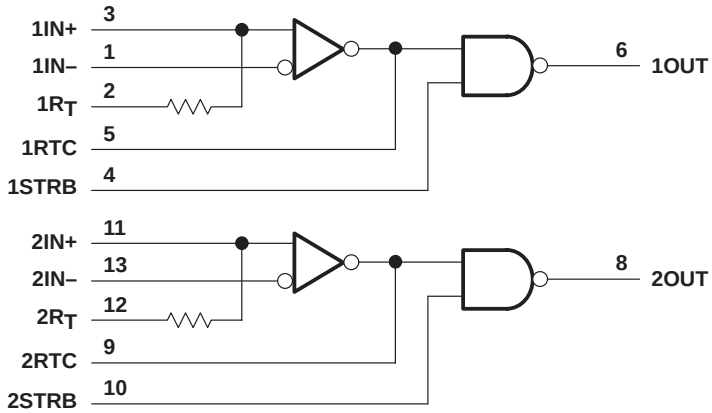
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

logic symbol†



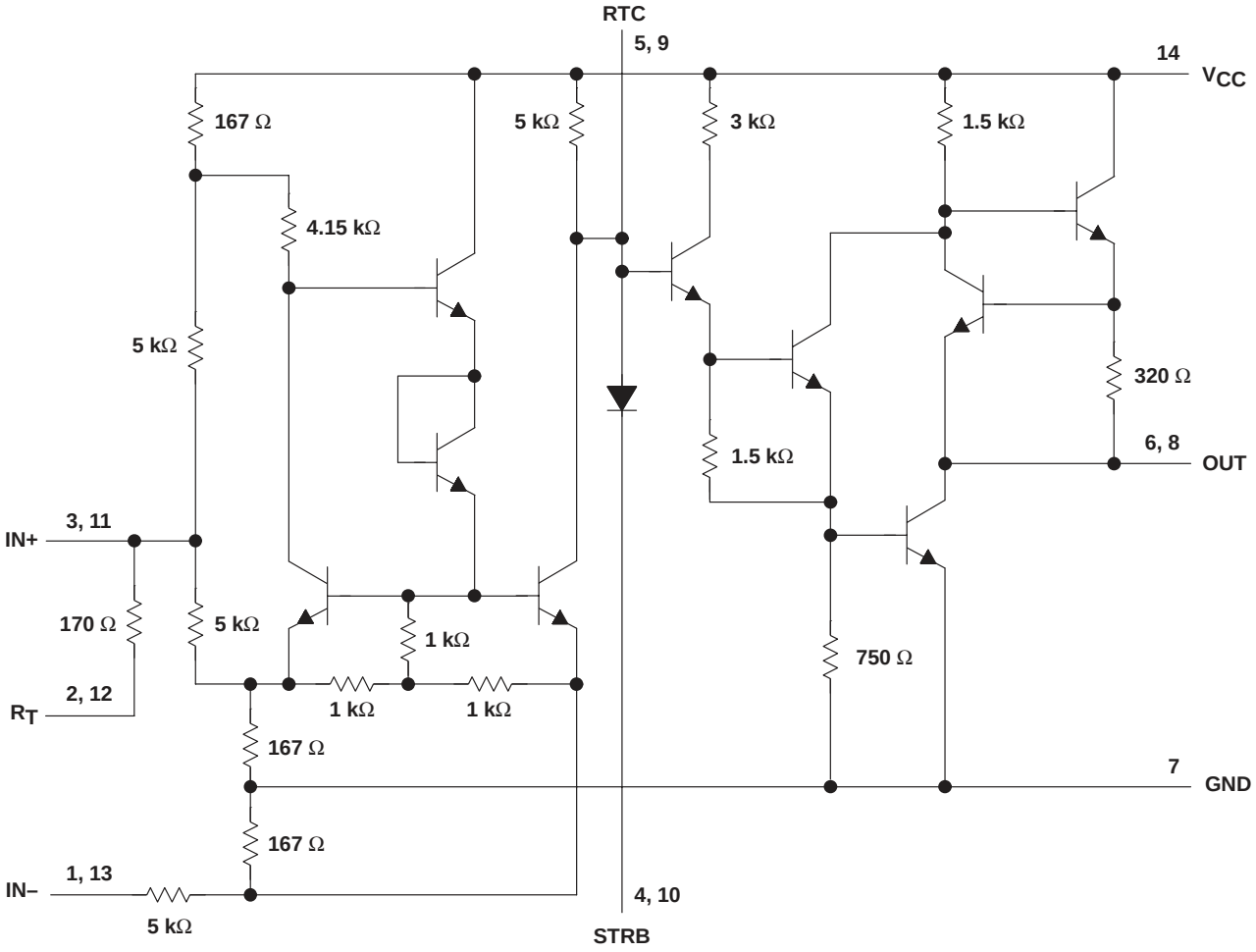
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the J, N, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the J, N, and W packages.

schematic (each receiver)



Resistor values shown are nominal.
Pin numbers shown are for the J, N, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 8 V
Common-mode input voltage, V_{IC} . . . . . ±20 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ±20 V
Strobe input voltage, $V_{I(STRB)}$ . . . . . 8 V
Output sink current . . . . . 50 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or W package . . . . . 300°C
Case temperature for 60 seconds, T_c: FK package . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltage values are at the noninverting terminal with respect to the inverting terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
FK‡	1375 mW	11.0 mW/°C	880 mW	275 mW
J‡	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	–
W‡	1000 mW	8.0 mW/°C	640 mW	200 mW

‡ In the FK, J, and W packages, SN55182 chips are alloy mounted.

recommended operating conditions

	SN55182			SN75182			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
Common-mode input voltage, V_{IC}			±15			±15	V
High-level strobe input voltage, $V_{IH(STRB)}$	2.1		5.5	2.1		5.5	V
Low-level strobe input voltage, $V_{IL(STRB)}$	0		0.9	0		0.9	V
High-level output current, I_{OH}			–400			–400	µA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	–55		125	0		70	°C

electrical characteristics over recommended ranges of V_{CC}, V_{IC}, and operating free-air temperature (unless otherwise noted)

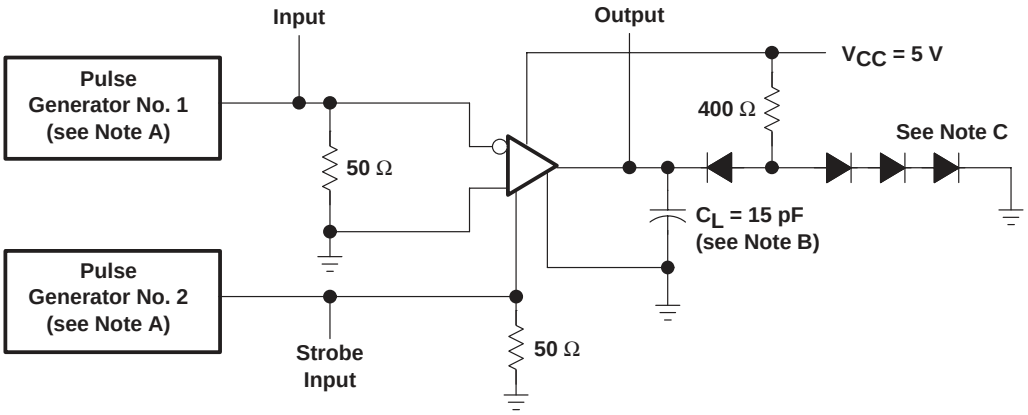
PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		V_O = 2.5 V, I_{OH} = –400 µA	V_{IC} = –3 V to 3 V			0.5	V
				V_{IC} = –15 V to 15 V			1	
$V_{IT–}$	Negative-going input threshold voltage		V_O = 0.4 V, I_{OL} = 16 mA	V_{IC} = –3 V to 3 V			–0.5	V
				V_{IC} = –15 V to 15 V			–1	
V_{OH}	High-level output voltage		V_{ID} = 1 V, $V_{(STRB)}$ = 2.1 V, I_{OH} = –400 µA		2.5	4.2	5.5	V
			V_{ID} = –1 V, $V_{(STRB)}$ = 0.4 V, I_{OH} = –400 µA		2.5	4.2	5.5	
V_{OL}	Low-level output voltage		V_{ID} = –1 V, $V_{(STRB)}$ = 2.1 V, I_{OL} = 16 mA			0.25	0.4	V
I_I	Input current	Inverting input	V_{IC} = 15 V			3	4.2	mA
			V_{IC} = 0			0	–0.5	
			V_{IC} = –15 V			–3	–4.2	
		Noninverting input	V_{IC} = 15 V			5	7	
			V_{IC} = 0			–1	–1.4	
			V_{IC} = –15 V			–7	–9.8	
$I_{IH(STRB)}$	High-level strobe input current		$V_{(STRB)}$ = 5.5 V				5	µA
$I_{IL(STRB)}$	Low-level strobe input current		$V_{(STRB)}$ = 0			–1	–1.4	mA
r_i	Input resistance	Inverting input			3.6	5		kΩ
		Noninverting input			1.8	2.5		
	Line-terminating resistance		T_A = 25°C		120	170	250	Ω
I_{OS}	Short-circuit output current		V_{CC} = 5.5 V,	V_O = 0	–2.8	–4.5	–6.7	mA
I_{CC}	Supply current (average per receiver)		V_{IC} = 15 V,	V_{ID} = –1 V		4.2	6	mA
			V_{IC} = 0,	V_{ID} = –0.5 V		6.8	10.2	
			V_{IC} = –15 V,	V_{ID} = –1 V		9.4	14	

† Unless otherwise noted, $V_{(STRB)} \geq 2.1$ V or open.
‡ All typical values are at V_{CC} = 5 V, V_{IC} = 0, and T_A = 25°C.

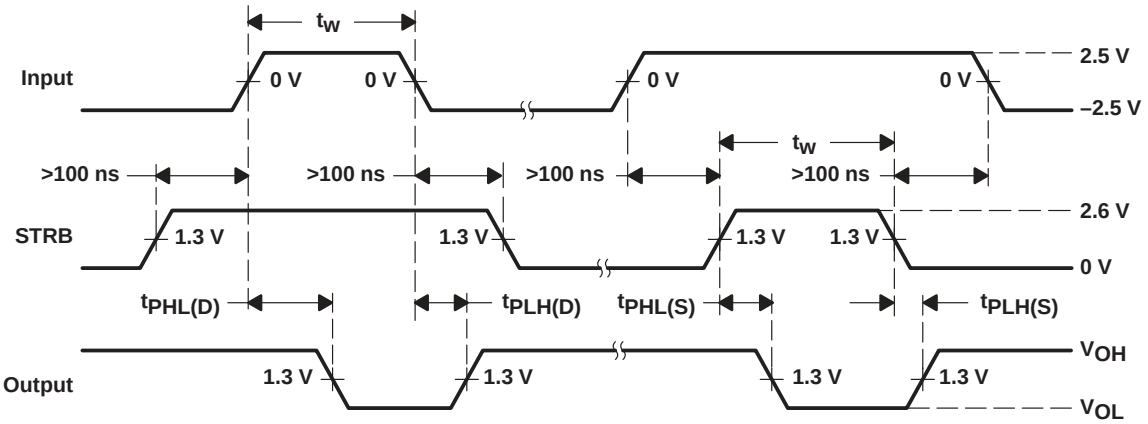
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH(D)}$	Propagation delay time, low- to high-level output from differential input	R_L = 400 Ω, C_L = 15 pF, see Figure 1		18	40	ns
$t_{PHL(D)}$	Propagation delay time, high- to low-level output from differential input	R_L = 400 Ω, C_L = 15 pF, see Figure 1		31	45	ns
$t_{PLH(S)}$	Propagation delay time, low- to high-level output from STRB input	R_L = 400 Ω, C_L = 15 pF, see Figure 1		9	30	ns
$t_{PHL(S)}$	Propagation delay time, high- to low-level output from STRB input	R_L = 400 Ω, C_L = 15 pF, see Figure 1		15	25	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_O = 50 Ω, $t_r \le 10$ ns, $t_f \le 10$ ns, t_w = 0.5 ±0.1 µs, PRR ≤ 1 MHz.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS†

DIFFERENTIAL INPUT THRESHOLD VOLTAGE vs SUPPLY VOLTAGE

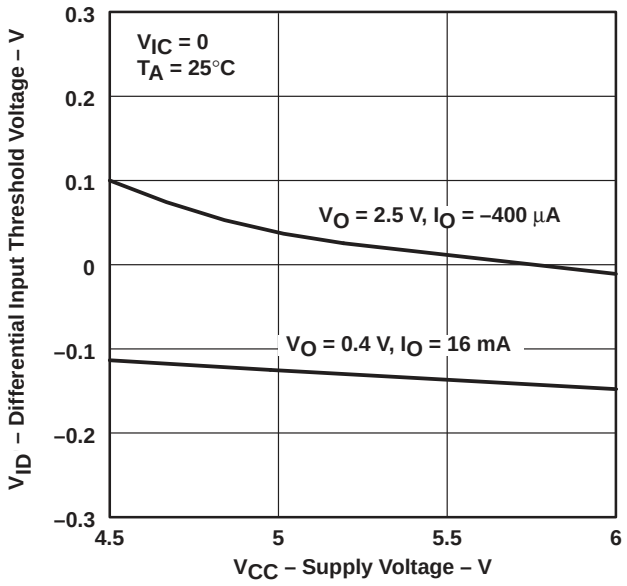


Figure 2

DIFFERENTIAL INPUT THRESHOLD VOLTAGE vs COMMON-MODE INPUT VOLTAGE

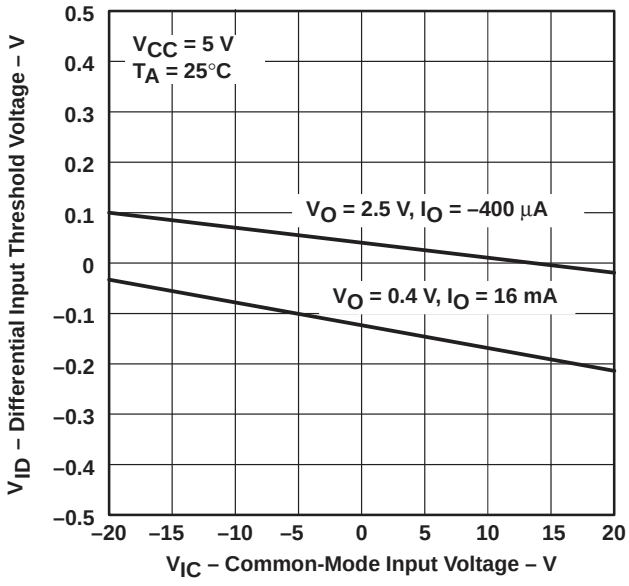


Figure 3

DIFFERENTIAL INPUT THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE

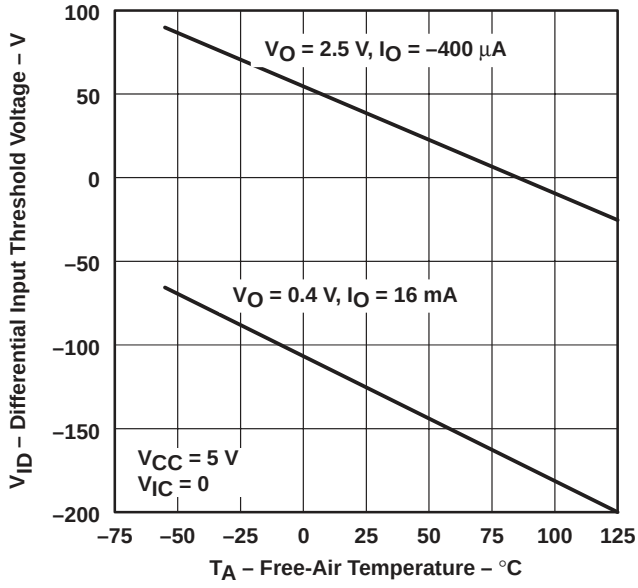


Figure 4

† Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

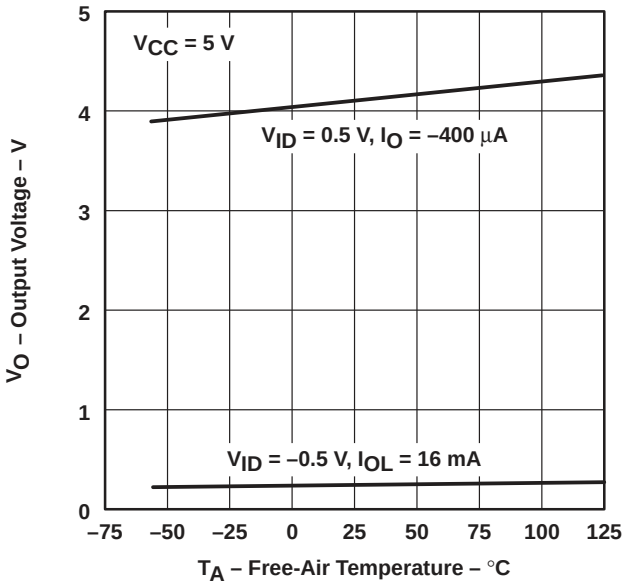


Figure 5

VOLTAGE TRANSFER CHARACTERISTICS

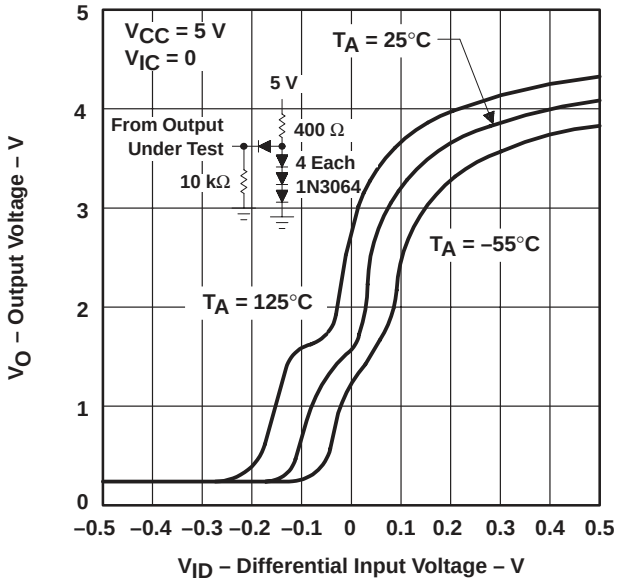


Figure 6

INPUT CURRENT vs INPUT VOLTAGE

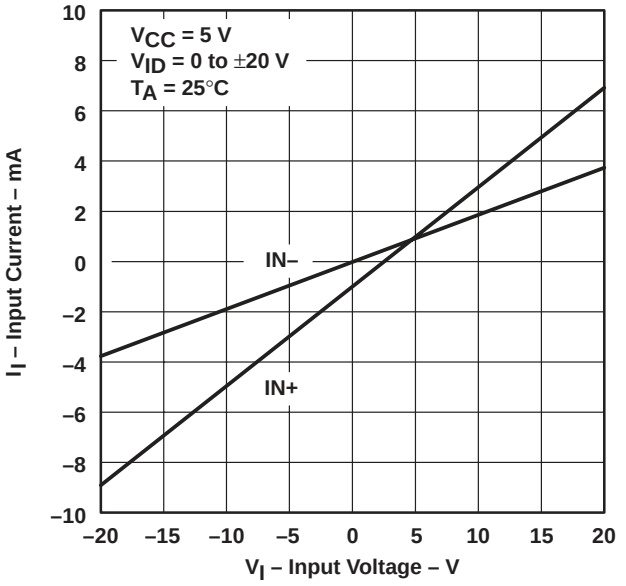


Figure 7

TERMINATING RESISTANCE vs FREE-AIR TEMPERATURE

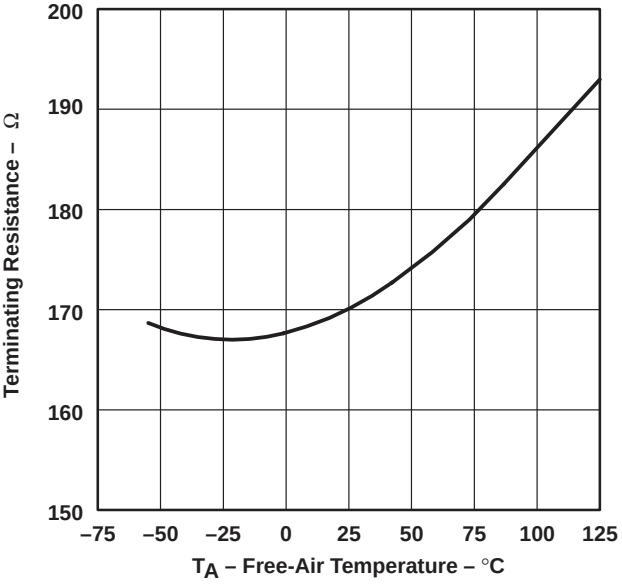


Figure 8

† Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

TYPICAL CHARACTERISTICS†

**SUPPLY CURRENT
(AVERAGE PER RECEIVER)
vs
COMMON-MODE INPUT VOLTAGE**

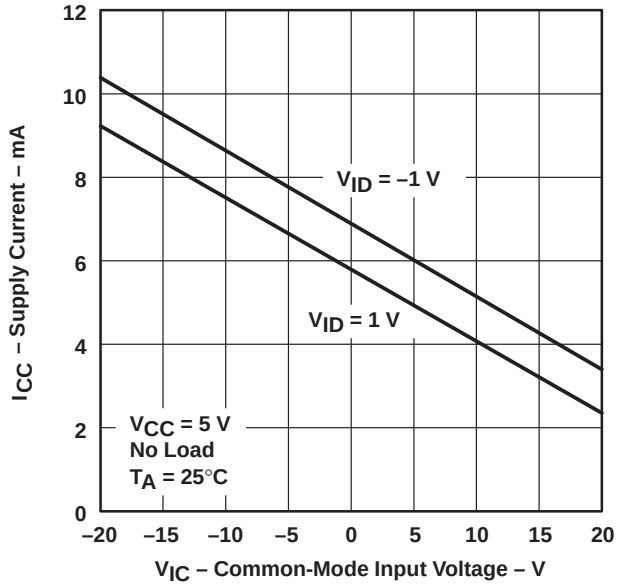


Figure 9

**POWER DISSIPATION
(AVERAGE PER RECEIVER)
vs
COMMON-MODE INPUT VOLTAGE**

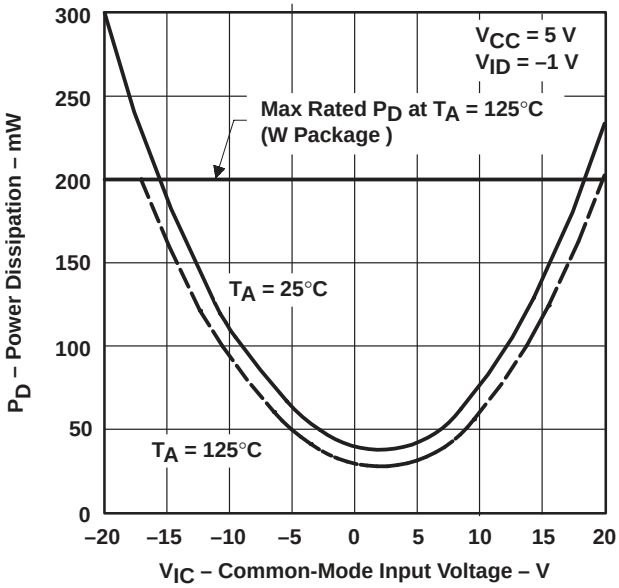
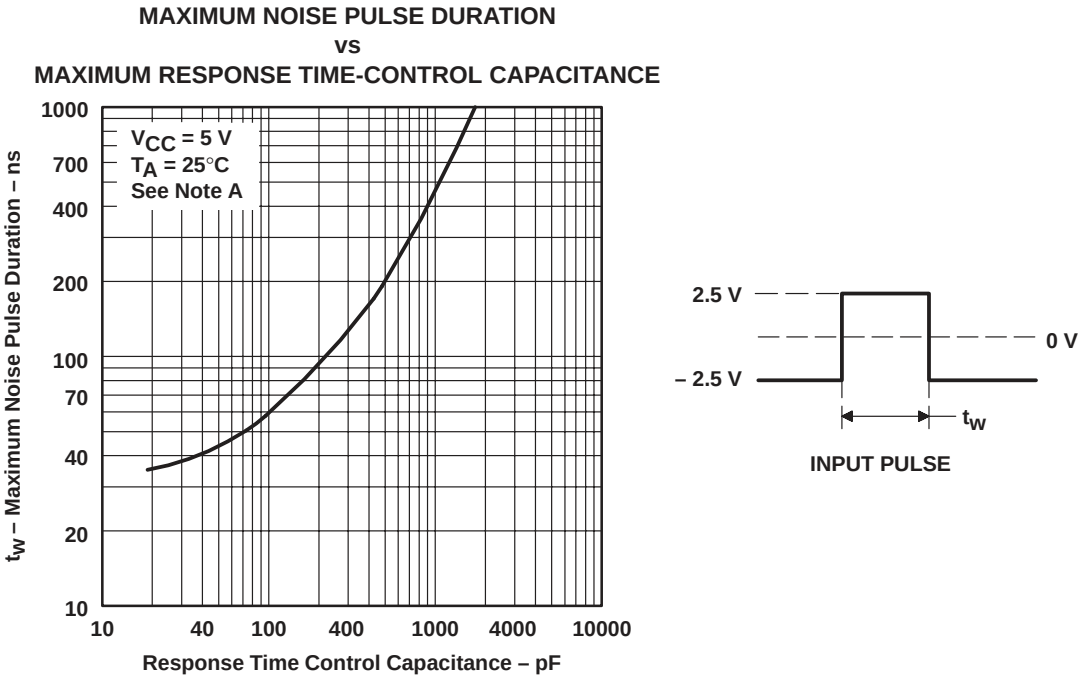


Figure 10

† Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

TYPICAL CHARACTERISTICS†



NOTE A: Figure 11 shows the maximum duration of the illustrated pulse that can be applied differently without the output changing from the low to high level.

Figure 11

† Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

TYPICAL CHARACTERISTICS†

PROPAGATION DELAY TIME FROM DIFFERENTIAL INPUT vs FREE-AIR TEMPERATURE

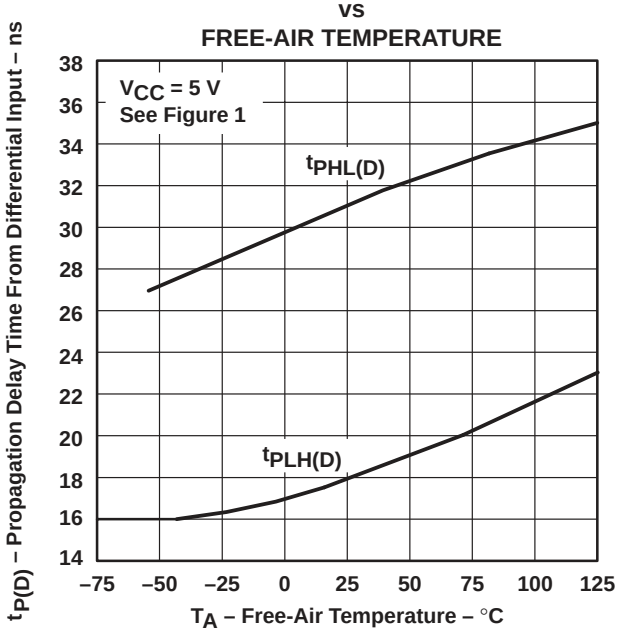


Figure 12

PROPAGATION DELAY TIME FROM STROBE INPUT vs FREE-AIR TEMPERATURE

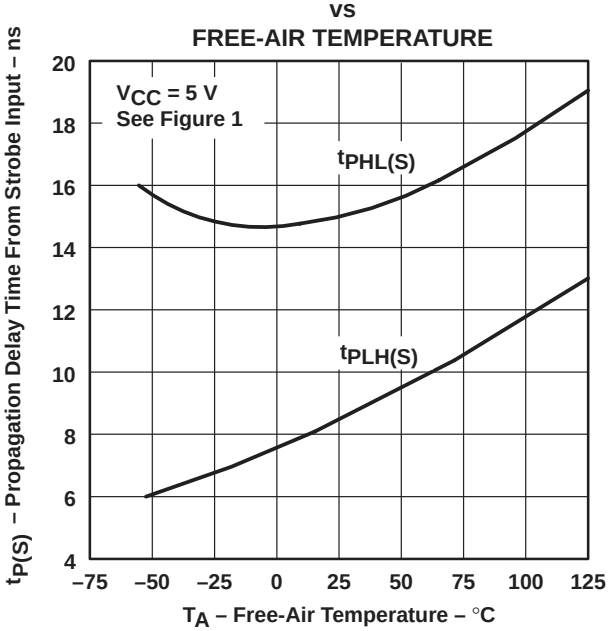


Figure 13

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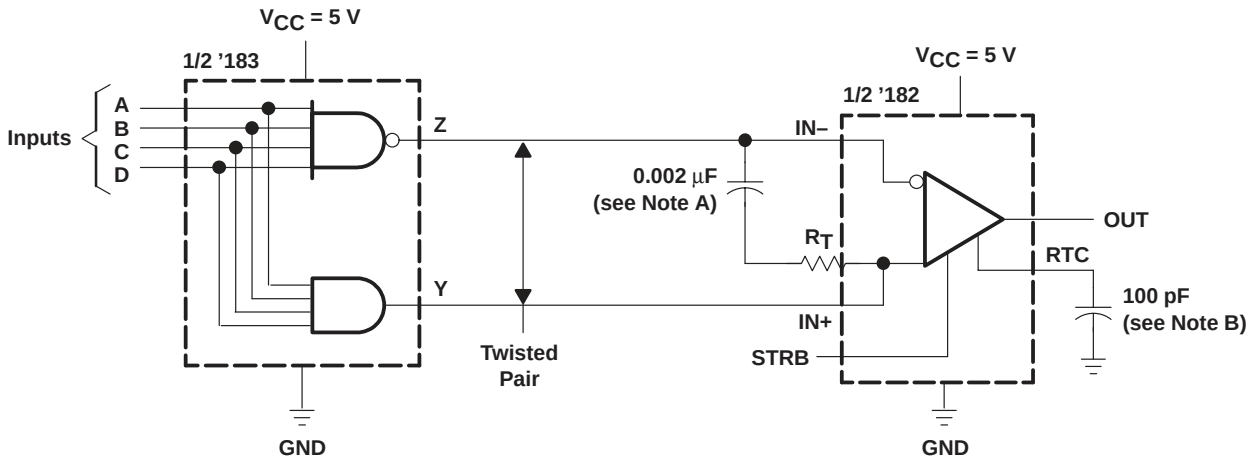
APPLICATION INFORMATION



NOTES: A. When the inputs are open circuited, the output is high. A capacitor may be used for dc isolation of the line-terminating resistor. At the frequency of operation, the impedance of the capacitor should be relatively small.

Example: let f = 5 MHz
C = 0.002 μF

$$Z_{(C)} = \frac{1}{2\pi fC} = \frac{1}{2\pi(5 \times 10^{6})(0.002 \times 10^{-6})}$$

$$Z_{(C)} \approx 16\Omega$$

B. Use of a capacitor to control response time is optional.

Figure 14. Transmission of Digital Data Over Twisted-Pair Line

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SN75182, DUAL DIFFERENTIAL LINE RECEIVER

Device Status: Active

Parameter Name	SN75182
Receivers Per Package	2
Receiver tpd (ns)	45
Receiver (Vth) (mV)	1000
Supply Voltage(s) (V)	5
ICC (max) (mA)	10.2
Footprint	DS8820

Description

The SN55182 and SN75182 dual differential line receivers are designed to sense small differential signals in the presence of large common-mode noise. These devices give TTL-compatible output signals as a function of the polarity of the differential input voltage. The frequency response of each channel can be easily controlled by a single external capacitor to provide immunity to differential noise spikes. The output goes to a high level when the inputs are open circuited. A strobe input (STRB) is provided that, when in the low level, disables the receiver and forces the output to a high level.

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$L = V_I <= V_{IL}$ max or V_{ID} more negative than V_{TL} max
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Features

- Single 5-V Supply
- Differential Line Operation
- Dual Channels
- TTL Compatibility
- ±15-V Common-Mode Input Voltage Range
- ±15-V Differential Input Voltage Range
- Individual Channel Strobes
- Built-In Optional Line-Termination Resistor
- Individual Frequency Response Controls
- Designed for Use With Dual Differential Drivers SN55183 and SN75183
- Designed to Be Interchangeable With National Semiconductor DS7820A and DS8820A

To view the following documents, Acrobat Reader 3.x is required.
To download a document to your hard drive, right-click on the link and choose 'Save'.

Datasheets

Full datasheet in Acrobat PDF: slls092d.pdf (190 KB)
Full datasheet in Zipped PostScript: slls092d.psz (164 KB)

Pricing/Samples/Availability

Orderable Device	Package	Pins	Temp (°C)	Status	Price/unit USD (100-999)	Pack Qty	Availability / Samples
SN75182D	D	14	0 TO 70	NRND	2.00	50	Check stock or order
SN75182DR	D	14	0 TO 70	ACTIVE	1.70	2500	Check stock or order
SN75182N	N	14	0 TO 70	ACTIVE	2.00	25	Check stock or order
SN75182NS	NS	14	0 TO 70	ACTIVE			Check stock or order

Application Reports

- 422 AND 485 OVERVIEW AND SYSTEM CONFIGURATIONS (SLLA070 - Updated: 02/15/2000)
- ANALOG APPLICATIONS JOURNAL, FEBRUARY 2000 (SLYT012A - Updated: 03/23/2000)
- ANALOG APPLICATIONS JOURNAL, NOVEMBER 1999 (SLYT010A - Updated: 03/23/2000)
- COMPARING BUS SOLUTIONS (SLLA067 - Updated: 03/06/2000)
- ELECTROSTATIC DISCHARGE APPLICATION NOTE (SSYA008 - Updated: 05/05/1999)
- JITTER ANALYSIS (SLLA075 - Updated: 03/31/2000)
- SKEW DEFINITIONS (SLLA060 - Updated: 08/13/1999)
- THERMAL CHARACTERISTICS OF LINEAR AND LOGIC PACKAGES USING JEDEC PCB DESIGNS (SZZA017A - Updated: 09/15/1999)

Related Documents

- A STATISTICAL SURVEY OF COMMON-MODE NOISE (SLLA057, 131 KB - Updated: 12/23/1999)

Table Data Updated on: 6/2/2000