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OPAx180-Q1 0.1-µV/°C Drift, Low-Noise, Rail-to-Rail Output, 36-V, Zero-Drift Operational Amplifiers

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - OPA180-Q1 Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature Range
  - OPA2180-Q1 Device Temperature Grade 2: –40°C to +105°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 1C
  - Device CDM ESD Classification Level C5
  - Wide Supply Range: ±2 V to ±18 V
  - Low Offset Voltage: 75 µV (Maximum)
  - Zero Drift: 0.1 µV/°C
  - Low Noise: 10 nV/$\sqrt{\text{Hz}}$
  - Very Low 1/f Noise
  - Excellent DC Precision:
    - PSRR: 126 dB
    - CMRR: 114 dB
    - Open-Loop Gain (A_{OL}): 120 dB
  - Quiescent Current: 525 µA (Maximum)
  - Rail-to-Rail Output:
    Input Includes Negative Rail
  - Low Bias Current: 250 pA (Typical)
  - RFI Filtered Inputs
  - *Micro*SIZE Packages

2 Applications

- Automotive Precision Current Measurements
- Onboard Chargers (OBC)
- Battery Management Systems (BMS)
- Motor Control
- Traction Inverters

3 Description

The OPA180-Q1 and OPA2180-Q1 operational amplifiers (op amps) use TI's proprietary zero-drift techniques to simultaneously provide low offset voltage (75 µV), and near zero-drift over time and temperature. These miniature, high-precision, low-quiescent-current op amps offer high input impedance and rail-to-rail output swing within 18 mV of the rails. The input common-mode range includes the negative rail. Single- or dual-supplies ranging from 4 V to 36 V (±2 V to ±18 V) can be used.

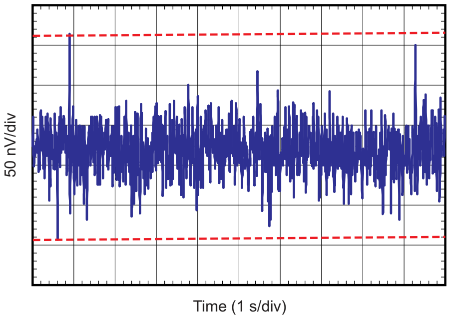
The single-channel and dual-channel versions are offered in VSSOP-8 packages. The single package offering (OPA180-Q1) is specified from –40°C to +125°C, and the dual package (OPA2180-Q1) is specified from –40°C to +105°C.

Device Information(1)

DEVICE NAME	PACKAGE	BODY SIZE (NOM)
OPA180-Q1	VSSOP (8)	3.00 mm × 3.00 mm
OPA2180-Q1	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Low Noise
(Peak-to-Peak Noise = 250 nV)



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4 Revision History

Changes from Original (June 2017) to Revision A — Page

- Added OPA180-Q1 and OPA4180-Q1 device temperature grades to *Features* list ... 1
- Changed OPA2180-Q1 device temperature grade from grade 1 to grade 2 in *Features* list ... 1
- Changed OPA2180-Q1 ambient operating temperature range from "–40°C to +105°C" to "–40°C to +125°C" in *Features* list ... 1
- Changed OPA180-Q1 and OPA4180-Q1 operating temperature from "–40°C to +105°C" to "–40°C to +125°C" in *Description* section ... 1
- Changed input offset voltage drift temperature range from T_A = –40°C to 105°C to T_A = –40°C to +125°C in *Electrical Characteristics* table ... 8
- Changed power supply rejection ratio temperature range from T_A = –40°C to 105°C to T_A = –40°C to +125°C in *Electrical Characteristics* table ... 8
- Changed OPA180-Q1 input bias current temperature range from T_A = –40°C to 105°C to T_A = –40°C to +125°C in *Electrical Characteristics* table ... 8
- Changed OPA180-Q1 input offset current temperature range from T_A = –40°C to 105°C to T_A = –40°C to +125°C in *Electrical Characteristics* table ... 8
- Changed common-mode rejection ratio temperature range from T_A = –40°C to 105°C to T_A = –40°C to +125°C in *Electrical Characteristics* table ... 8
- Changed open-loop voltage gain temperature range from T_A = –40°C to 105°C to T_A = –40°C to +125°C in *Electrical Characteristics* table ... 8
- Changed voltage output swing from rail temperature range from T_A = –40°C to 105°C to T_A = –40°C to +125°C in *Electrical Characteristics* table ... 9
- Changed quiescent current temperature range from T_A = –40°C to 105°C to T_A = –40°C to +125°C in *Electrical Characteristics* table ... 9
- Changed operating temperature from "–40°C to +105°C" to " –40°C to +125°C" in *Feature Description* section ... 16
- Updated Figure 34 ... 22

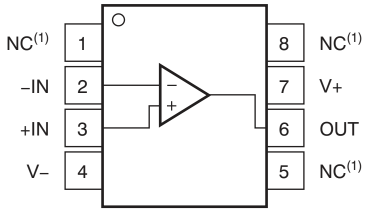
5 Device Comparison Table

Table 1. Zero-Drift Amplifier Portfolio

VERSION	PRODUCT	OFFSET VOLTAGE (µV)	OFFSET VOLTAGE DRIFT (µV/°C)	BANDWIDTH (MHz)
Single	OPA188-Q1(4 V to 36 V)	25	0.085	2
	OPA180-Q1 (4 V to 36 V)	75	0.35	2
	OPA333 (5 V)	10	0.05	0.35
	OPA378 (5 V)	50	0.25	0.9
	OPA735 (12 V)	5	0.05	1.6
Dual	OPA2188-Q1 (4 V to 36 V)	25	0.085	2
	OPA2180-Q1 (4 V to 36 V)	75	0.35	2
	OPA2333 (5 V)	10	0.05	0.35
	OPA2378 (5 V)	50	0.25	0.9
	OPA2735 (12 V)	5	0.05	1.6
Quad	OPA4188 (4 V to 36 V)	25	0.085	2
	OPA4180 (4 V to 36 V)	75	0.35	2
	OPA4330 (5 V)	50	0.25	0.35

6 Pin Configuration and Functions

OPA180-Q1 DGK Package
8-Pin VSSOP
Top View

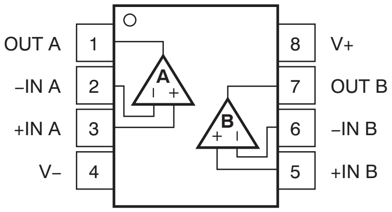


(1) NC- no internal connection

Pin Functions: OPA180-Q1

PIN		DESCRIPTION
NAME	NO.	
–IN	2	Inverting input
+IN	3	Noninverting input
NC	1, 5, 8	No connection
OUT	6	Output
V–	4	Negative power supply
V+	7	Positive power supply

OPA2180-Q1 DGK Package
8-Pin VSSOP
Top View



Pin Functions: OPA2180-Q1

PIN		DESCRIPTION
NAME	NO.	
–IN A	2	Inverting input, channel A
+IN A	3	Noninverting input, channel A
–IN B	6	Inverting input, channel B
+IN B	5	Noninverting input, channel B
OUT A	1	Output, channel A
OUT B	7	Output, channel B
V–	4	Negative power supply
V+	8	Positive power supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
	Supply voltage			±20, ±40 (single-supply)	V
	Signal input terminals	Voltage	(V–) – 0.5	(V+) + 0.5	V
		Current		±10	mA
	Output short-circuit(2)		Continuous		
	Operating temperature		–55	125	°C
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±1500	V
		Charged-device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted), R_L = 10 kΩ connected to V_S / 2, and V_{COM} = V_{OUT} = V_S / 2, (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage [(V+) – (V–)]	Single-supply	4.5		36	V
	Bipolar-supply	±2.25		±18	V
Operating temperature		–40		125	°C

7.4 Thermal Information: OPA180-Q1

THERMAL METRIC[1]		OPA180-Q1 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	180.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	67.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	102.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	100.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Thermal Information: OPA2180-Q1

THERMAL METRIC[1]		OPA2180-Q1 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	159.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	37.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	48.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	77.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.6 Electrical Characteristics: V_S = ±2 V to ±18 V (V_S = 4 V to 36 V)

at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, and V_{COM} = V_{OUT} = V_S / 2, (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{IO}	Input offset voltage			15	75	μV
dV_{IO}/dT	Input offset voltage drift	T_A = –40°C to +125°C		0.1	0.35	μV/°C
PSRR	Power-supply rejection ratio	V_S = 4 V to 36 V V_{CM} = V_S / 2		0.1	0.5	μV/V
		T_A = –40°C to +125°C, V_S = 4 V to 36 V V_{CM} = V_S / 2			0.5	μV/V
	Long-term stability			4(1)		μV
	Channel separation, DC			1		μV/V
INPUT BIAS CURRENT						
I_{IB}	Input bias current	OPA2180-Q1		±0.25	±1	nA
		OPA2180-Q1: T_A = –40°C to +105°C	18		±5	nA
		OPA180-Q1		±0.25	±1.7	nA
		OPA180-Q1: T_A = –40°C to +125°C	18		±6	nA
I_{IO}	Input offset current	OPA2180-Q1		±0.5	±2	nA
		OPA2180-Q1: T_A = –40°C to +105°C	6		±2.5	nA
		OPA180-Q1			±3.4	nA
		OPA180-Q1: T_A = –40°C to +125°C	6		±3	nA
NOISE						
	Input voltage noise	f = 0.1 Hz to 10 Hz		0.25		μV_{PP}
e_n	Input voltage noise density	f = 1 kHz		10		nV/√Hz
i_n	Input current noise density	f = 1 kHz		10		fA/√Hz
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range		V–		(V+) – 1.5	V
CMRR	Common-mode rejection ratio	(V–) < V_{CM} < (V+) – 1.5 V	104	114		dB
		T_A = –40°C to +125°C (V–) + 0.5 V < V_{CM} < (V+) – 1.5 V	100	104		dB
INPUT IMPEDANCE						
z_{id}	Differential			100 || 6		MΩ || pF
z_{ic}	Common-mode			6 || 9.5		10^{12} Ω || pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	(V–) + 500 mV < V_O < (V+) – 500 mV R_L = 10 kΩ	110	120		dB
		T_A = –40°C to +125°C (V–) + 500 mV < V_O < (V+) – 500 mV R_L = 10 kΩ	104	114		dB
FREQUENCY RESPONSE						
GBW	Gain bandwidth product			2		MHz
SR	Slew rate	G = 1		0.8		V/μs
t_s	Settling time 0.1%	V_S = ±18 V, G = 1, 10-V step		22		μs
	0.01%	V_S = ±18 V, G = 1, 10-V step		30		μs
t_{or}	Overload recovery time	V_{IN} × G = V_S		1		μs
THD+N	Total harmonic distortion + noise	f = 1 kHz, G = 1, V_{OUT} = 1 V_{RMS}		0.0001%		

(1) 1000-hour life test at 125°C demonstrated randomly distributed variation in the range of measurement limits, or approximately 4 μV.

Electrical Characteristics: V_S = ±2 V to ±18 V (V_S = 4 V to 36 V) (continued)

at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, and V_{COM} = V_{OUT} = V_S / 2, (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
	Voltage output swing from rail	No load		8	18	mV
		R_L = 10 kΩ		250	300	mV
		T_A = –40°C to +125°C R_L = 10 kΩ		325	360	mV
I_{OS}	Short-circuit current			±18		mA
r_o	Output resistance (open loop)	f = 2 MHz, I_O = 0 mA		120		Ω
C_{LOAD}	Capacitive load drive			1		nF
POWER SUPPLY						
V_S	Operating voltage range		±2 (or 4)		±18 (or 36)	V
I_Q	Quiescent current (per amplifier)			450	525	µA
		T_A = –40°C to +125°C I_O = 0 mA			600	µA
TEMPERATURE						
	Specified range		–40		105	°C
	Operating range		–40		105	°C

7.7 Typical Characteristics: Table of Graphs

Table 2. Characteristic Performance Measurements

DESCRIPTION	FIGURE
I_B and I_{OS} vs Common-Mode Voltage	Figure 1
Input Bias Current vs Temperature	Figure 2
Output Voltage Swing vs Output Current (Maximum Supply)	Figure 3
CMRR vs Temperature	Figure 4
0.1-Hz to 10-Hz Noise	Figure 5
Input Voltage Noise Spectral Density vs Frequency	Figure 6
Open-Loop Gain and Phase vs Frequency	Figure 7
Open-Loop Gain vs Temperature	Figure 8
Open-Loop Output Impedance vs Frequency	Figure 9
Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)	Figure 10, Figure 11
No Phase Reversal	Figure 12
Positive Overload Recovery	Figure 13
Negative Overload Recovery	Figure 14
Small-Signal Step Response (100 mV)	Figure 15, Figure 16
Large-Signal Step Response	Figure 17, Figure 18
Large-Signal Settling Time (10-V Positive Step)	Figure 19
Large-Signal Settling Time (10-V Negative Step)	Figure 20
Short-Circuit Current vs Temperature	Figure 21
Maximum Output Voltage vs Frequency	Figure 22
Channel Separation vs Frequency	Figure 23
EMIRR IN+ vs Frequency	Figure 24

7.8 Typical Characteristics

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

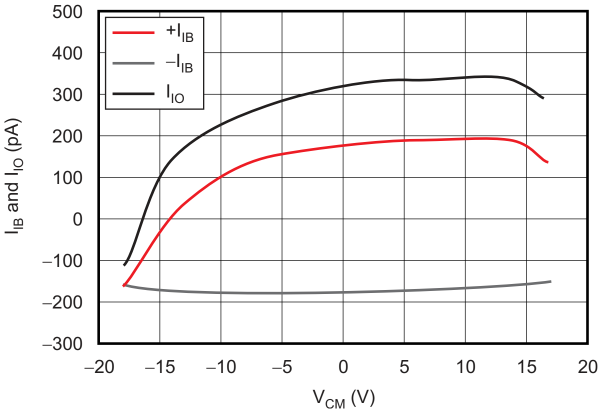


Figure 1. I_{IB} and I_{IO} vs Common-Mode Voltage

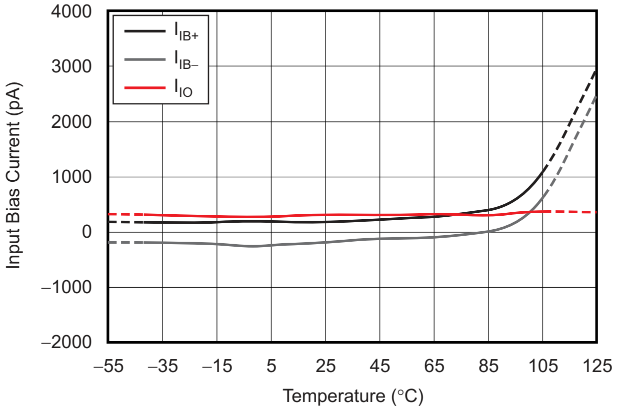


Figure 2. Input Bias Current vs Temperature

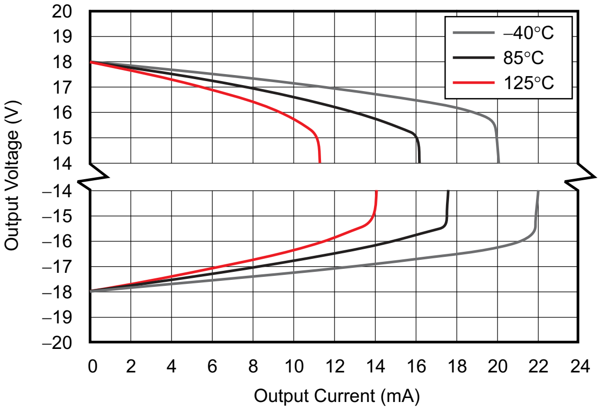
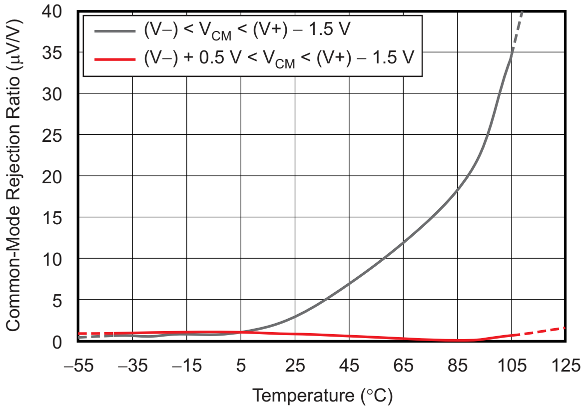
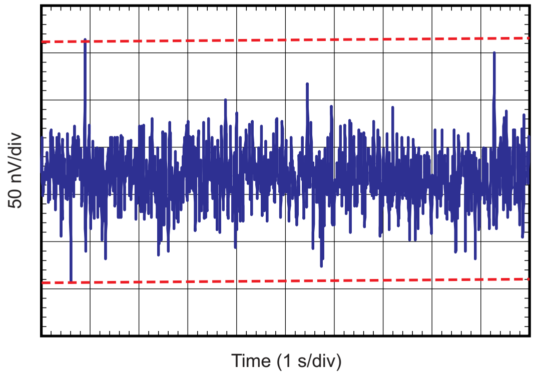


Figure 3. Output Voltage Swing vs Output Current (Maximum Supply)



V_{SUPPLY} = ±2 V

Figure 4. CMRR vs Temperature



Peak-to-Peak Noise = 250 nV

Figure 5. 0.1-Hz to 10-Hz Noise

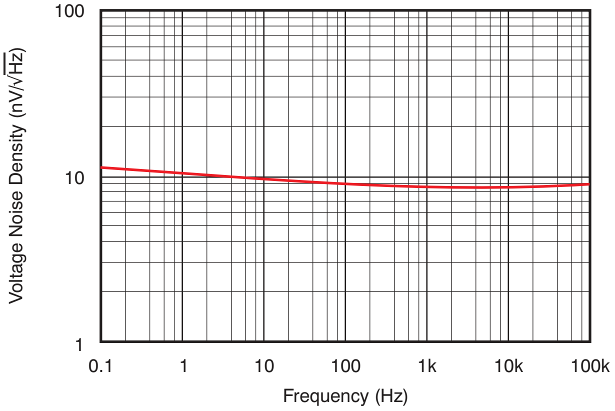


Figure 6. Input Voltage Noise Spectral Density vs Frequency

Typical Characteristics (continued)

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

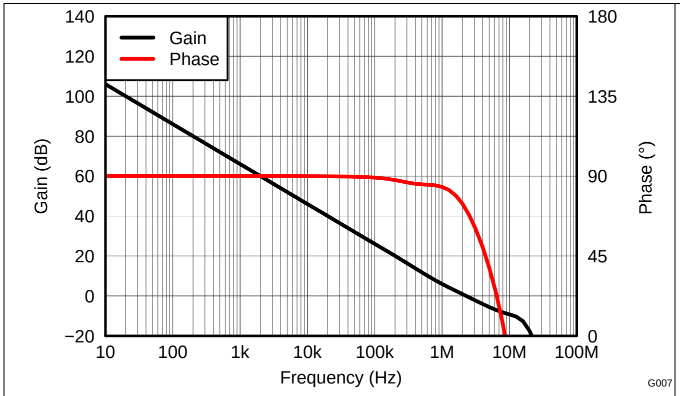


Figure 7. Open-Loop Gain and Phase vs Frequency

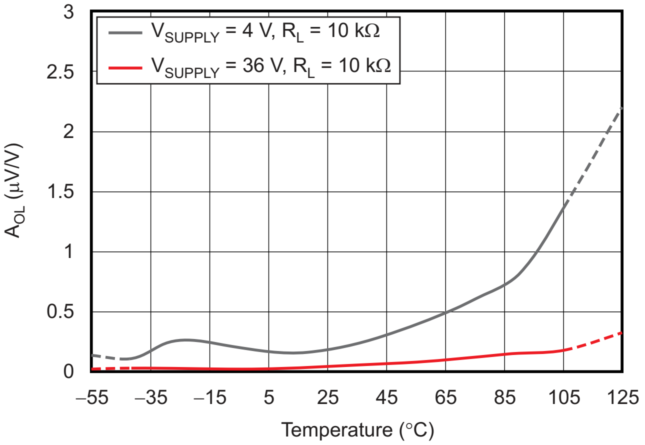


Figure 8. Open-Loop Gain vs Temperature

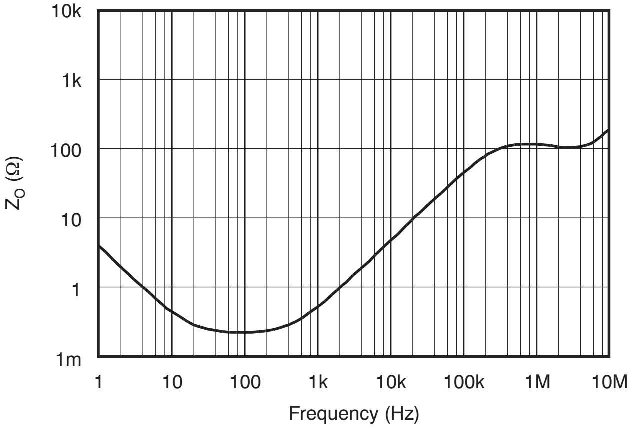


Figure 9. Open-Loop Output Impedance vs Frequency

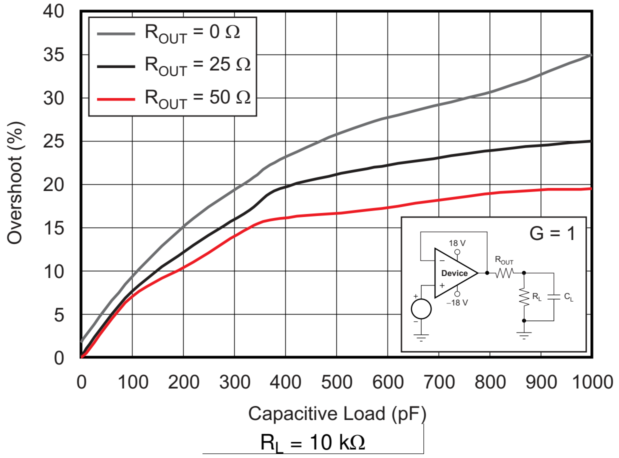


Figure 10. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

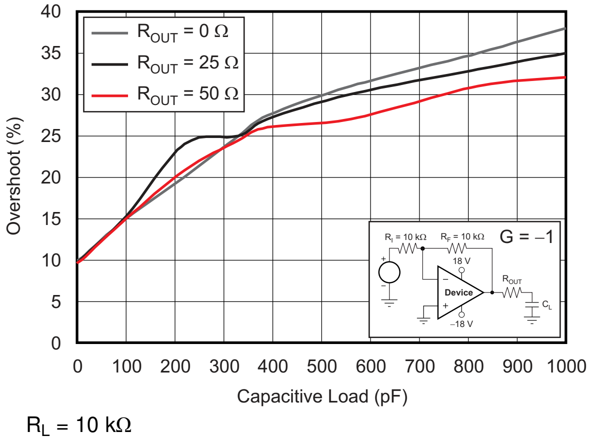


Figure 11. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

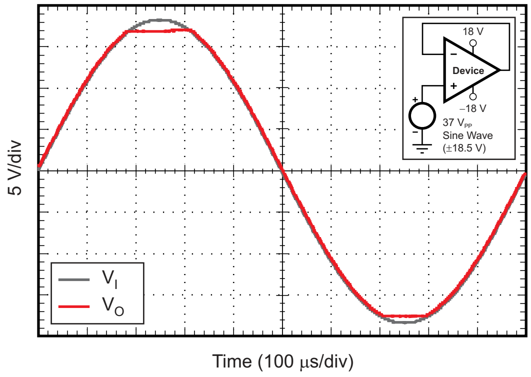


Figure 12. No Phase Reversal

Typical Characteristics (continued)

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

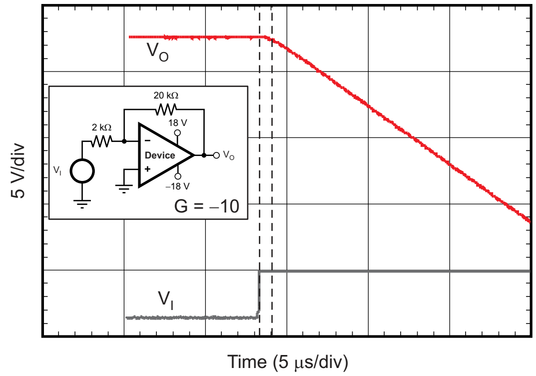


Figure 13. Positive Overload Recovery

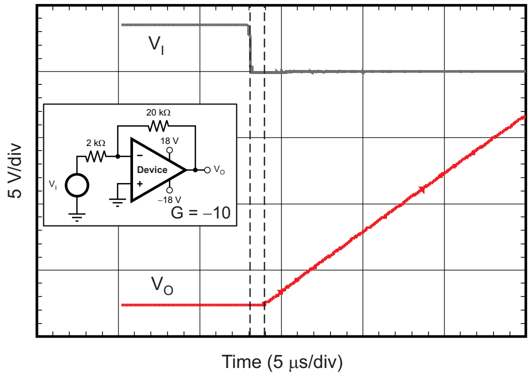
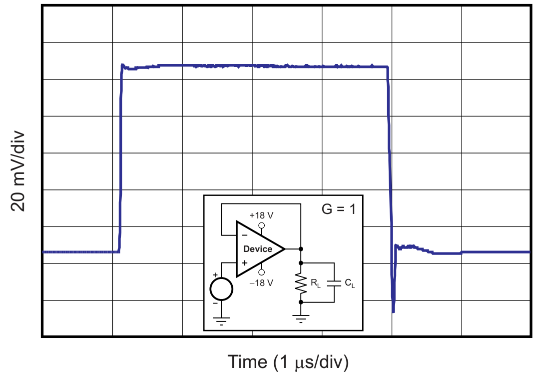
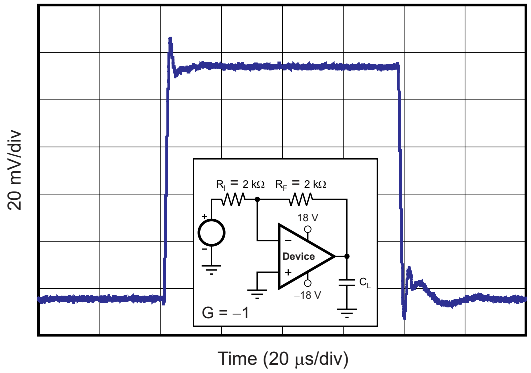


Figure 14. Negative Overload Recovery



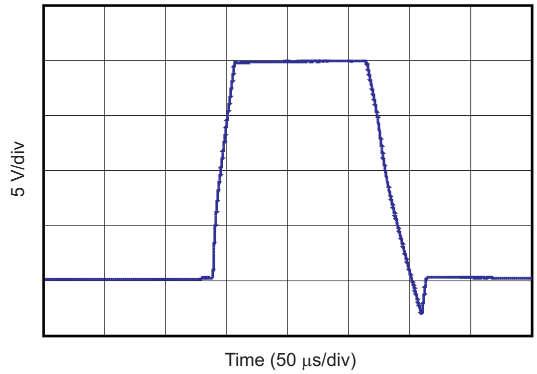
R_L = 10 kΩ C_L = 10 pF

Figure 15. Small-Signal Step Response (100 mV)



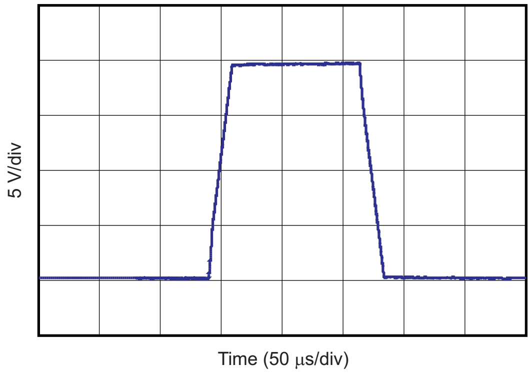
R_L = 10 kΩ C_L = 10 pF

Figure 16. Small-Signal Step Response (100 mV)



G = 1 R_L = 10 kΩ C_L = 10 pF

Figure 17. Large-Signal Step Response

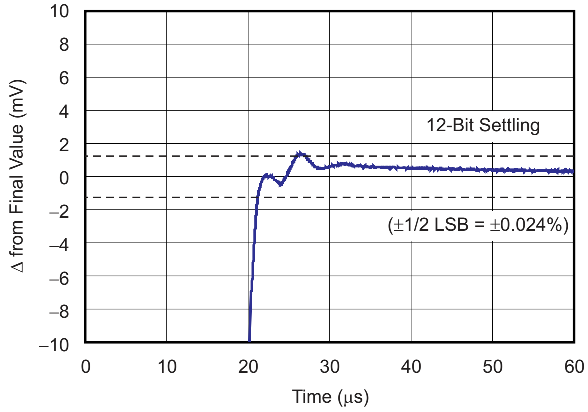


G = –1 R_L = 10 kΩ C_L = 10 pF

Figure 18. Large-Signal Step Response

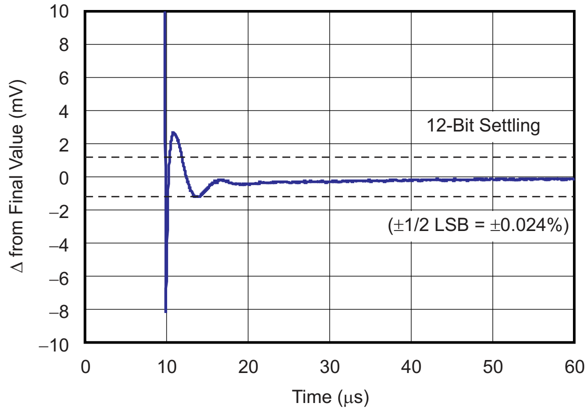
Typical Characteristics (continued)

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.



G = −1

Figure 19. Large-Signal Settling Time (10-V Positive Step)



G = −1

Figure 20. Large-Signal Settling Time (10-V Negative Step)

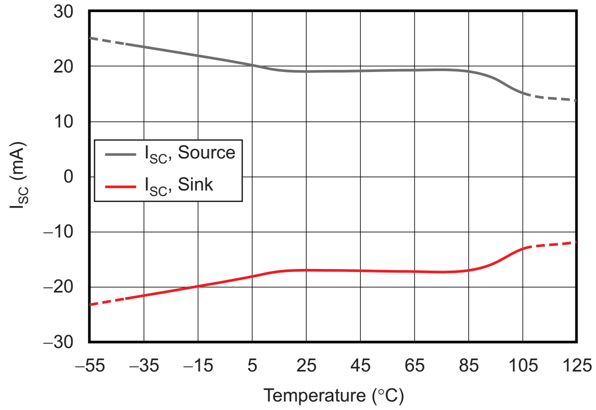


Figure 21. Short-Circuit Current vs Temperature

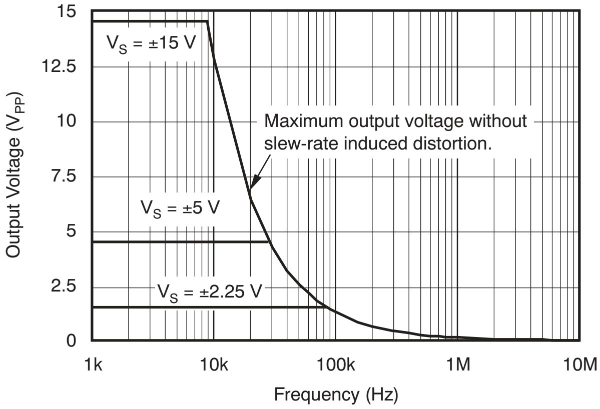


Figure 22. Maximum Output Voltage vs Frequency

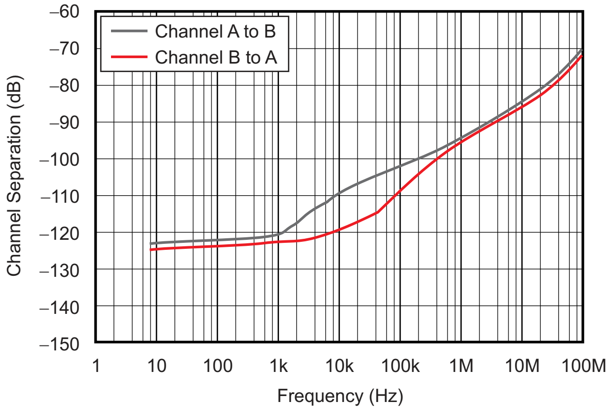


Figure 23. Channel Separation vs Frequency

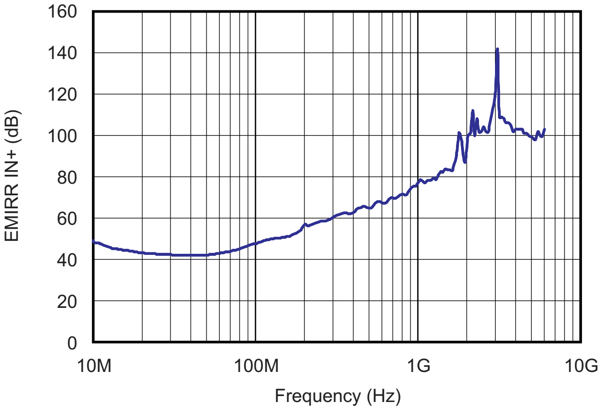


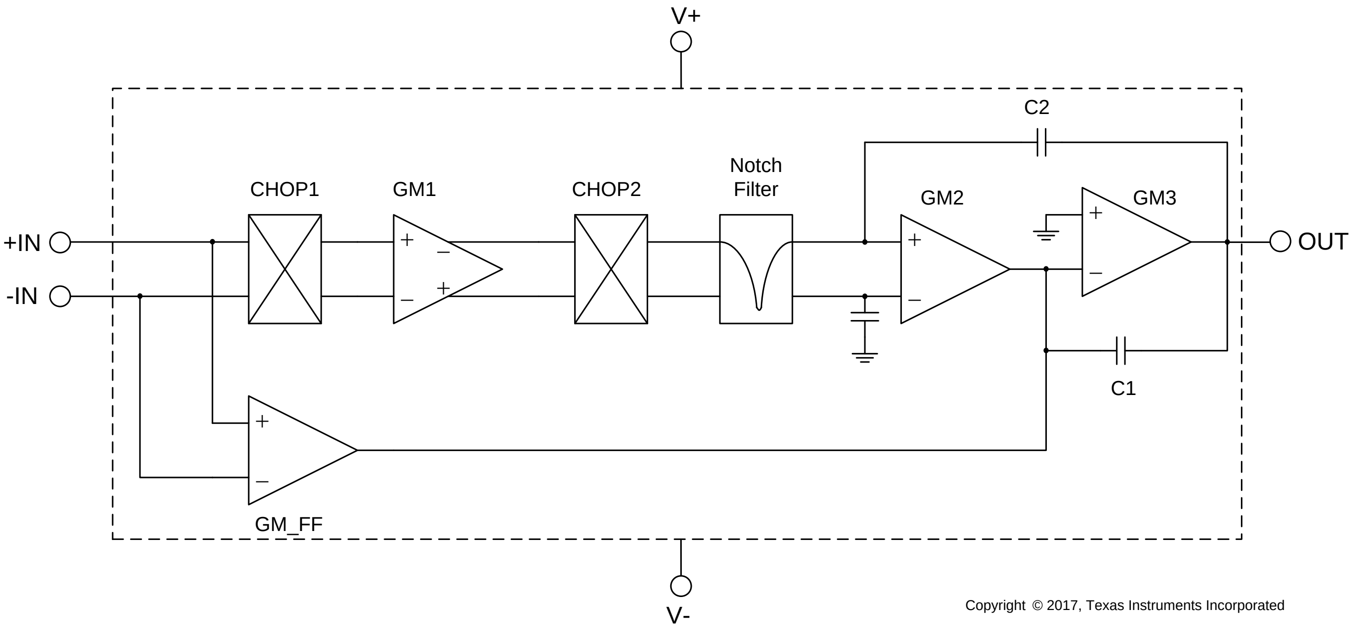
Figure 24. EMIRR IN+ vs Frequency

8 Detailed Description

8.1 Overview

The OPAx180-Q1 family of operational amplifiers combine precision offset and drift with excellent overall performance, making them designed for many precision applications. The precision offset drift of only 0.1 µV/°C provides stability over the entire temperature range. In addition, the devices offer excellent overall performance with high CMRR, PSRR, and A_{OL}. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Operating Characteristics

The OPAx180-Q1 family of amplifiers is specified for operation from 4 V to 36 V (±2 V to ±18 V). Many of the specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

8.3.2 EMI Rejection

The OPAx180-Q1 family uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI interference from sources such as wireless communications and densely populated boards with a mix of analog signal chain and digital components. EMI immunity can improve with circuit design techniques; the OPAx180-Q1 family benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. Figure 25 shows the results of this testing on the OPAx180-Q1 family . For more detailed information, see the *EMI Rejection Ratio of Operational Amplifiers* application report, available for download from www.ti.com.

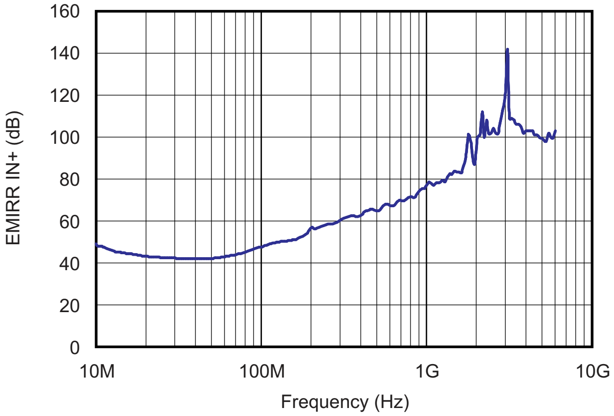


Figure 25. OPAx180-Q1 EMIRR Testing

8.3.3 Phase-Reversal Protection

The OPAx180-Q1 family has an internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the OPAx180-Q1 prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. This performance is shown in Figure 26.

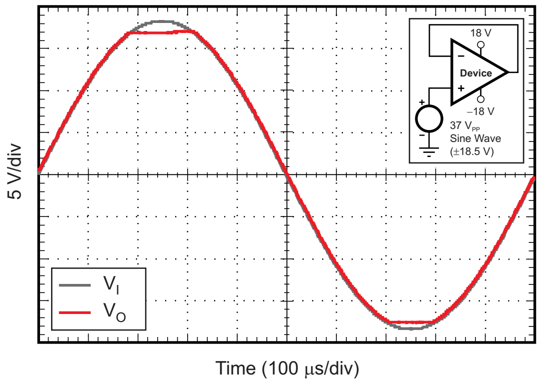
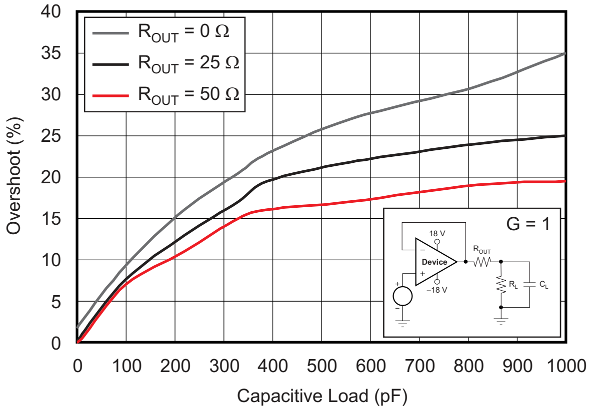


Figure 26. No Phase Reversal

Feature Description (continued)

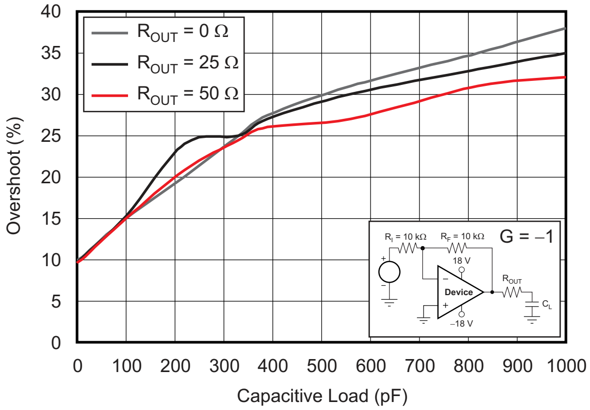
8.3.4 Capacitive Load and Stability

The dynamic characteristics of the OPAx180-Q1 are optimized for a range of common operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, R_{OUT} equal to 50 Ω) in series with the output. Figure 27 and Figure 28 illustrate graphs of small-signal overshoot versus capacitive load for several values of R_{OUT}. See the *Feedback Plots Define Op Amp AC Performance*, application report, available for download from the TI website, for details of analysis techniques and application circuits.



R_L = 10 kΩ   100-mV output step

Figure 27. Small-Signal Overshoot Versus Capacitive Load



R_L = 10 kΩ   100-mV output step

Figure 28. Small-Signal Overshoot Versus Capacitive Load

8.3.5 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA as stated in the *Absolute Maximum Ratings* table. Figure 29 shows how a series input resistor may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.

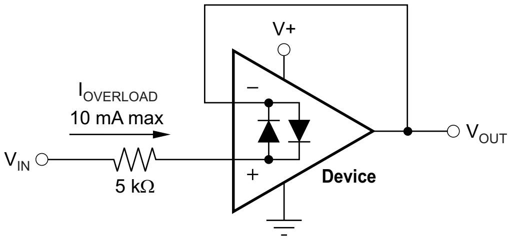


Figure 29. Input Current Protection

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as the pulse discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to protect the core from damage. The energy absorbed by the protection circuitry is then dissipated as heat.

Feature Description (continued)

When the operational amplifier connects into a circuit, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise when an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through ESD cells and rarely involves the absorption device.

If there is an uncertainty about the ability of the supply to absorb this current, external zener diodes may be added to the supply pins. The zener voltage must be selected so the diode does not turn on during normal operation.

However, the zener voltage must be low enough so that the zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.

8.4 Device Functional Modes

The OPAx180-Q1, and OPA2180-Q1 devices are powered on when the supply is connected. These devices can operate as a single-supply operational amplifier or dual-supply amplifier depending on the application. In single-supply operation with V– at ground (0 V), V+ can be any value between 4 V and 36 V. In dual-supply operation, the supply voltage difference between V– and V+ is from 4 V to 36 V. Typical examples of dual-supply configuration are ±5 V, ±10 V, ±15 V, and ±18 V. However, the supplies must not be symmetrical. Less common examples are V– at –3 V and V+ at 9 V, or V– at –16 V and V+ at 5 V. Any combination where the difference between V– and V+ is at least 4 V and no greater than 36 V is within the normal operating capabilities of these devices.

9 Application and Implementation

9.1 Application Information

The OPAx180-Q1 family offers excellent DC precision and AC performance. These devices operate up to 36-V supply rails and offer rail-to-rail output, ultra-low offset voltage, offset voltage drift and 2-MHz bandwidth. These features make the OPAx180-Q1 a robust, high-performance amplifier for high-voltage industrial applications.

9.2 Typical Applications

These application examples highlight a few of the circuits where the OPAx180-Q1 family can be used.

9.2.1 Bipolar ±10-V Analog Output from a Unipolar Voltage Output DAC

This design is used for conditioning a unipolar digital-to-analog converter (DAC) into an accurate bipolar signal source using the OPAx180-Q1 family and three resistors. The circuit is designed with reactive load stability in mind, and is compensated to drive nearly any conventional capacitive load associated with long cable lengths.

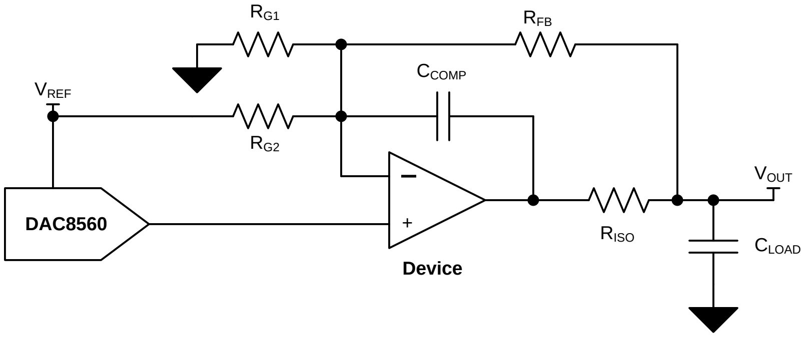


Figure 30. Circuit Schematic

9.2.1.1 Design Requirements

The design requirements are as follows:

- DAC Supply Voltage: 5-V DC
- Amplifier Supply Voltage: ±15-V DC
- Input: 3-Wire, 24-Bit SPI
- Output: ±10-V DC

Typical Applications (continued)

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Component Selection

DAC: For convenience, devices with an external reference option or devices with accessible internal references are desirable in this application because the reference creates an offset. The DAC selection in this design must primarily be based on DC error contributions typically described by offset error, gain error, and integral nonlinearity error. Occasionally, additional specifications are provided that summarize end-point errors of the DAC typically called zero-code and full-scale errors. For AC applications, slew rate and settling time may require additional consideration.

Amplifier: Amplifier input offset voltage (V_{IO}) is a key consideration for this design. V_{IO} of an operational amplifier is a typical data sheet specification, but in-circuit performance is affected by drift over temperature, the common-mode rejection ratio (CMRR), and power-supply rejection ratio (PSRR). Consideration must be given to these parameters. For AC operation, additional considerations must be made for slew rate and settling time. Input bias current (I_{IB}) is also a factor, but typically the resistor network is implemented with sufficiently small resistor values that the effects of input bias current are negligible.

Passive: Resistor matching for the op-amp resistor network is critical for the success of this design; components with tight tolerances must be selected. For this design, 0.1% resistor values are implemented, but this constraint may be adjusted based on application-specific design goals. Resistor matching contributes to offset error and gain error in this design; see *Bipolar ±10V Analog Output from a Unipolar Voltage Output DAC* for further details. The tolerance of the $R_{ISO}$and C_{COMP} stability components is not critical, and 1% components are acceptable.

9.2.1.3 Application Curves

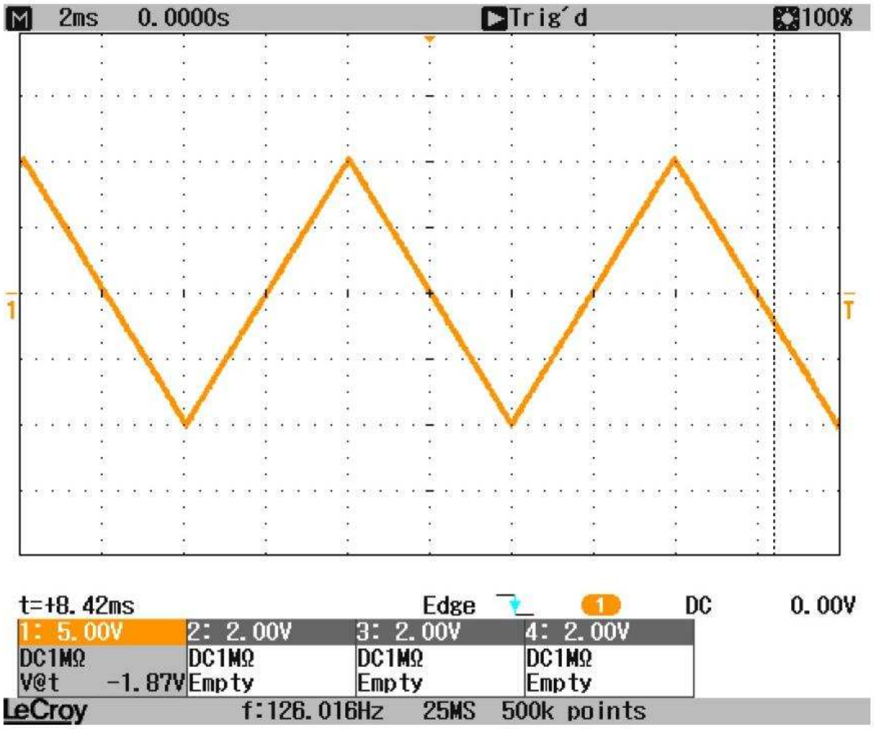


Figure 31. Full-Scale Output Waveform

Typical Applications (continued)

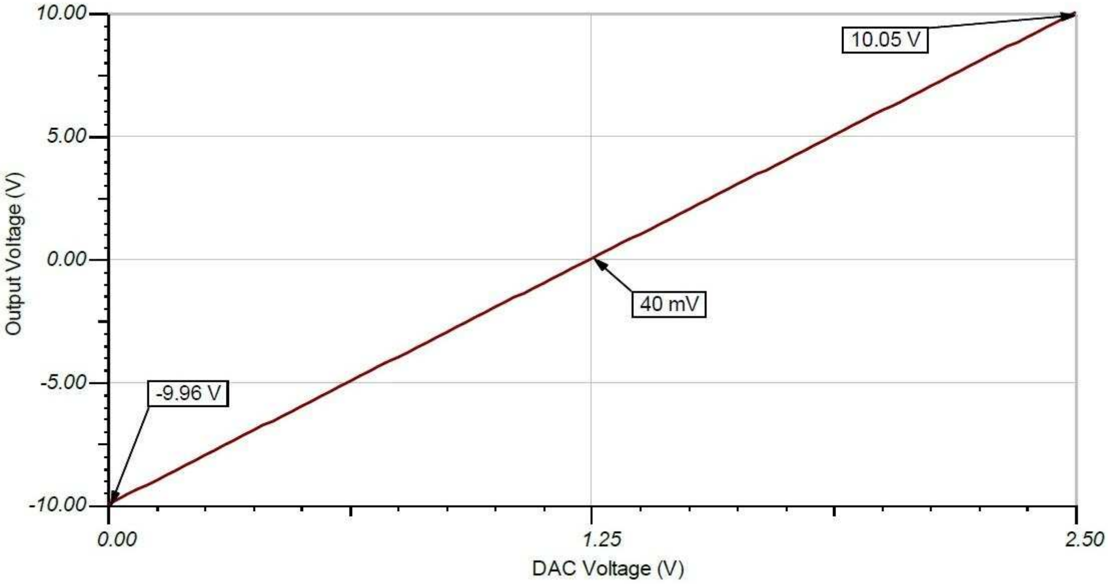


Figure 32. DC Transfer Characteristic

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, refer to TI Precision Design TIPD125, *Bipolar ±10V Analog Output from a Unipolar Voltage Output DAC*

9.2.2 Discrete INA + Attenuation

The OPAx180-Q1 family can be used as a high-voltage, high-impedance front-end for a precision, discrete instrumentation amplifier with attenuation. The INA159 in Figure 33 provides the attenuation that allows this circuit to simply interface with 3.3-V or 5-V analog-to-digital converters (ADCs).

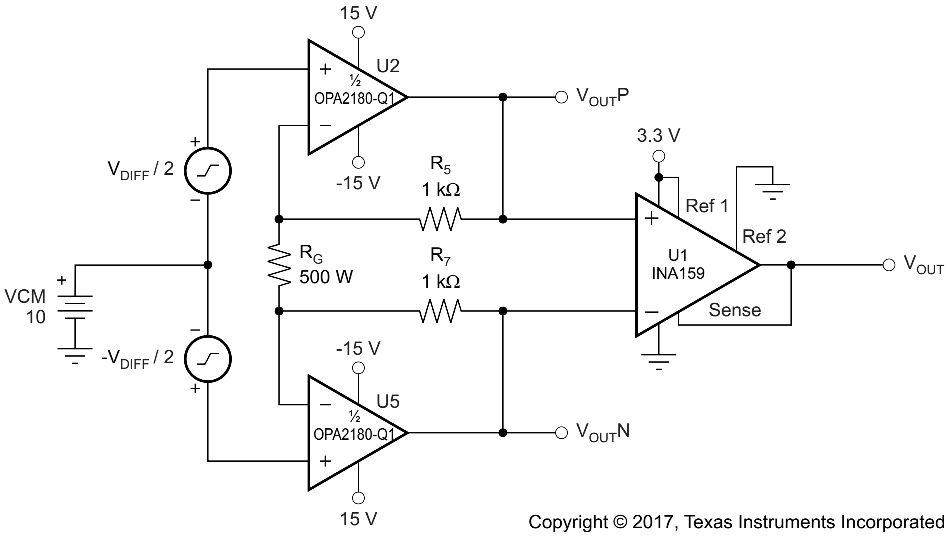
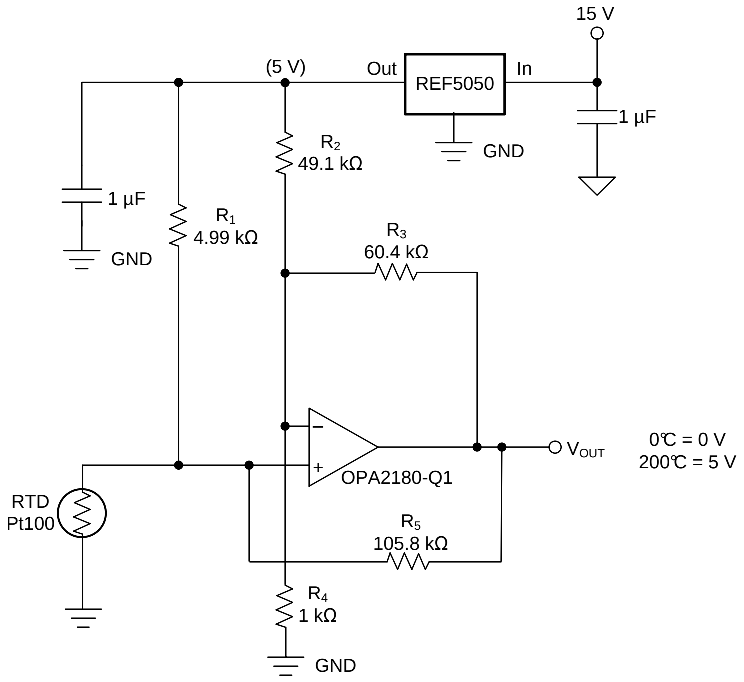


Figure 33. Discrete INA + Attenuation for ADC With a 3.3-V Supply

9.2.3 RTD Amplifier

The OPAx180-Q1 is excellent for use in analog linearization of resistance temperature detectors (RTDs). The circuit below (Figure 34) combines the precision of the OPAx180-Q1 amplifier and the precision reference of the REF5050 to linearize a Pt100 RTD.



(1) R_5 provides positive-varying excitation to linearize output.

Figure 34. RTD Amplifier with Linearization

10 Power Supply Recommendations

The OPAx180-Q1 family is specified for operation from 4 V to 36 V (±2 V to ±18 V); many specifications apply from –40°C to +105°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in *Layout*

CAUTION

Supply voltages larger than 40 V can permanently damage the device; see the *Absolute Maximum Ratings*.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see *Layout* .

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are typically devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep the input traces separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in Figure 35, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Example

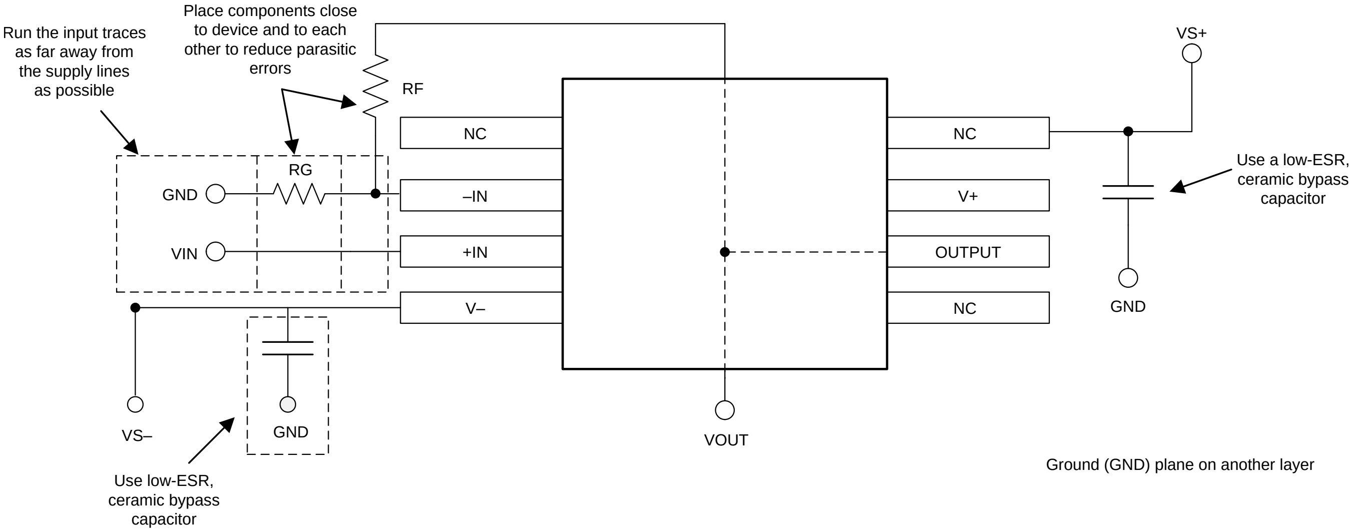


Figure 35. Operational Amplifier Board Layout for Noninverting Configuration

12 Device and Documentation Support

12.1 Related Links

Table 3 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
OPA180-Q1	Click here	Click here	Click here	Click here	Click here
OPA2180-Q1	Click here	Click here	Click here	Click here	Click here

12.2 Trademarks

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA180QDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	180	Samples
OPA2180QDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	2180	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF OPA180-Q1, OPA2180-Q1 :

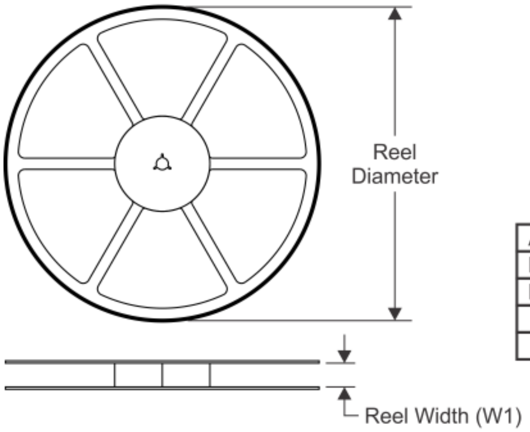
- Catalog: OPA180, OPA2180

NOTE: Qualified Version Definitions:

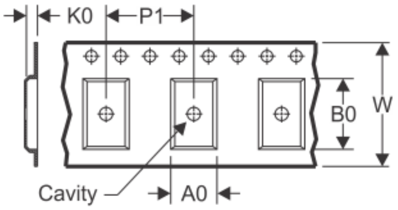
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

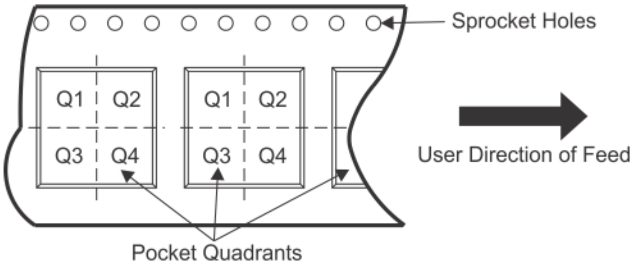


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

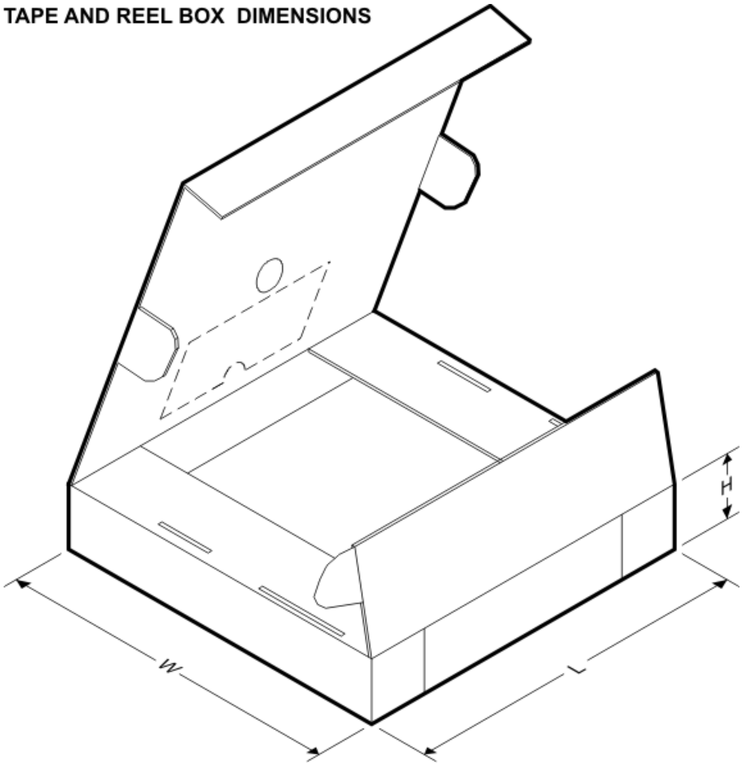
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA180QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2180QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

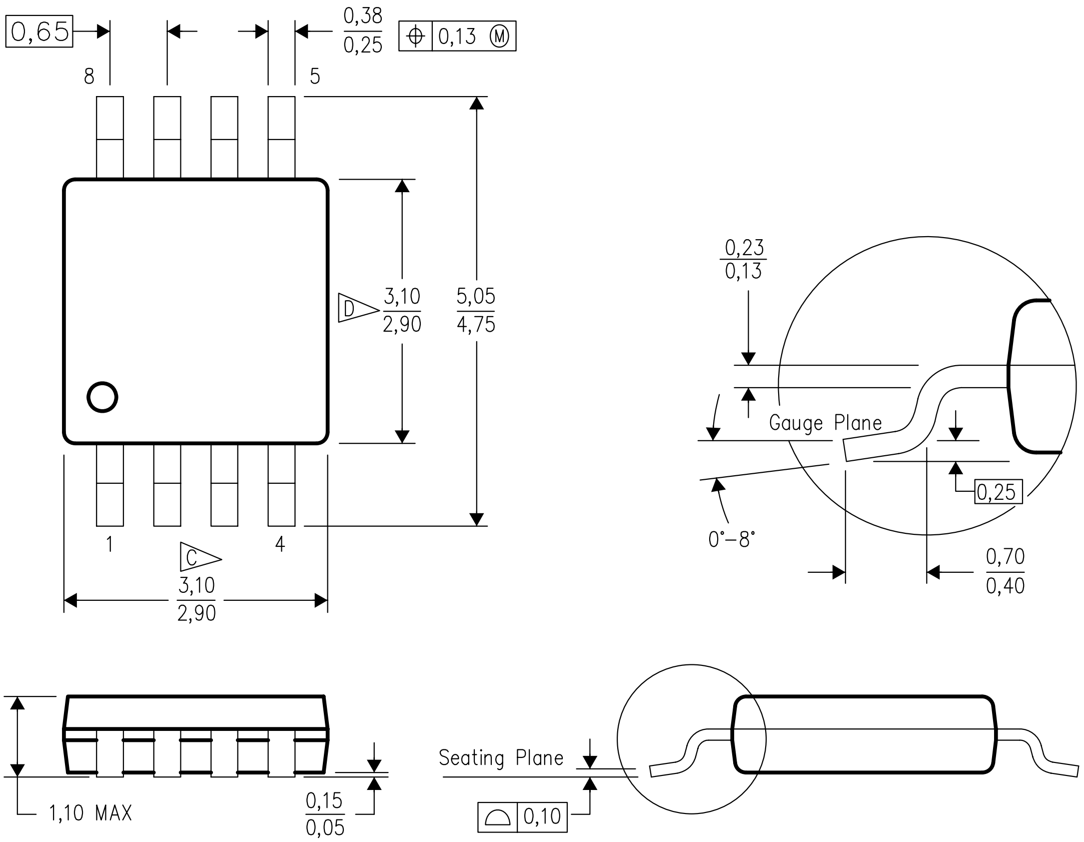
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA180QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2180QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0

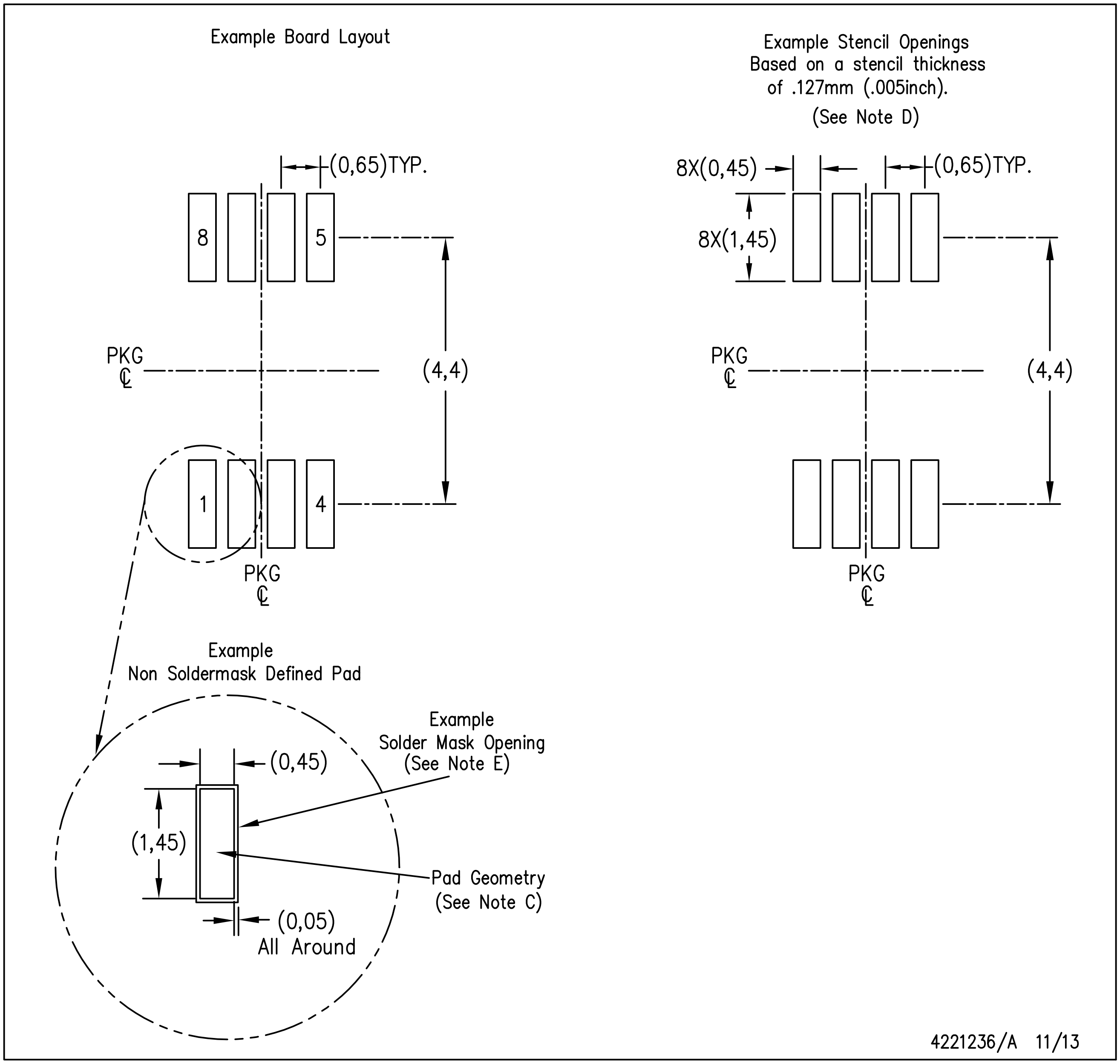
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S-PDSO-G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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