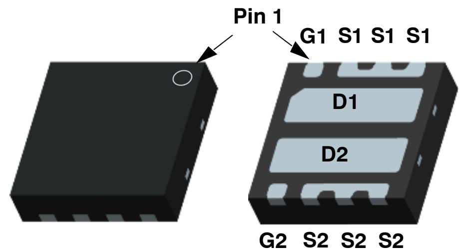
MOSFET – Dual, N-Channel, Logic Level, POWERTRENCH®

40 V, 12 A, 8.2 mΩ

FDMC9430L-F085



WDFN8
3x3, 0.65P
CASE 511DG

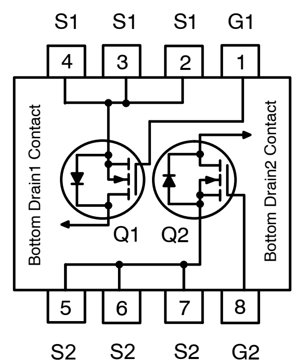
Features

- Typical $R_{DS(on)} = 6.3\ m\Omega$ at $V_{GS} = 10\ V$, $I_D = 12\ A$
- Typical $Q_{g(tot)} = 15\ nC$ at $V_{GS} = 10\ V$, $I_D = 12\ A$
- UIS Capability
- This Device is Pb−Free, Halide Free and RoHS Compliant
- AEC Qualified AEC−Q101

Applications

- Battery Protection
- Load Switching
- Point of Load

PIN ASSIGNMENT



Dual N−Channel MOSFET

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DSS}	Drain−to−Source Voltage	40	V
V_{GS}	Gate−to−Source Voltage	±12	V
I_D	Drain Current – Continuous (V_{GS} = 10) (Note 1) T_C = 25°C	12	A
	Pulsed Drain Current T_C = 25°C	See Figure 4	
E_{AS}	Single Pulse Avalanche Energy (Note 2)	21.6	mJ
P_D	Power Dissipation	11.4	W
	Derate Above 25°C	0.1	W/°C
T_J, T_{stg}	Operating and Storage Temperature	−55 to +150	°C
$R_{\theta JC}$	Thermal Resistance, Junction−to−Case	13	°C/W
$R_{\theta JA}$	Maximum Thermal Resistance, Junction−to−Ambient (Note 3)	65	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Current is limited by bondwire configuration.
2. Starting T_J = 25°C, L = 0.3 mH, I_{AS} = 12 A, V_{DD} = 40 V during inductor charging and V_{DD} = 0 V during time in avalanche.
3. $R_{\theta JA}$ is the sum of the junction−to−case and case−to−ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in^2 pad of 2 oz copper.

MARKING DIAGRAM

XXXX
AYWW▪
▪

XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
FDMC9430L−F085	WDFN8 (Pb−Free, Halide Free)	3000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
B_{VDSS}	Drain−to−Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V		40	–	–	V
I_{DSS}	Drain−to−Source Leakage Current	V_{DS} = 40 V, V_{GS} = 0 V	T_J = 25°C	–	–	1	μA
			T_J = 150°C (Note 4)	–	–	0.2	mA
I_{GSS}	Gate−to−Source Leakage Current	V_{GS} = ±12 V		–	–	±100	nA
ON CHARACTERISTICS							
$V_{GS(th)}$	Gate−to−Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA		1	1.8	3	V
$R_{DS(on)}$	Drain−to−Source On Resistance	I_D = 10 A, V_{GS} = 4.5 V		–	8.9	11.5	mΩ
		I_D = 12 A, V_{GS} = 10 V	T_J = 25°C	–	6.3	8.0	
			T_J = 150°C (Note 4)	–	10.2	13.0	
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz		–	984	–	pF
C_{oss}	Output Capacitance			–	315	–	
C_{rss}	Reverse Transfer Capacitance			–	18	–	
R_g	Gate Resistance	V_{GS} = 0.5 V, f = 1 MHz		–	1.1	–	Ω
$Q_{g(ToT)}$	Total Gate Charge	V_{GS} = 0 to 10 V	V_{DD} = 32 V, I_D = 12 A	–	15	22	nC
$Q_{g(th)}$	Threshold Gate Charge	V_{GS} = 0 to 1 V		–	0.9	–	
Q_{gs}	Gate−to−Source Gate Charge			–	2.6	–	
Q_{gd}	Gate−to−Drain “Miller” Charge			–	2.1	–	
SWITCHING CHARACTERISTICS							
t_{on}	Turn−On Time	V_{DD} = 20 V, I_D = 12 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		–	–	13	ns
$t_{d(on)}$	Turn−On Delay			–	7	–	
t_r	Rise Time			–	2	–	
$t_{d(off)}$	Turn−Off Delay			–	17	–	
t_f	Fall Time			–	2	–	
t_{off}	Turn−Off Time			–	–	28	
DRAIN−SOURCE DIODE CHARACTERISTICS							
V_{SD}	Source−to−Drain Diode Voltage	I_{SD} = 12 A, V_{GS} = 0 V		–	–	1.2	V
		I_{SD} = 6 A, V_{GS} = 0 V		–	–	1.1	
t_{rr}	Reverse−Recovery Time	V_{DD} = 32 V, I_F = 12 A, dI_{SD}/dt = 100 A/μs		–	32	48	ns
Q_{rr}	Reverse−Recovery Charge			–	16	24	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The maximum value is specified by design at T_J = 150°C. Product is not tested to this condition in production.

TYPICAL CHARACTERISTICS

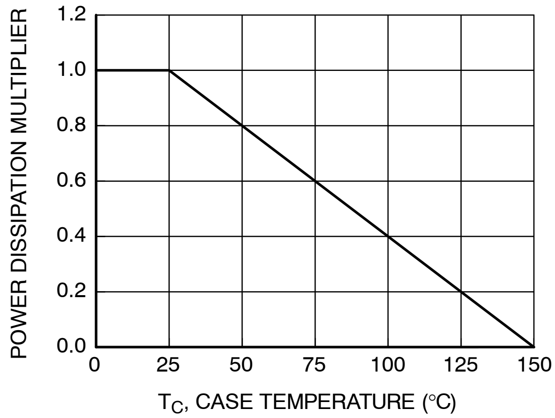


Figure 1. Normalized Power Dissipation vs. Case Temperature

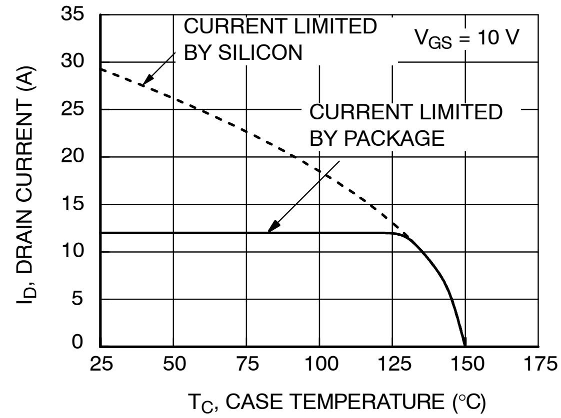


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

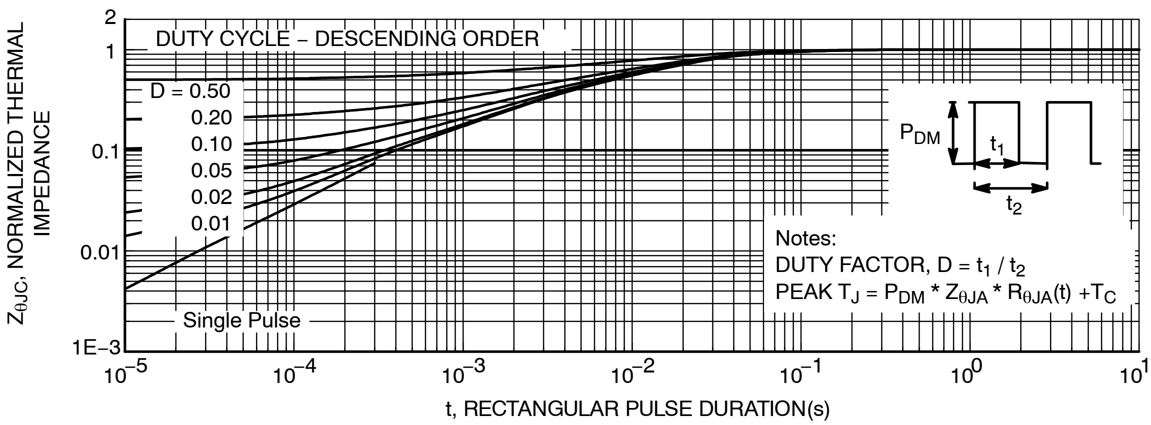


Figure 3. Normalized Maximum Transient Thermal Impedance

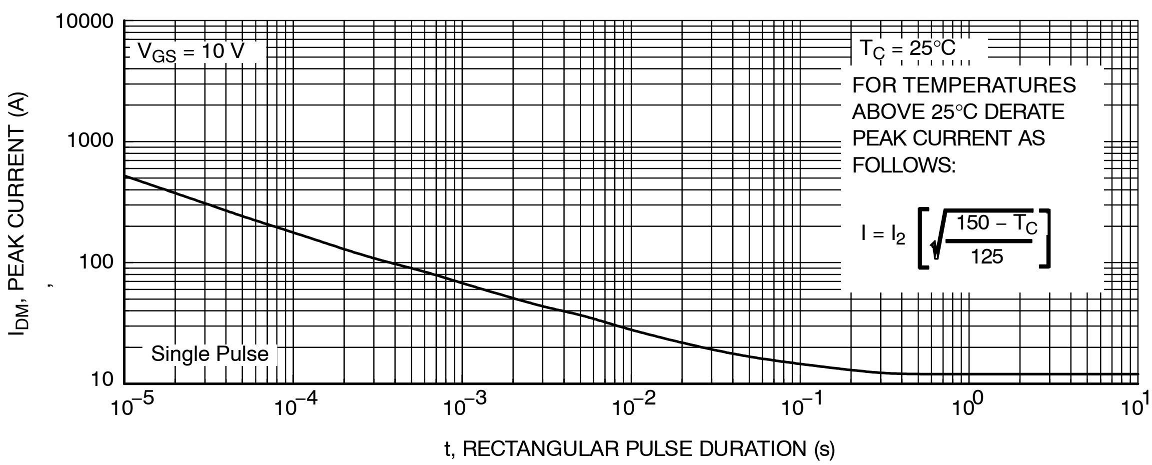


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS

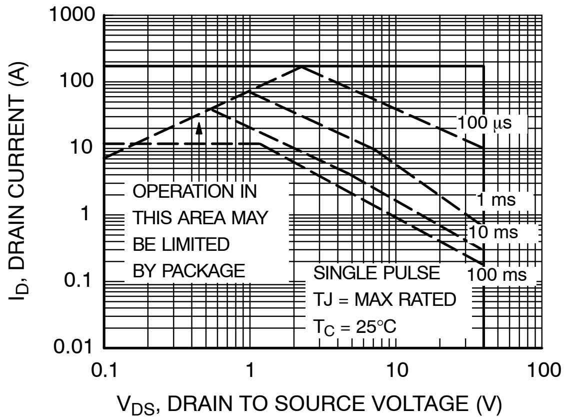
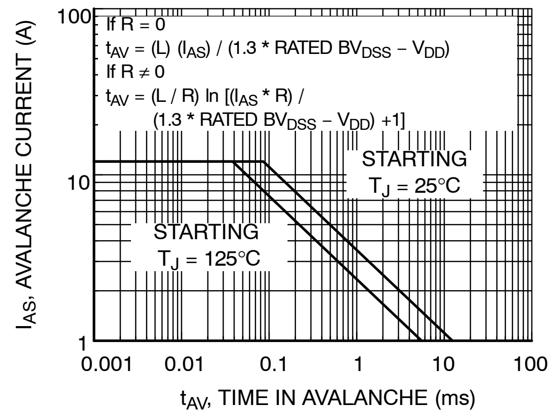


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to **onsemi** Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

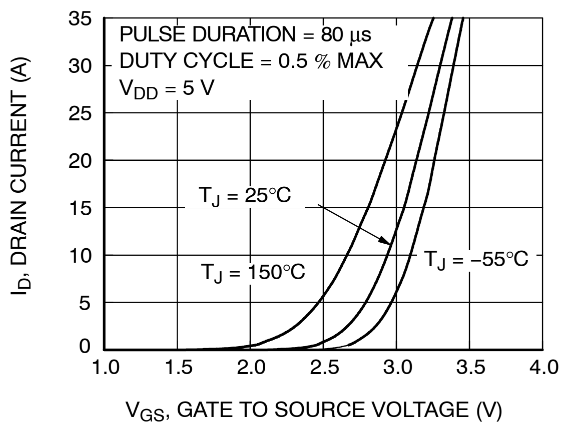


Figure 7. Transfer Characteristics

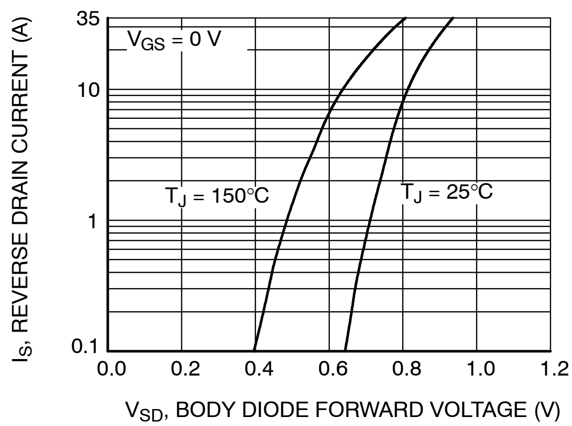


Figure 8. Forward Diode Characteristics

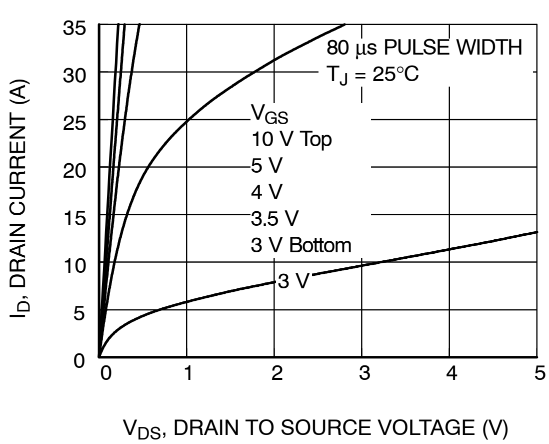


Figure 9. Saturation Characteristics

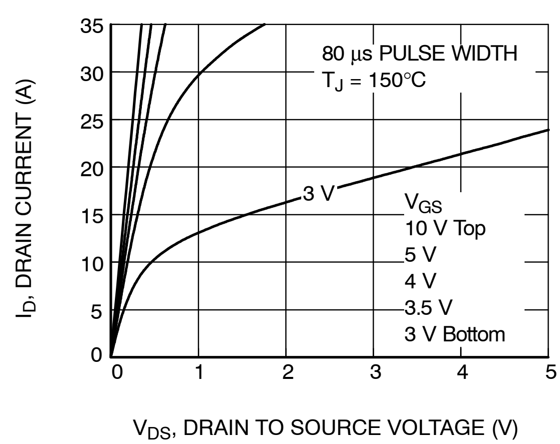


Figure 10. Saturation Characteristics

TYPICAL CHARACTERISTICS

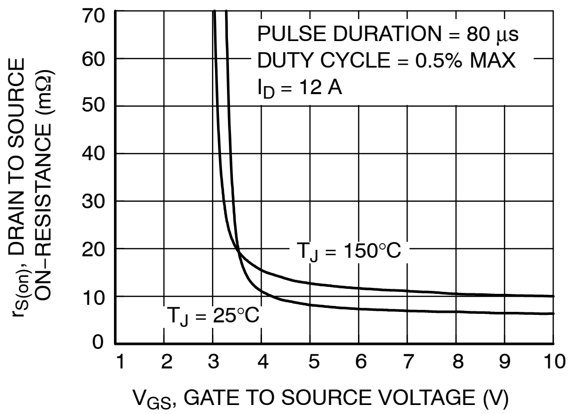


Figure 11. $R_{DS(on)}$ vs. Gate Voltage

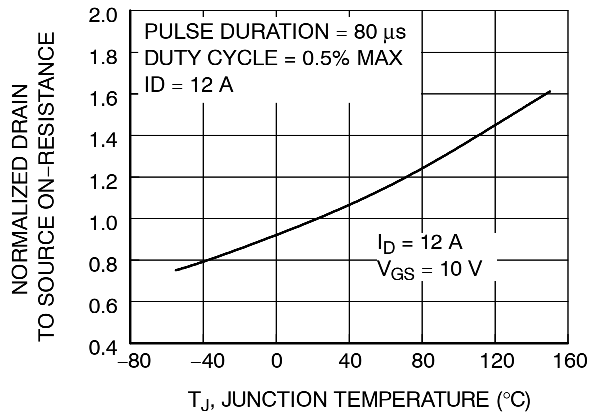


Figure 12. Normalized $R_{DS(on)}$ vs. Junction Temperature

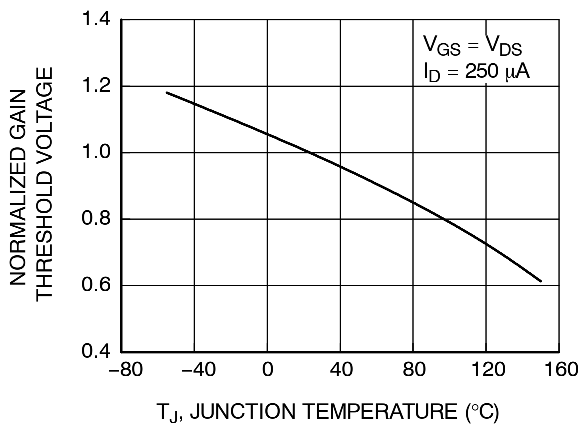


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

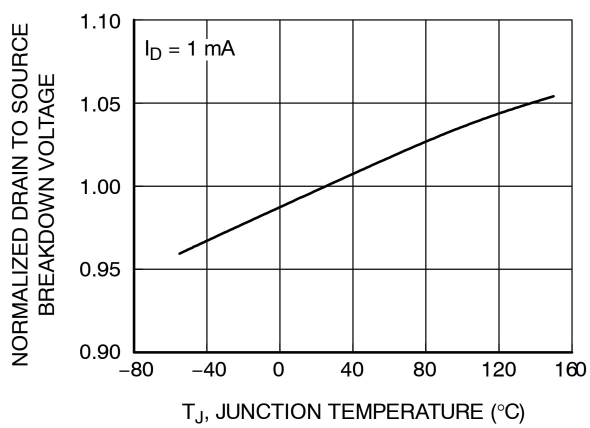


Figure 14. Normalized Drain−to−Source Breakdown Voltage vs. Junction Temperature

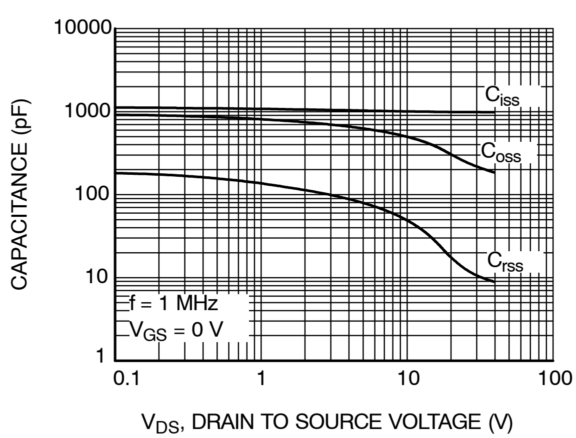


Figure 15. Capacitance vs. Drain−to−Source Voltage

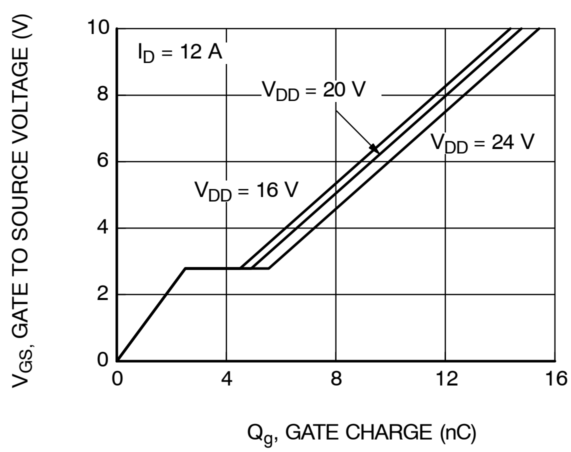
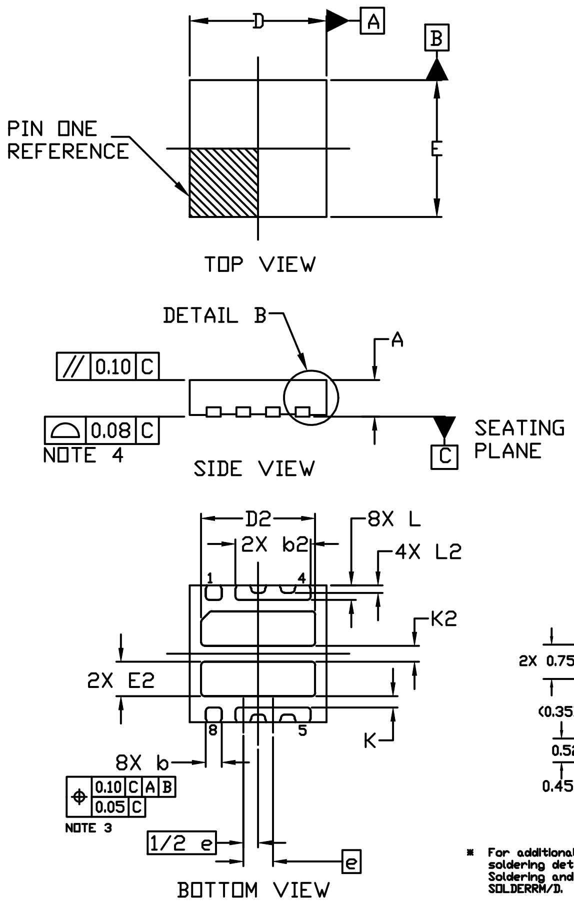
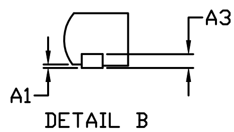


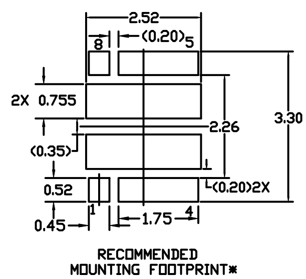
Figure 16. Gate Charge vs. Gate−to−Source Voltage

WDFN8 3x3, 0.65P
CASE 511DG
ISSUE A

DATE 12 FEB 2019







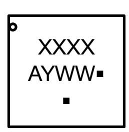
* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	---	0.05
A3	0.20 REF		
b	0.30	0.35	0.40
b2	1.65 REF		
D	2.90	3.00	3.10
D2	2.45	2.50	2.55
E	2.90	3.00	3.10
E2	1.40	1.50	1.60
e	0.65 BSC		
K	0.25	---	---
K2	0.35 REF		
L	0.27	0.32	0.37
L2	0.163 REF		

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**WDFN8 3x3, 0.65P**	**PAGE 1 OF 1**

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