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# **Motherboard Power Conversion Solutions Using the HIP6020 and HIP6021 Controller ICs**

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**AN9836**

### **Introduction**

The rapidly changing desktop motherboard architecture for core processor and Accelerated Graphics Port (AGP) voltages demand innovative power conversion solutions. The HIP6020 [1] and HIP6021 [2] controllers provide a bridge over these challenging power concerns. This document describes the HIP6020EVAL1 and HIP6021EVAL1 reference designs, features, and usage guidelines.



**FIGURE 1. HIP6020/21EVAL1 BLOCK DIAGRAM**

Figure 1 presents a simple block diagram of the HIP6020/21 application circuit. The +3.3V, +5V, and +12V power inputs are provided by an ATX power supply. The HIP6020 [1] and HIP6021 [2] both monitor and regulate four output voltages. Both provide a synchronous-rectified buck converter controller which regulates the microprocessor core voltage (VCC\_CORE) to a level programmed by a 5-bit digital code. As well as, two adjustable linear controllers which drive external MOSFETs to supply the 1.5V GTL bus voltage (VCC\_VTT) and 1.8V North/South Bridge core voltage (VCC\_MCH) and/or cache memory. The linear regulators use the 3.3V from the ATX for their input voltage to minimize the power dissipated.

For high performance AGP systems, the HIP6020EVAL1 monitors and controls a standard buck converter to regulate the 1.5V or 3.3V Universal AGP Card bus voltage (VCC\_VDDQ). While the HIP6021EVAL1 addresses the lower performance AGP systems with a third integrated adjustable linear controller to regulate the 1.5V or 3.3V AGP core voltage.



**FIGURE 2. QUICK START EVALUATION CONNECTIONS**

The HIP6020/21 EVAL1 circuit board shows the layout and traces of the power supply portion of a computer motherboard. Included on the boards are the ATX input power connector and a Pentium II, SLOT 1 connector. Motherboard designers should reference the component placement and printed circuit routing of the specific circuit board. Both circuit boards contain jumpers and spare component placeholders to facilitate detailed evaluation of the HIP6020 or HIP6021.

## **Quick Start Evaluation**

Both evaluation platforms support testing with standard power supplies or an ATX-style power supply. Simply connect the ATX supply to J2 connector, see Figure 2, or connect standard laboratory supplies to the related posts marked +12VIN, +5VIN, +3.3VIN and GND. No power-up sequence is required when using standard laboratory power supplies.

The outputs can be exercised using either resistive loads, electronic loads, or the Intel Slot 1 EMT tool. Shielded scope probe test points (TP2, TP5, TP6 and TP8) on the outputs (VCC\_VDDQ, VCC\_CORE, VCC\_VTT and VCC\_MCH) allow for accurate inspection of the output power quality. Before proceeding, please consult Table 1 for the evaluation board's design envelope characteristics.



**TABLE 1. HIP6020/21EVAL1 OUTPUT LOAD CAPABILITIES**

When using the Intel Slot 1 EMT Tool, note that the core regulator VID jumpers (JP0-JP4) located on the evaluation board are in parallel with the ones located on the EMT tool. Remember to de-populate one set of jumpers completely and use the other set to dial-in the desired output voltage.

### **HIP6020/21EVAL1 Reference Designs**

The evaluation board is designed to simultaneously meet all the applicable criteria outlined in Table 1. The following section highlights some of the most important features of this system power solution.

#### **ATX Power Supply Control Interface**

JP7 allows control of the ATX power supply. Placing the jumper in the 1-2 position, connects the PS-ON (output enable) input of the ATX supply to ground, thus unconditionally enabling the outputs. Placing the jumper in the 2-3 position enables automatic control of the ATX. When ATX supply turns on, the 5V stand-by output turns Q6A on to enable the main ATX outputs. When FAULT/RT pin goes high, Q6B latches on, thus turning off Q6A and disabling the ATX outputs. Cycling power off and then back on re-enables the ATX power supply. The sole purpose of this circuit is to exemplify a possible interface between the control circuit's FAULT output and an ATX power supply.



**FIGURE 3. ATX POWER SUPPLY CONTROL CIRCUIT**

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### **Lossless Output Voltage Droop with Load**

The synchronous switching regulator on the HIP6020/21EVAL1 board implements output voltage droop functions, where the output voltage sags proportionately with the output current. Although not necessary for proper circuit operation, this method takes advantage of the static regulation limits to improve the dynamic regulation by expanding the available headroom for transient edge output excursion. In such practical applications, compared to a nondroop implementation, this translates to fewer output capacitors or better regulation for the same type and number of capacitors. Figure 4 details the output voltage characteristics of a converter with 3.0% droop compared to a non-droop implementation.



**FIGURE 4. OUTPUT VOLTAGE DROOP AT 2.0V DAC SETTING**

In contrast to droop implementation involving a resistive element placed in the output current path, this method does not involve the additional power loss introduced by the resistor. By moving the voltage regulation point ahead of the output inductor (at the PHASE node), droop becomes equal to the average voltage drop across the output inductor's DC resistance as well as any distributed resistance. To insure symmetric output voltage excursions in response to load transients, the output voltage is offset above the nominal level by half the calculated droop.

#### **Over-Current Protection**

The switching regulators within the HIP6020 and HIP6021 employ a lossless current sensing technique based on the upper MOSFETs  $r_{DS(ON)}$ . During the ON-time of the upper MOSFET, its drain-to-source voltage is compared with a user-adjustable voltage created by an internal current source across R<sub>OCSET</sub> (i.e., R2, R3 in the HIP6020EVAL1 schematic). When the MOSFETs drain-to-source voltage exceeds the preset threshold, the regulator immediately shuts down all outputs and initiates a soft-start cycle. If the condition persists, the third shutdown latches the chip off and pulls the FAULT/RT pin high. Cycling the bias voltage OFF and ON resets the protection circuitry.

The linear regulator outputs employ a different method of overcurrent detection. Given the relatively large  $r_{DS(ON)}$  of the pass devices, a short-circuit condition usually translates into a dip in the output voltage. If the output voltage (as sensed at the feedback pin) dips below approximately 75% of the set point, this undervoltage is interpreted as an overcurrent event and the control IC reacts accordingly, shutting down all outputs and cycling the soft-start.

The internal regulator is protected by an additional internal output current mirror. Output current exceeding the preset threshold (see data sheet) generates a similar response. Any over-current event on any output is reported by the toggle of the PGOOD output.

#### **Over-Voltage Protection**

The microprocessor core regulator (synchronous buck) has a voltage-tracking over-voltage threshold set at 115% (typically) of the DAC setting. In the case of an over-voltage event, the microprocessor core regulator attempts to regulate the output voltage at the over-voltage threshold. It also reports the condition through a high output on the FAULT/RT pin.

In addition to the normal over-voltage operation, the microprocessor core regulator has another very useful protection feature presented in Figures 5 and 6. In case of a power-up sequence with a shorted upper MOSFET, the microprocessor can be destroyed without the protective circuitry integrated into the HIP6020/21. An independent functional block acts upon the lower gate driver, regulating the core voltage to around 1.3V until the controller bias voltage reaches power-on threshold. At this point normal operation resumes, core voltage is regulated to 115% of the DAC setting (2.0V in this case), and fault condition is reported on the FAULT/RT pin.

Figure 5 exemplifies operation of the evaluation board without the help of the ATX supply control circuit (Figure 3). Initially the core voltage is held around 1.3V until the poweron threshold is reached (15ms till 50ms). Then the output voltage is released to rise up to 115% of the DAC setting (DAC = 2.0V). FAULT/RT goes high at this time signaling an over-voltage condition. About 20ms later the 15A fuse (F1)

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blows due to the magnitude of the surge current being drawn from the 5V input supply. Proper operation of this protection feature is contingent, however, on the 12V bias voltage being sufficiently high to turn on the lower MOSFET. The circuit has been tested with several ATX supplies, and they all produced acceptable bias voltage for the operation of the protection circuitry and the on-board UltraFET MOSFETs.

Figure 6 depicts the same start-up scenario, this time with the ATX supply control interface enabled. As seen in the oscilloscope capture, as soon as power-on reset (POR) thresholds are detected, the HIP6020/21 detects the overvoltage condition and reports it on the FAULT/RT pin. In turn, the control circuit shuts down the ATX supply by generating a logic high at the PS-ON input, before any expensive damage can occur.



**FIGURE 5. START-UP SEQUENCE WITH SHORTED Q1 (ATX CONTROL CIRCUIT BY-PASSED)**





#### **Printed Circuit Board**

The practical implementation of the circuit is done on a twoounce four-layer printed circuit board. The two internal layers are dedicated for ground and power planes. The layout is compact and several additional footprints are provided for increased evaluation flexibility. The component side of the board contains two embedded serpentine resistors. One in series with the drain of Q4 and Q5, approximately 220mΩ and 200mΩ respectively. These resistors is not necessary for the proper operation of the circuit; their role is simply to share the power dissipation which otherwise would be dissipated entirely by Q4 or Q5. Both serpentine resistors can be removed by shorted them via two separate footprints on the bottom of the EVAL boards. Contact Intersil for board layout Gerber files.

#### **Power MOSFETs**

The power transistors utilized by HIP6020/21EVAL1 belong to Intersil' newest line of 30V UltraFET MOSFETs. Featuring reduced  $r_{DS(ON)}$  and low  $t_{rr}$  and  $Q_{rr}$ , these transistors allow for elimination of the traditional lower MOSFET anti-parallel schottky.

### **HIP6020/21EVAL1 Performance**

#### **Efficiency**

Figure 7 displays the efficiency of the HIP6021EVAL1 core regulator reference design versus load current. Laboratory measurements were made with a 5V input and 100 linear feet per minute (LFM) of airflow across the evaluation board. The linear regulators are neglected since their efficiency is not a figure of merit for the application circuit.



Similarly, Figure 8 displays the efficiency obtained in the HIP6020EVAL1 reference design. Since this evaluation platform contains two switching regulators, both switching regulator outputs were simultaneously loaded and measured. The efficiency curve in Figure 8 represents a composite result of the overall circuit efficiency plotted against total converter output power. For those interested in

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only the core regulator efficiency, use Figure 7. The core regulator design of the HIP6020 is identical to that of the HIP6021.



**EFFICIENCY**

#### **Load Transient Response**

HIP6020EVAL1 response of the core voltage regulation to a 13.5A output step load transient is shown in Figure 9. An Intel Slot 1 Test Tool provided the load transient which was larger than the 9.5A design point. All other outputs are subjected to the maximum transient loading conditions and nominal output voltage settings as described in Table 1.



**FIGURE 9. HIP6020EVAL1 OUTPUT TRANSIENT RESPONSE**

### **HIP6020/21EVAL1 Modifications**

#### **Input Capacitors Selection**

In a DC/DC converter employing an input inductor, the input RMS current is supplied entirely by the input capacitors. The number of input capacitors is usually determined by their maximum RMS current rating. The voltage rating at maximum ambient temperature of the input capacitors

should be at least 1.25 to 1.5 times the maximum input voltage. High frequency decoupling (highly recommended) is implemented through the use of ceramic capacitors in parallel with the bulk aluminum capacitor filtering. The switching converter's input RMS current is dependent on the input and output voltages as well as the output current. Figure 10 shows this approximate relationships for five different levels of current. Based on the linearity of the relationship, the graph results can be interpolated for additional levels of output current. For output voltages ranging from 2 to 3 volts, a good approximation of the input RMS current is 1/2 the output current.



**FIGURE 10. SWITCHING CONVERTER RMS INPUT CURRENT**

Using the above graph and the capacitor RMS current rating, a minimum number of input capacitors can be easily determined. If the time-averaged load is different than the maximum load, the number of input capacitors may be cautiously scaled down.

#### **Output Voltages**

The synchronous buck converter supplying the microprocessor core voltage is controlled by the internal DAC. Output voltage can be adjusted by selecting the appropriate VID jumper combination. For more information please refer to the HIP6020 or HIP6021 data sheet which contains a very comprehensive table detailing all the VID combinations and the resultant output voltages. If droop implementation is desired, the no-load output voltage can be determined from the following equation:



where  $V_{\text{DAC}} = \text{DAC-set output voltage target.}$ 

The AGP bus voltage is controlled by the SELECT pin. A TTL low inputs sets the internal resistor dividers for 1.5V output and a TTL high sets the AGP output to 3.3V. Leaving

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out JP5 will allow the internal pullup to hold the SELECT pin at a TTL high.

The HIP6020 linear controller outputs (VCC\_VTT and VCC\_MCH) are set by internal resistor dividers to 1.5V and 1.8V respectively. The output levels can be increased by adding external resistors to the VSEN lines per the following equations:

$$
V_{VCC-VTT} = 1.5V P (1 + \frac{R8}{R9})
$$
  
 $V_{VCC-MCH} = 1.8V P (1 + \frac{R10}{R11})$ 

Note that the resistor values used should be no more than 5kΩ in total value. If this is not met, the internal resistor values will induce some degree of offset in the output voltages.

The HIP6021 gives the user the option to override the internal resistors and adjust the output voltage based on the chip's internal bandgap voltage reference. By grounding the FIX pin (pin 2), simple resistor value changes allow for outputs as low as 1.3V or as high as the input voltage. The steady-state DC output voltages can be set using the following equations:

$$
V_{VCC-VTT} = V_{REF} P (1 + \frac{R9}{R10})
$$

 $V_{REF}$  = HIP6021 internal reference voltage (typically 1.267V)

$$
V_{VCC-CLK} = V_{REF} P \left( 1 + \frac{R11}{R12} \right), \text{where}
$$

Left open, the FIX pin is pulled high internally and the fixed 1.5V and 1.8V outputs are enabled.

### **Conclusion**

The HIP6020/21EVAL1 board lends itself to a wide variety of high-power DC-DC microprocessor converter designs. The built-in flexibility allows the designer to quickly modify for applications with various requirements, the printed circuit board being laid out to accommodate the necessary components for operation at currents up to 19A.

### **References**

For Intersil documents available on the web, see http://www.intersil.com/

- [1] HIP6020 Data Sheet, Intersil Corporation, FN4683
- [2] HIP6021 Data Sheet, Intersil Corporation, FN4684
- [3] Slot 1 Test Kit, Intel # EUCDSLOTKIT1

**HIP6020EVAL1 Schematic**



### **HIP6021EVAL1 Schematic**



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## **Bill of Materials for HIP6020EVAL1**



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## **Bill of Materials for HIP6020EVAL1 (Continued)**



## **Bill of Materials for HIP6021EVAL1**



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## **Bill of Materials for HIP6021EVAL1 (Continued)**



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