

August 1991

Features

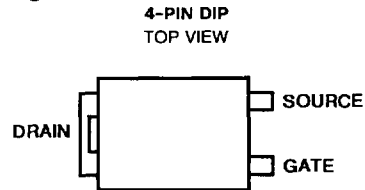
- 1.3A and 1.1A, 80V - 100V
- $r_{DS(on)} = 0.30\Omega$ and 0.40Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Description

The IRFD120, IRFD121, IRFD122, and IRFD123 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRFD120R, IRFD121R, IRFD122R, and IRFD123R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

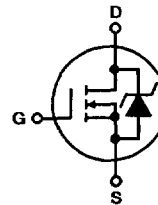
The IRFD types are supplied in the 4-pin dual-in-line plastic package.

Package



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^\circ\text{C}$), Unless Otherwise Specified

	IRFD120 IRFD120R	IRFD121 IRFD121R	IRFD122 IRFD122R	IRFD123 IRFD123R	UNITS
Drain-Source Voltage (1)	100	80	100	80	V
Drain-Gate Voltage ($R_{GS} = 20k\Omega$) (1)	100	80	100	80	V
Continuous Drain Current					
$T_C = +25^\circ\text{C}$	1.3	1.3	1.1	1.1	A
Pulsed Drain Current	5.2	5.2	4.4	4.4	A
Gate-Source Voltage	± 20	± 20	± 20	± 20	V
Maximum Power Dissipation					
$T_C = +25^\circ\text{C}$ (See Figure 13)	1.0	1.0	1.0	1.0	W
Linear Derating Factor (See Figure 13)	0.008	0.008	0.008	0.008	W/ $^\circ\text{C}$
Inductive Current, Clamped	5.2	5.2	4.4	4.4	A
(See Figure 14, $L = 100\mu\text{H}$)					
Single Pulse Avalanche Energy Rating (3)	36	36	36	36	mJ
Operating and Storage Junction	-55 to +150	-55 to +150	-55 to +150	-55 to +150	$^\circ\text{C}$
Temperature Range					
Maximum Lead Temperature for Soldering	300	300	300	300	$^\circ\text{C}$
(0.063" (1.6mm) from case for 10s)					

NOTES:

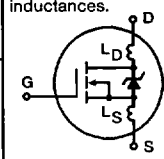
1. $T_J = +25^\circ\text{C}$ to $+150^\circ\text{C}$.

2. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.

3. $V_{DD} = 25\text{V}$, starting $T_J = +25^\circ\text{C}$, $L = 32\text{mH}$, $R_{GS} = 25\Omega$, $I_{PEAK} = 1.3\text{A}$. See Figure 15.

* R Suffix Types Only

Electrical Characteristics $T_C = +25^\circ\text{C}$, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS		
			MIN	TYP	MAX			
Drain-Source Breakdown Voltage IRFD120/122, IRFD120R/122R IRFD121/123, IRFD121R/123R	BV _{DSS}	V _{GS} = 0V, I _D = 250μA	100	-	-	V		
			80	-	-	V		
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} = V _{GS} , I _D = 250μA	2.0	-	4.0	V		
Gate-Source Leakage Forward	I _{GSS}	V _{GS} = 20V	-	-	500	nA		
Gate-Source Leakage Reverse	I _{GSS}	V _{GS} = -20V	-	-	-500	nA		
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = Max Rating, V _{GS} = 0V	-	-	250	μA		
		V _{DS} = Max Rating x 0.8, V _{GS} = 0V, T _C = +125°C	-	-	1000	μA		
On-State Drain Current (Note 2) IRFD120/121, IRFD120R/121R IRFD122/123, IRFD122R/123R	I _{D(ON)}	V _{DS} > I _{D(ON)} x r _{DS(ON)} Max, V _{GS} = 10V	1.3	-	-	A		
			1.1	-	-	A		
Static Drain-Source On-State Resistance (Note 2) IRFD120/121, IRFD120R/121R IRFD122/123, IRFD122R/123R	r _{DS(ON)}	V _{GS} = 10V, I _D = 0.6A	-	0.25	0.30	Ω		
			-	0.30	0.40	Ω		
			-	-	-	-		
Forward Transconductance (Note 2)	g _{fS}	V _{DS} > I _{D(ON)} x r _{DS(ON)} Max, I _D = 0.6A	0.9	1.0	-	S(Ω)		
Input Capacitance	C _{ISS}	V _{GS} = 0V, V _{DS} = 25V, f = 1.0MHz	-	450	-	pF		
Output Capacitance	C _{OSS}	See Figure 9	-	200	-	pF		
Reverse Transfer Capacitance	C _{RSS}		-	50	-	pF		
Turn-On Delay Time	t _{d(ON)}	V _{DD} ≈ 0.5BV _{DSS} , I _D = 1.3A, R _G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	20	40	ns		
Rise Time	t _r		-	35	70	ns		
Turn-Off Delay Time	t _{d(OFF)}		-	50	100	ns		
Fall Time	t _f		-	35	70	ns		
Total Gate Charge (Gate-Source + Gate-Drain)	Q _g	V _{GS} = 10V, I _D = 1.3A, V _{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	11	15	nC		
Gate-Source Charge	Q _{gs}		-	6.0	-	nC		
Gate-Drain ("Miller") Charge	Q _{gd}		-	5.0	-	nC		
Internal Drain Inductance	L _D	Measured from the drain lead, 2.0mm (0.08 in.) from package to center of die.			-	4.0	-	nH
Internal Source Inductance	L _S	Measured from the source lead, 2.0mm (0.08") from package to source bonding pad.			-	6.0	-	nH
Junction-to-Ambient	R _{θJA}	Free air operation	-	-	120	°C/W		

4
N-CHANNEL
POWER MOSFETS

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I _S	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.	-	-	1.3	A
Pulse Source Current (Body Diode) (Note 3)	I _{SM}		-	-	5.2	A
Diode Forward Voltage (Note 2)	V _{SD}	T _J = +25°C, I _S = 1.3A, V _{GS} = 0V	-	-	2.5	V
Reverse Recovery Time	t _{rr}	T _J = +150°C, I _F = 1.3A, dI _F /dt = 100A/μs	-	280	-	ns
Reverse Recovered Charge	Q _{RR}	T _J = +150°C, I _F = 1.3A, dI _F /dt = 100A/μs	-	1.6	-	μC
Forward Turn-on Time	t _{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .	-	-	-	-

NOTES:

1. T_J = +25°C to +150°C

2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%

3. V_{DD} = 25V, starting T_J = +25°C, L = 32mH, R_{GS} = 25Ω, I_{PEAK} = 1.3A.
(See Figure 15.)

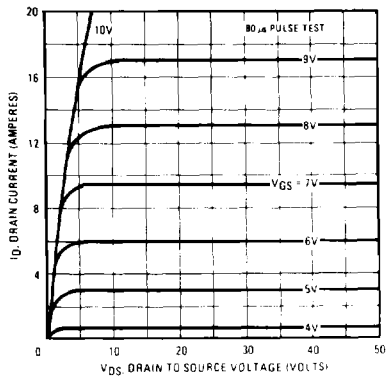


Fig. 1 - Typical Output Characteristics

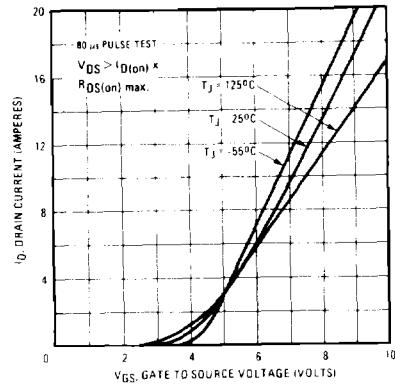


Fig. 2 - Typical Transfer Characteristics

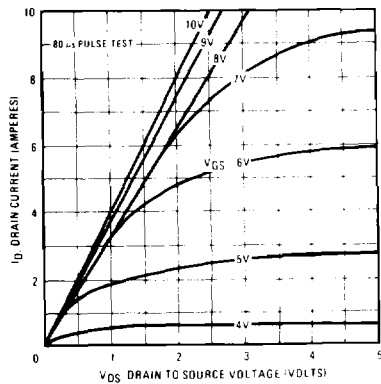


Fig. 3 - Typical Saturation Characteristics

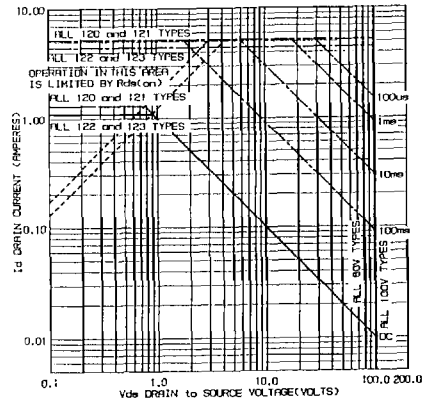


Fig. 4 - Maximum Safe Operating Area

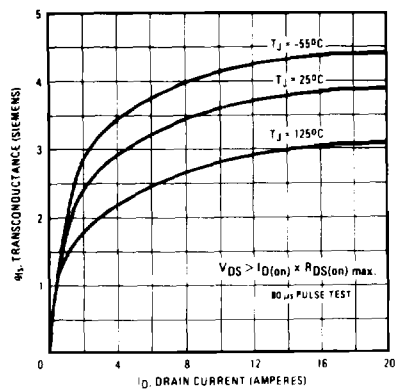


Fig. 5 - Typical Transconductance Vs. Drain Current

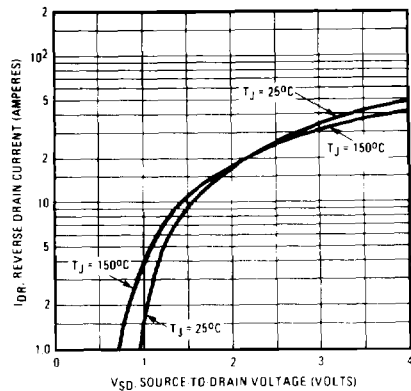


Fig. 6 - Typical Source-Drain Diode Forward Voltage

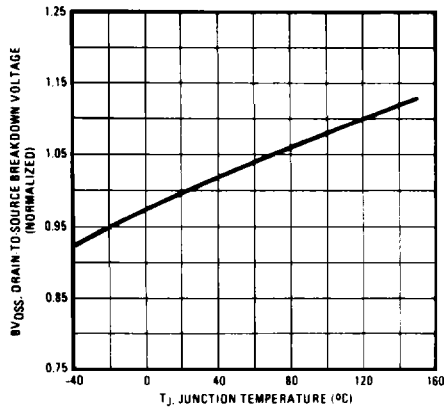


Fig. 7 - Breakdown Voltage Vs. Temperature

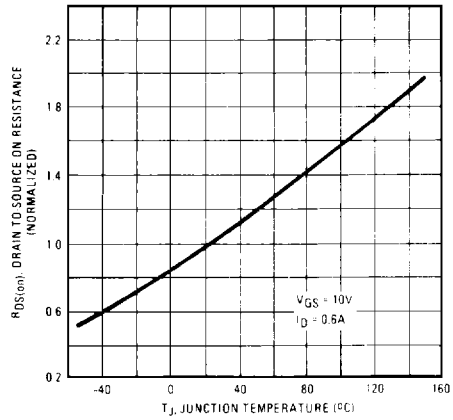


Fig. 8 - Normalized On-Resistance Vs. Temperature

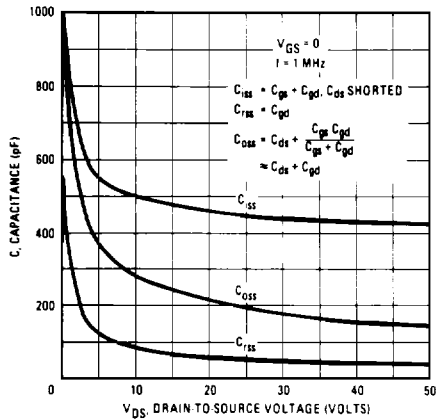


Fig. 9 - Typical Capacitance Vs. Drain-to-Source Voltage

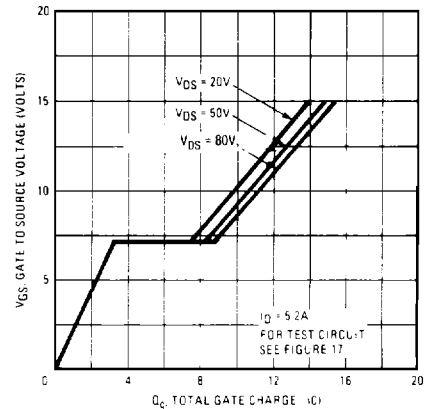


Fig. 10 - Typical Gate Charge Vs. Gate-to-Source Voltage

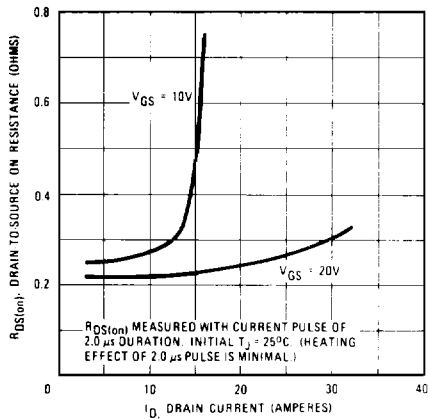


Fig. 11 - Typical On-Resistance Vs. Drain Current

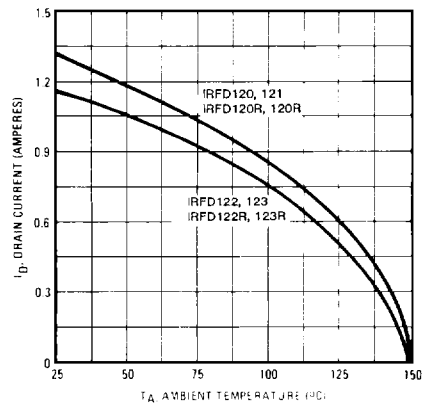


Fig. 12 - Maximum Drain Current Vs. Case Temperature

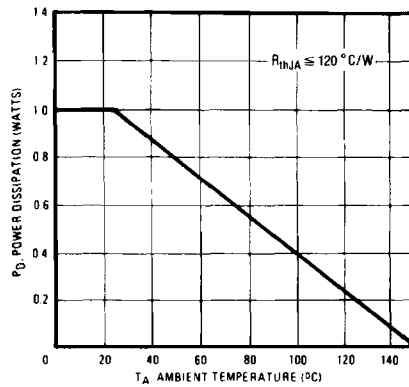


Fig. 13 - Power Vs. Temperature Derating Curve

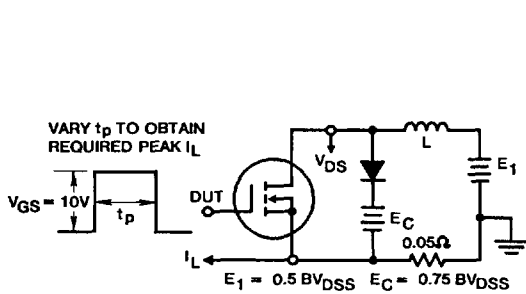


Fig. 14a - Clamped Inductive Test Circuit

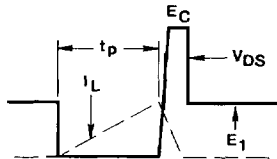


Fig. 14b - Clamped Inductive Waveforms

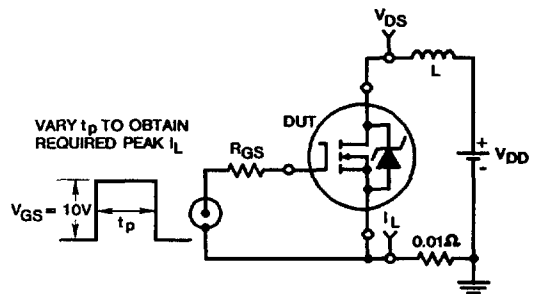


Fig. 15a - Unclamped Energy Test Circuit

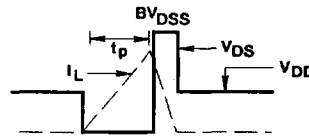


Fig. 15b - Unclamped Energy Waveforms

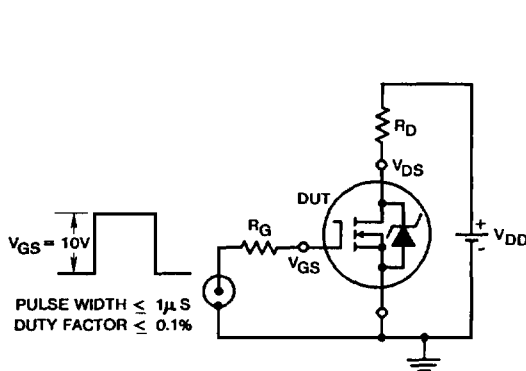


Fig. 16 - Switching Time Test Circuit

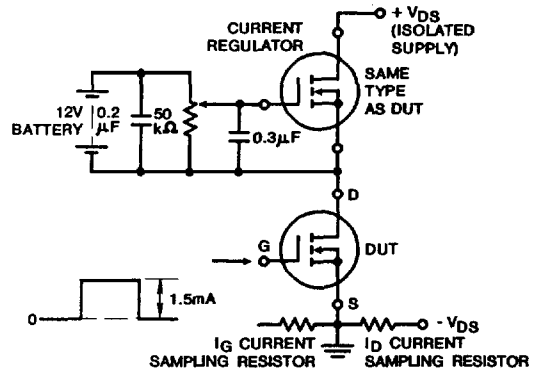


Fig. 17 - Gate Charge Test Circuit