Freescale Semiconductor
Technical Data

Document Number: MW7IC2750N
Rev. 4, 10/2011

RF LDMOS Wideband Integrated Power Amplifiers

MW7IC2750NR1
MW7IC2750GNR1
MW7IC2750NBR1

2500-2700 MHz, 8 W AVG., 28 V
WiMAX
RF LDMOS WIDEBAND
INTEGRATED POWER AMPLIFIERS

The MW7IC2750N wideband integrated circuit is designed with on-chip matching that makes it usable from 2300-2700 MHz. This multi-stage structure is rated for 26 to 32 Volt operation and covers all typical cellular base station modulation formats.

- Typical WiMAX Performance: V_{DD} = 28 Volts, I_{DQ1} = 160 mA, I_{DQ2} = 550 mA, P_{out} = 8 Watts Avg., f = 2700 MHz, OFDM 802.16d, 64 QAM $^3/_4$, 4 Bursts, 10 MHz Channel Bandwidth, Input Signal PAR = 9.5 dB @ 0.01% Probability on CCDF.
  Power Gain — 26 dB
  Power Added Efficiency — 17%
  Device Output Signal PAR — 8.6 dB @ 0.01% Probability on CCDF
  ACPR @ 8.5 MHz Offset — -49 dBc in 1 MHz Channel Bandwidth
- Capable of Handling 10:1 VSWR, @ 32 Vdc, 2600 MHz, 80 Watts CW Output Power (3 dB Input Overdrive from Rated P_{out})
- Stable into a 3:1 VSWR. All Spurs Below -60 dBc @ 1 mW to 80 W CW P_{out}
- Typical P_{out} @ 1 dB Compression Point $\simeq$ 50 Watts CW

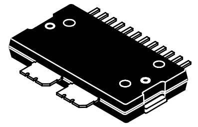
Driver Applications

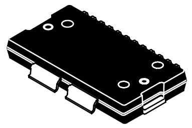
- Typical WiMAX Performance: V_{DD} = 28 Volts, I_{DQ1} = 160 mA, I_{DQ2} = 550 mA, P_{out} = 4 Watts Avg., f = 2700 MHz, OFDM 802.16d, 64 QAM $^3/_4$, 4 Bursts, 10 MHz Channel Bandwidth, Input Signal PAR = 9.5 dB @ 0.01% Probability on CCDF.
  Power Gain — 26 dB
  Power Added Efficiency — 11%
  Device Output Signal PAR — 9.2 dB @ 0.01% Probability on CCDF
  ACPR @ 8.5 MHz Offset — -57 dBc in 1 MHz Channel Bandwidth

Features

- 100% PAR Tested for Guaranteed Output Power Capability
- Characterized with Series Equivalent Large-Signal Impedance Parameters and Common Source S-Parameters
- On-Chip Matching (50 Ohm Input, DC Blocked)
- Integrated Quiescent Current Temperature Compensation with Enable/Disable Function (1)
- Integrated ESD Protection
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- 225°C Capable Plastic Package
- In Tape and Reel. R1 Suffix = 500 Units, 44 mm Tape Width, 13 inch Reel.

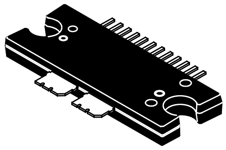
CASE 1618-02
TO-270 WB-14
PLASTIC
MW7IC2750NR1





CASE 1621-02
TO-270 WB-14 GULL
PLASTIC
MW7IC2750GNR1

CASE 1617-02
TO-272 WB-14
PLASTIC
MW7IC2750NBR1



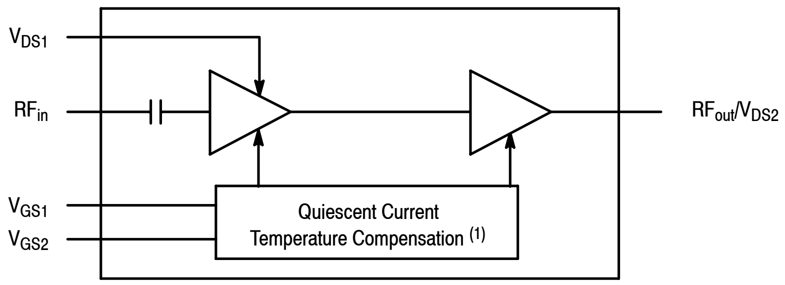
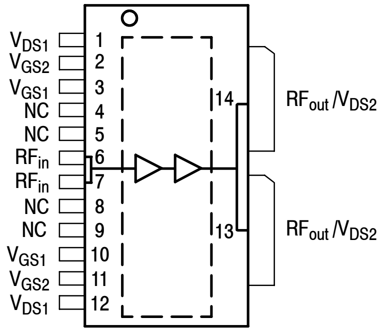


Figure 1. Functional Block Diagram



(Top View)

Note: Exposed backside of the package is the source terminal for the transistors.

Figure 2. Pin Connections

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1. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family* and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1977 or AN1987.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	- 65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature (1,2)	T_J	225	°C
Input Power	P_{in}	30	dBm

Table 2. Thermal Characteristics

Characteristic		Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case		$R_{\theta JC}$		°C/W
CW Application (Case Temperature 80°C, P_{out} = 50 W CW)	Stage 1, 28 Vdc, I_{DQ1} = 160 mA Stage 2, 28 Vdc, I_{DQ2} = 550 mA		3.0 0.7	
Final Application (Case Temperature 70°C, P_{out} = 8 W CW)	Stage 1, 28 Vdc, I_{DQ1} = 160 mA Stage 2, 28 Vdc, I_{DQ2} = 550 mA		2.9 0.7	
Driver Application (Case Temperature 65°C, P_{out} = 4 W CW)	Stage 1, 28 Vdc, I_{DQ1} = 160 mA Stage 2, 28 Vdc, I_{DQ2} = 550 mA		2.8 0.7	

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1C
Machine Model (per EIA/JESD22-A115)	A
Charge Device Model (per JESD22-C101)	III

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics (T$_A$ = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Stage 1 — Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Stage 1 — On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 46 μAdc)	$V_{GS(th)}$	1	2	3	Vdc
Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_{DQ1} = 160 mA, Measured in Functional Test)	$V_{GS(Q)}$	3	3.8	4.5	Vdc
Stage 1 — Dynamic Characteristics (4)					
Input Capacitance (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc ± 30 mV(rms)ac @ 1 MHz)	C_{iss}	—	550	—	pF

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.
4. Part internally matched both on input and output.

(continued)

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Stage 2 — Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Stage 2 — On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 185 μAdc)	$V_{GS(th)}$	1	2	3	Vdc
Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_{DQ2} = 550 mA, Measured in Functional Test)	$V_{GS(Q)}$	2.8	3.6	4.3	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 1 Adc)	$V_{DS(on)}$	0.1	0.12	0.8	Vdc
Stage 2 — Dynamic Characteristics [1]					
Reverse Transfer Capacitance (V_{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	0.68	—	pF
Output Capacitance (V_{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	220	—	pF

Functional Tests (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ1} = 160 mA, I_{DQ2} = 550 mA, P_{out} = 8 W Avg., f = 2700 MHz, WiMAX, OFDM 802.16d, 64 QAM $^3/_4$, 4 Bursts, 10 MHz Channel Bandwidth, Input Signal PAR = 9.5 dB @ 0.01% Probability on CCDF. ACPR measured in 1 MHz Channel Bandwidth @ ±8.5 MHz Offset.

Characteristic	Symbol	Min	Typ	Max	Unit
Power Gain	G_{ps}	24	26	31	dB
Power Added Efficiency	PAE	15	17	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	7.8	8.6	—	dB
Adjacent Channel Power Ratio	ACPR	—	-49	-45	dBc
Input Return Loss	IRL	—	-12	-10	dB

Typical Performances OFDM Signal — 10 MHz Channel Bandwidth (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ1} = 160 mA, I_{DQ2} = 550 mA, P_{out} = 8 W Avg., f = 2700 MHz, WiMAX, OFDM 802.16d, 64 QAM $^3/_4$, 4 Bursts, 10 MHz Channel Bandwidth, Input Signal PAR = 9.5 dB @ 0.01% Probability on CCDF.

Characteristic	Symbol	Min	Typ	Max	Unit
Relative Constellation Error [2]	RCE	—	-33	—	dB
Error Vector Magnitude [2]	EVM	—	2.3	—	% rms

Typical Performances OFDM Signal — 7 MHz Channel Bandwidth (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ1} = 160 mA, I_{DQ2} = 550 mA, P_{out} = 8 W Avg., f = 2700 MHz, WiMAX, OFDM 802.16d, 64 QAM $^3/_4$, 4 Bursts, 7 MHz Channel Bandwidth, Input Signal PAR = 9.5 dB @ 0.01% Probability on CCDF.

Characteristic	Symbol	Min	Typ	Max	Unit
Mask System Type G	Mask				dBc
Point B at 3.5 MHz Offset		—	-27	—	
Point C at 5 MHz Offset		—	-40	—	
Point D at 7.4 MHz Offset		—	-43	—	
Point E at 14 MHz Offset		—	-58	—	
Point F at 17.5 MHz Offset		—	-63	—	
Relative Constellation Error [2]	RCE	—	-33	—	dB
Error Vector Magnitude [2]	EVM	—	2.3	—	% rms

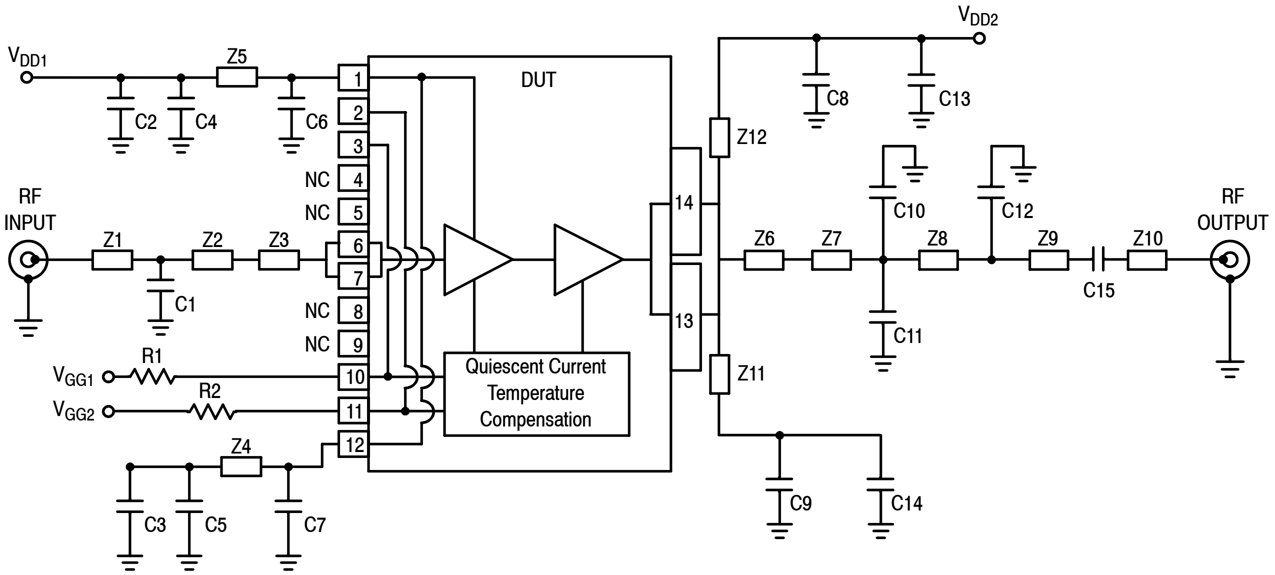
1. Part internally matched both on input and output.
2. RCE = 20Log(EVM/100)

(continued)

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Typical Performances (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ1} = 160 mA, I_{DQ2} = 550 mA, 2700 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	55	—	W
IMD Symmetry @ 50 W PEP, P_{out} where IMD Third Order Intermodulation $\cong$ 30 dBc (Delta IMD Third Order Intermodulation between Upper and Lower Sidebands > 2 dB)	IMD_{sym}	—	60	—	MHz
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	50	—	MHz
Gain Flatness in 200 MHz Bandwidth @ P_{out} = 8 W Avg.	G_F	—	0.5	—	dB
Average Deviation from Linear Phase in 200 MHz Bandwidth @ P_{out} = 50 W CW	Φ	—	1.1	—	°
Average Group Delay @ P_{out} = 50 W CW, f = 2600 MHz	Delay	—	2.3	—	ns
Part-to-Part Insertion Phase Variation @ P_{out} = 50 W CW, f = 2600 MHz, Six Sigma Window	$\Delta\Phi$	—	38.7	—	°
Gain Variation over Temperature (-30°C to +85°C)	ΔG	—	0.037	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C)	ΔP1dB	—	0.005	—	dB/°C
Typical Driver Performances (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ1} = 160 mA, I_{DQ2} = 550 mA, P_{out} = 4 W Avg., f = 2700 MHz, WiMAX, OFDM 802.16d, 64 QAM $^3/_4$, 4 Bursts, 10 MHz Channel Bandwidth, Input Signal PAR = 9.5 dB @ 0.01% Probability on CCDF. ACPR measured in 1 MHz Channel Bandwidth @ ±8.5 MHz Offset.					
Power Gain	G_{ps}	—	26	—	dB
Power Added Efficiency	PAE	—	11	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	—	9.2	—	dB
Adjacent Channel Power Ratio	ACPR	—	-57	—	dBc
Input Return Loss	IRL	—	-13	—	dB
Relative Constellation Error @ P_{out} = 2.5 W Avg. (1)	RCE	—	-39	—	dB

1. RCE = 20Log(EVM/100)



Z1	0.662″ x 0.064″ Microstrip	Z8	0.417″ x 0.064″ Microstrip
Z2	1.530″ x 0.064″ Microstrip	Z9	1.137″ x 0.064″ Microstrip
Z3	0.126″ x 0.060″ Microstrip	Z10	0.293″ x 0.064″ Microstrip
Z4, Z5	0.771″ x 0.046″ Microstrip	Z11, Z12	0.615″ x 0.095″ Microstrip
Z6	0.192″ x 0.860″ Microstrip	PCB	Rogers RO4350B, 0.030″, ε_r = 3.5
Z7	0.280″ x 0.719″ Microstrip		

Figure 3. MW7IC2750NR1(GNR1)(NBR1) Test Circuit Schematic

Table 6. MW7IC2750NR1(GNR1)(NBR1) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1	0.8 pF Chip Capacitor	ATC100B0R8BT500XT	ATC
C2, C3, C13, C14	10 μF, 50 V Chip Capacitors	GRM55DR61H106KA88B	Murata
C4, C5, C8, C9, C15	5.1 pF Chip Capacitors	ATC100B5R1CT500XT	ATC
C6, C7	1 μF, 100 V Chip Capacitors	GRM32ER72A105KA01L	Murata
C10, C11	0.2 pF Chip Capacitors	ATC100B0R2BT500XT	ATC
C12	0.5 pF Chip Capacitor	ATC100B0R5BT500XT	ATC
R1, R2	1 kΩ, 1/4 W Chip Resistors	CRCW12061001FKEA	Vishay

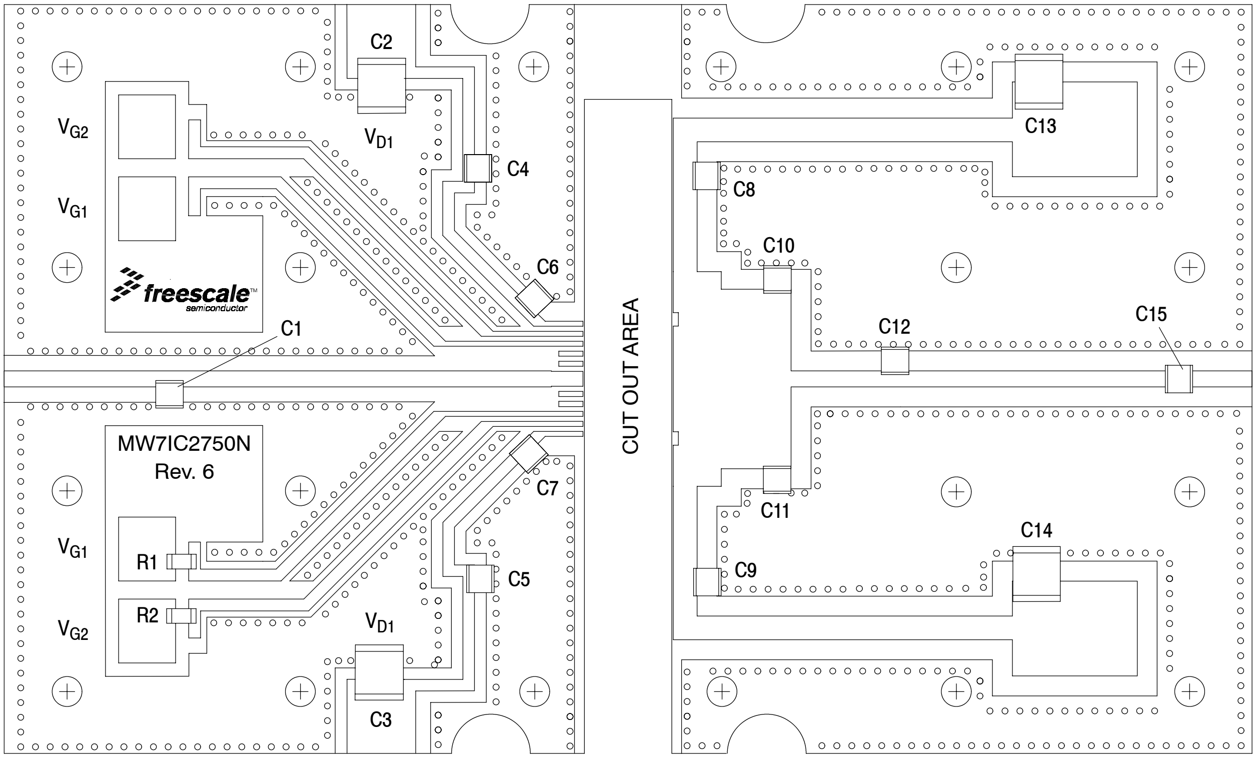


Figure 4. MW7IC2750NR1(GNR1)(NBR1) Test Circuit Component Layout

TYPICAL CHARACTERISTICS

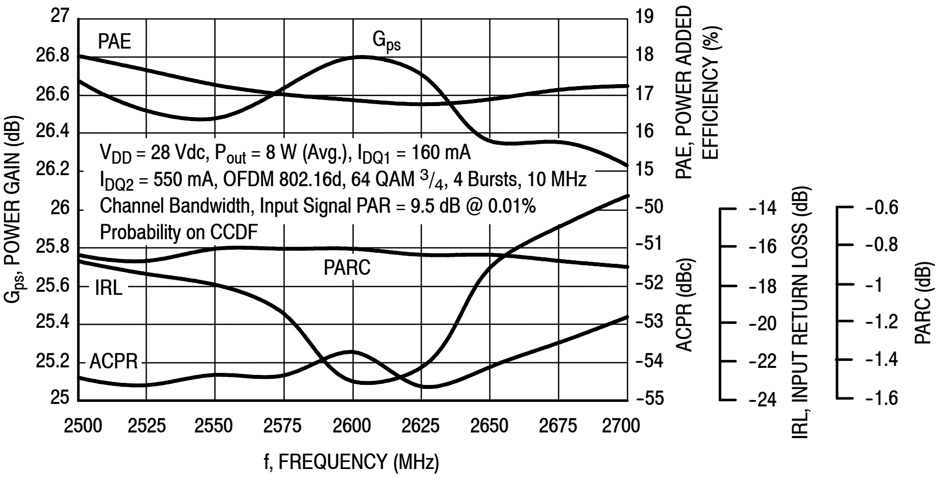


Figure 5. WiMAX Broadband Performance @ P_{out} = 8 Watts Avg.

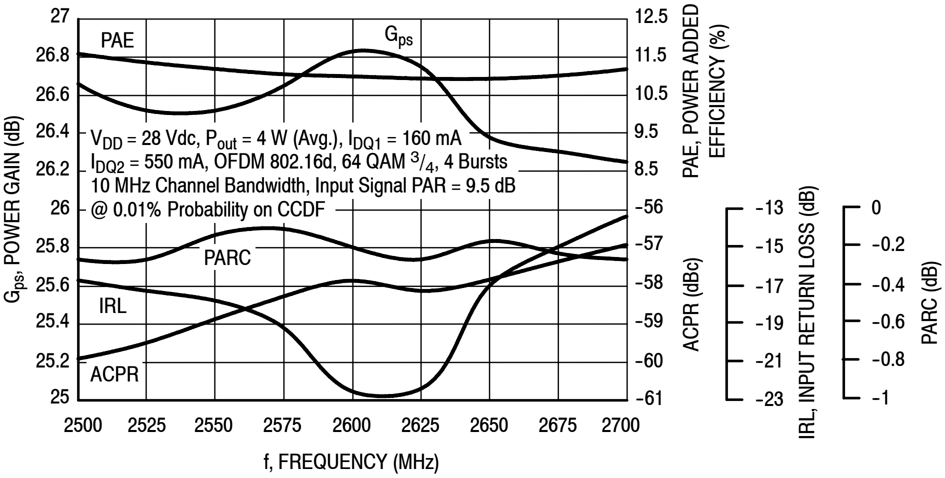


Figure 6. WiMAX Broadband Performance @ P_{out} = 4 Watts Avg.

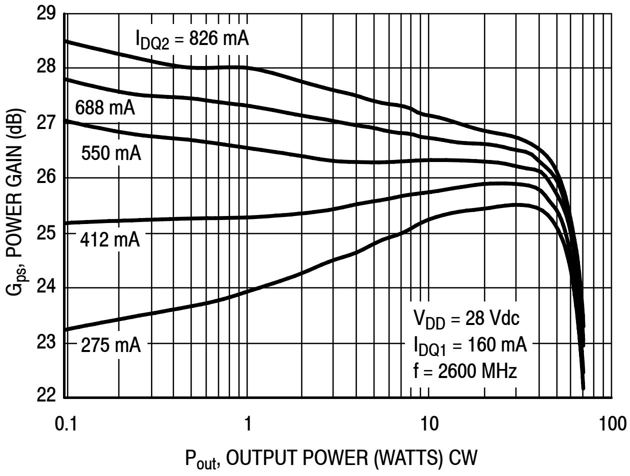


Figure 7. Power Gain versus Output Power @ I_{DQ1} = 160 mA

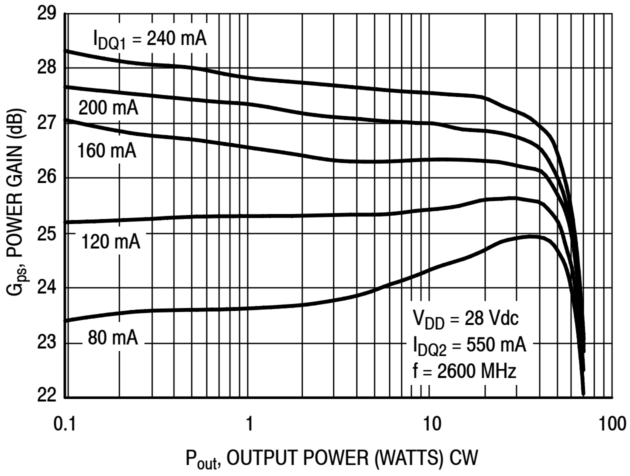


Figure 8. Power Gain versus Output Power @ I_{DQ2} = 550 mA

TYPICAL CHARACTERISTICS

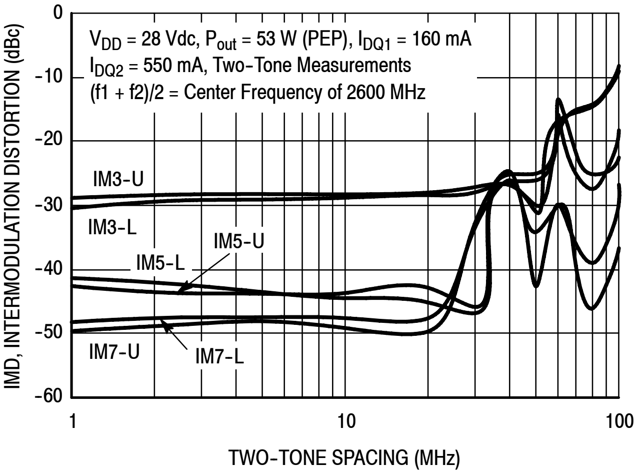


Figure 9. Intermodulation Distortion Products versus Tone Spacing

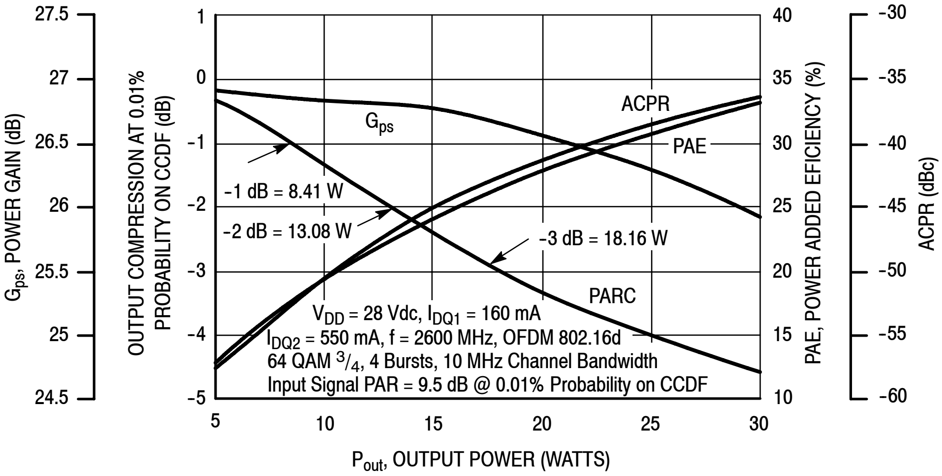


Figure 10. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

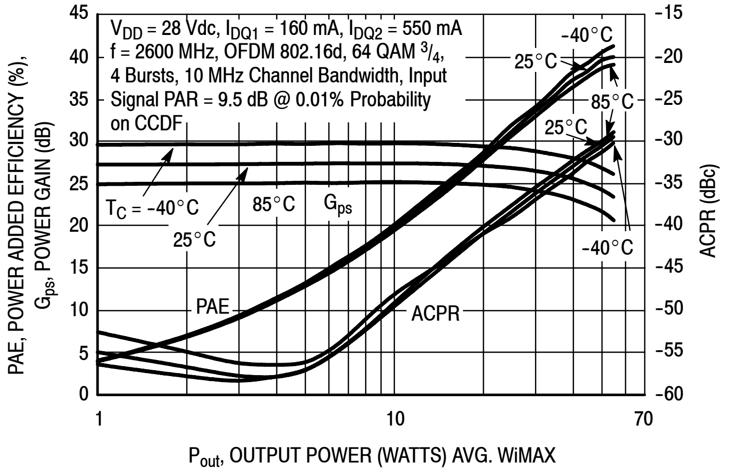


Figure 11. WiMAX, ACPR, Power Gain and Power Added Efficiency versus Output Power

TYPICAL CHARACTERISTICS

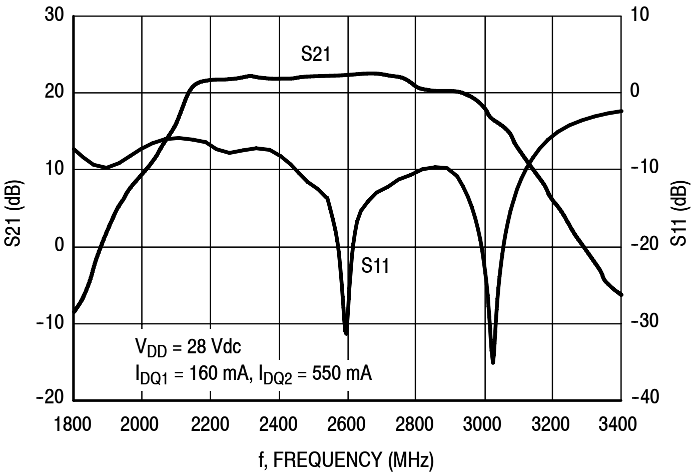


Figure 12. Broadband Frequency Response

WIMAX TEST SIGNAL

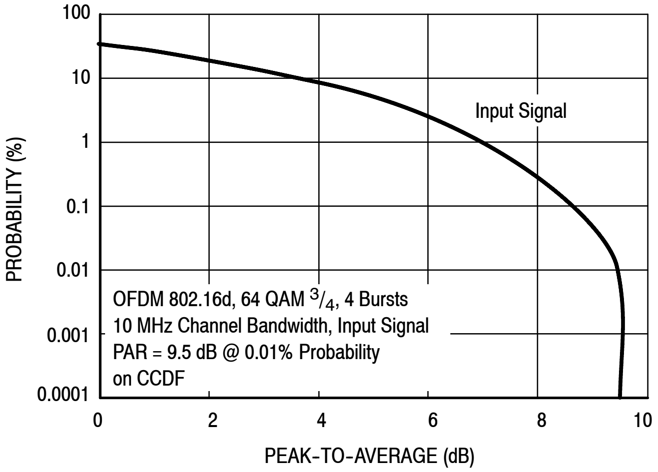


Figure 13. OFDM 802.16d Test Signal

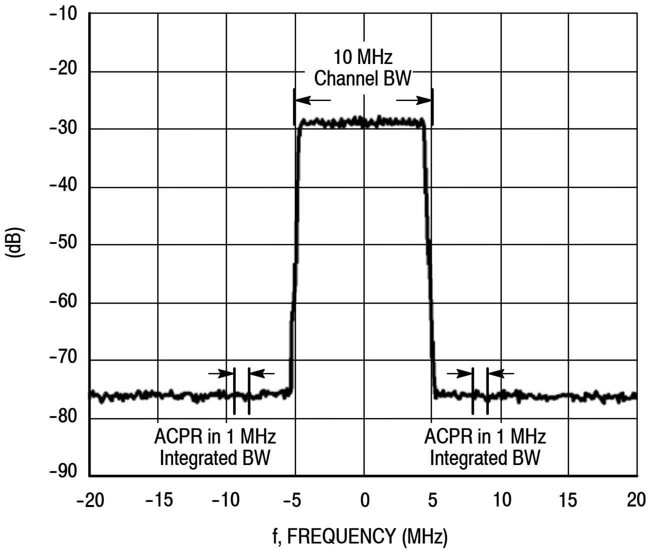
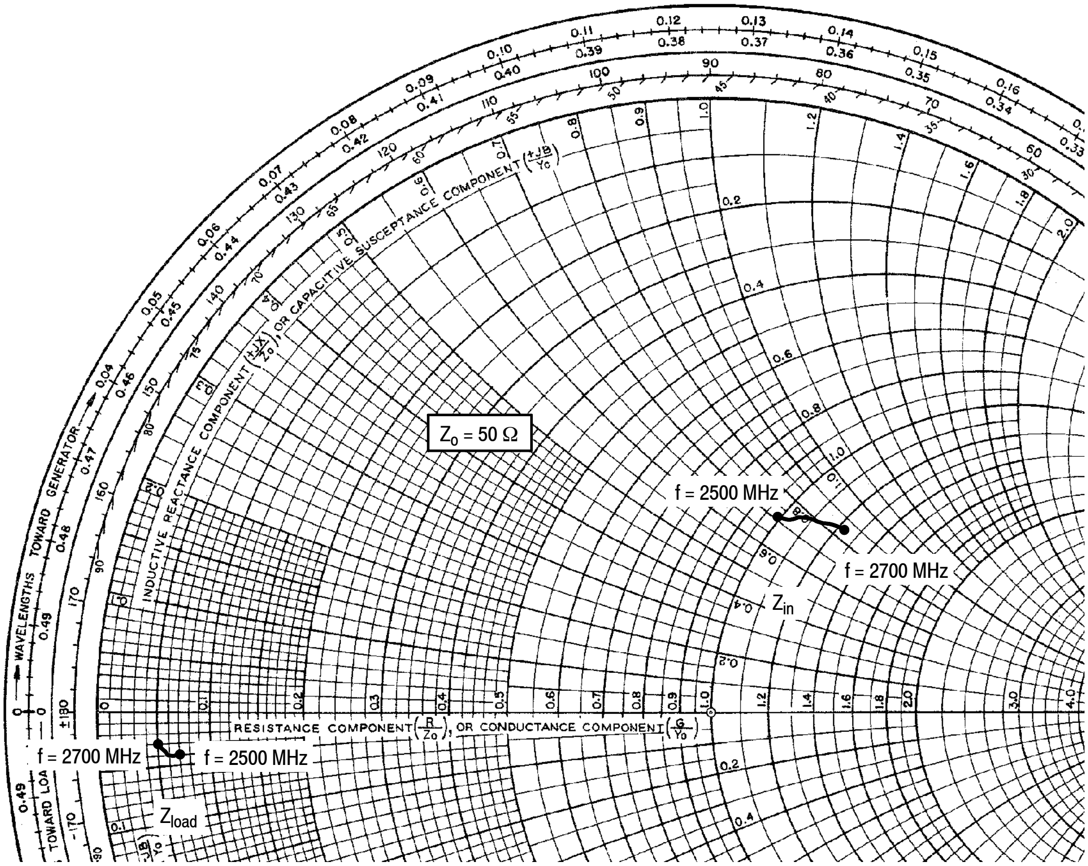


Figure 14. WiMAX Spectrum Mask Specifications



V_{DD} = 28 Vdc, I_{DQ1} = 160 mA, I_{DQ2} = 550 mA, P_{out} = 8 W Avg.

f MHz	Z_{in} Ω	Z_{load} Ω
2500	49.58 + j35.82	3.52 - j1.79
2525	50.78 + j36.71	3.46 - j1.82
2550	52.04 + j37.58	3.37 - j1.86
2575	53.39 + j38.45	3.24 - j1.88
2600	54.82 + j39.30	3.09 - j1.87
2625	56.35 + j40.14	2.94 - j1.84
2650	57.96 + j40.95	2.77 - j1.77
2675	59.68 + j41.74	2.60 - j1.66
2700	61.50 + j42.49	2.44 - j1.56

Z_{in} = Device input impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

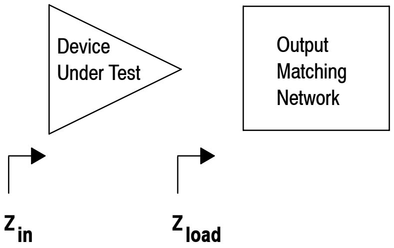


Figure 15. Series Equivalent Source and Load Impedance

Table 7. Common Source S-Parameters (V_{DD} = 28 V, I_{DQ1} = 160 mA, I_{DQ2} = 550 mA, T_A = 25°C, 50 Ohm System)

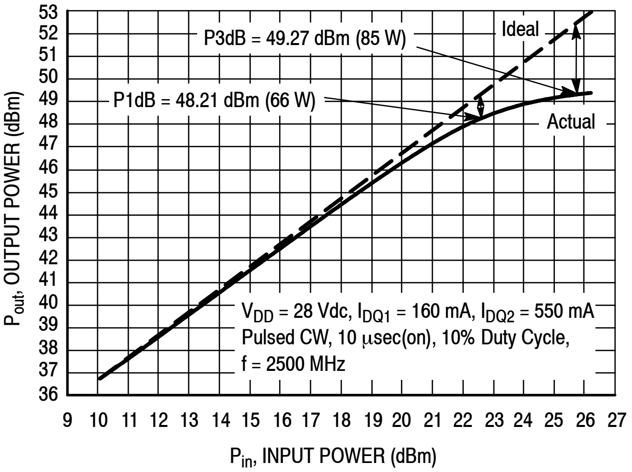
f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
1500	0.754	78.5	0.001	−17.9	0.000774	17.4	0.994	174.5
1550	0.734	70.1	0.001	−118.8	0.000326	85.4	0.993	175.3
1600	0.716	61.7	0.003	−116.5	0.000392	58.7	0.998	174.6
1650	0.697	53.4	0.009	−135.3	0.000268	27.8	0.997	173.9
1700	0.677	45.1	0.024	−152.3	0.000211	−33.8	0.996	172.9
1750	0.651	36.6	0.064	−179.9	0.000309	148.0	0.991	171.7
1800	0.619	27.6	0.141	146.0	0.000599	148.7	0.981	170.3
1850	0.578	17.7	0.255	113.0	0.000732	142.6	0.970	169.0
1900	0.527	5.6	0.425	84.8	0.000734	149.1	0.957	167.3
1950	0.462	−9.3	0.701	61.4	0.000911	144.7	0.941	165.6
2000	0.392	−27.8	1.237	39.8	0.00154	174.4	0.924	163.6
2050	0.312	−51.0	2.342	15.9	0.00286	159.0	0.895	160.9
2100	0.218	−74.1	4.772	−11.8	0.00377	142.2	0.843	156.6
2150	0.139	−77.4	11.680	−51.5	0.00588	128.7	0.691	149.4
2200	0.426	−69.8	27.658	−129.7	0.00919	73.9	0.342	−169.4
2250	0.490	−123.5	21.740	150.4	0.00545	38.1	0.800	−166.9
2300	0.416	−146.4	16.087	106.5	0.00314	33.9	0.864	−174.9
2350	0.352	−160.1	13.279	71.6	0.00239	24.9	0.879	−177.0
2400	0.321	−166.6	11.654	41.9	0.00175	33.1	0.891	−177.5
2450	0.274	−173.2	10.543	13.4	0.00197	27.7	0.908	−177.4
2500	0.233	−177.6	9.748	−13.4	0.00181	34.5	0.924	−177.5
2550	0.178	179.0	8.983	−40.5	0.00204	31.5	0.943	−177.7
2600	0.123	−167.7	8.199	−65.8	0.00218	35.6	0.957	−178.0
2650	0.108	−148.8	7.452	−89.9	0.00208	33.2	0.970	−178.7
2700	0.121	−132.6	6.730	−113.1	0.00198	23.8	0.978	−179.6
2750	0.146	−119.9	6.008	−135.3	0.00191	31.0	0.985	179.4
2800	0.184	−119.9	5.323	−156.1	0.00211	23.7	0.987	178.3
2850	0.214	−121.0	4.700	−175.6	0.00159	15.5	0.987	177.3
2900	0.261	−127.6	4.109	166.0	0.00205	14.6	0.985	176.3
2950	0.316	−134.0	3.591	149.0	0.00171	19.2	0.984	175.4
3000	0.372	−141.4	3.130	133.3	0.00103	16.7	0.984	174.5
3050	0.430	−150.2	2.733	118.1	0.00095	26.4	0.984	173.8
3100	0.485	−158.9	2.388	103.6	0.00103	36.9	0.984	173.2
3150	0.534	−166.3	2.091	90.1	0.00108	24.1	0.985	172.7
3200	0.585	−172.7	1.846	77.3	0.00127	47.6	0.984	172.4
3250	0.625	−178.0	1.635	65.2	0.00119	57.1	0.986	172.1
3300	0.657	177.3	1.472	52.9	0.00132	53.2	0.985	171.9
3350	0.686	173.2	1.342	40.8	0.00200	53.8	0.985	171.7

(continued)

Table 7. Common Source S-Parameters (V_{DD} = 28 V, I_{DQ1} = 160 mA, I_{DQ2} = 550 mA, T_A = 25°C, 50 Ohm System) **(continued)**

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	$\angle \phi$	$\|S_{21}\|$	$\angle \phi$	$\|S_{12}\|$	$\angle \phi$	$\|S_{22}\|$	$\angle \phi$
3400	0.702	169.7	1.243	28.4	0.00230	54.4	0.982	171.3
3450	0.718	166.7	1.193	10.8	0.00211	62.5	0.947	170.1
3500	0.721	164.7	0.937	3.1	0.00233	24.3	0.976	173.0
3550	0.746	162.0	0.914	-7.9	0.00213	51.7	0.981	171.9
3600	0.758	158.9	0.857	-21.4	0.00236	55.6	0.978	171.1

ALTERNATIVE PEAK TUNE LOAD PULL CHARACTERISTICS

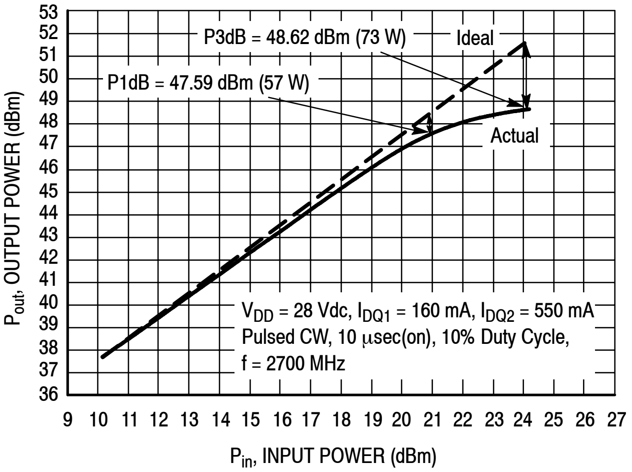


NOTE: Load Pull Test Fixture Tuned for Peak P1dB Output Power @ 28 V

Test Impedances per Compression Level

	Z_{source} Ω	Z_{load} Ω
P1dB	28.46 + j5.15	1.67 - j1.53

Figure 16. Pulsed CW Output Power versus Input Power @ 28 V @ 2500 MHz



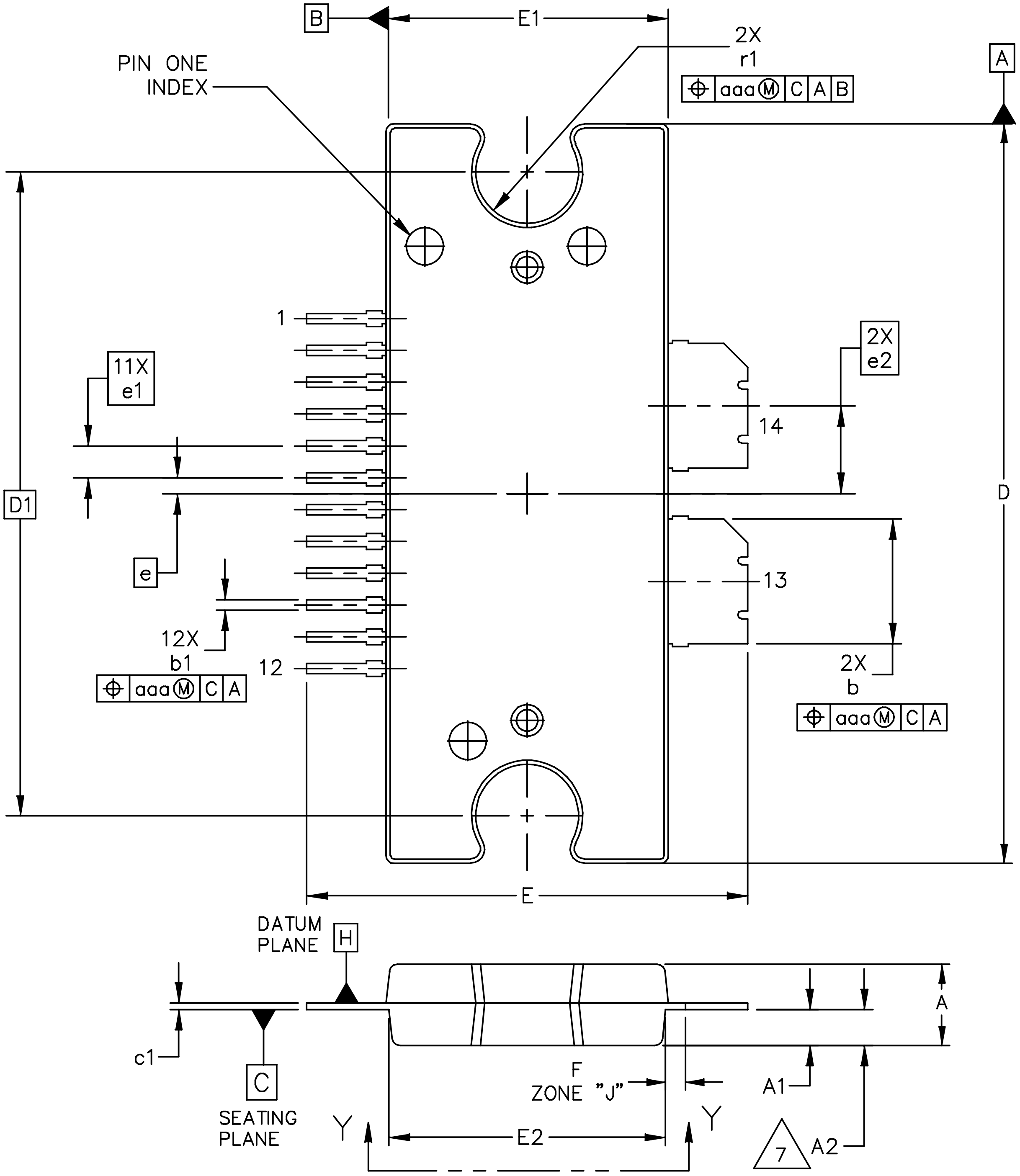
NOTE: Load Pull Test Fixture Tuned for Peak P1dB Output Power @ 28 V

Test Impedances per Compression Level

	Z_{source} Ω	Z_{load} Ω
P1dB	36.24 + j1.75	1.19 - j1.29

Figure 17. Pulsed CW Output Power versus Input Power @ 28 V @ 2700 MHz

PACKAGE DIMENSIONS



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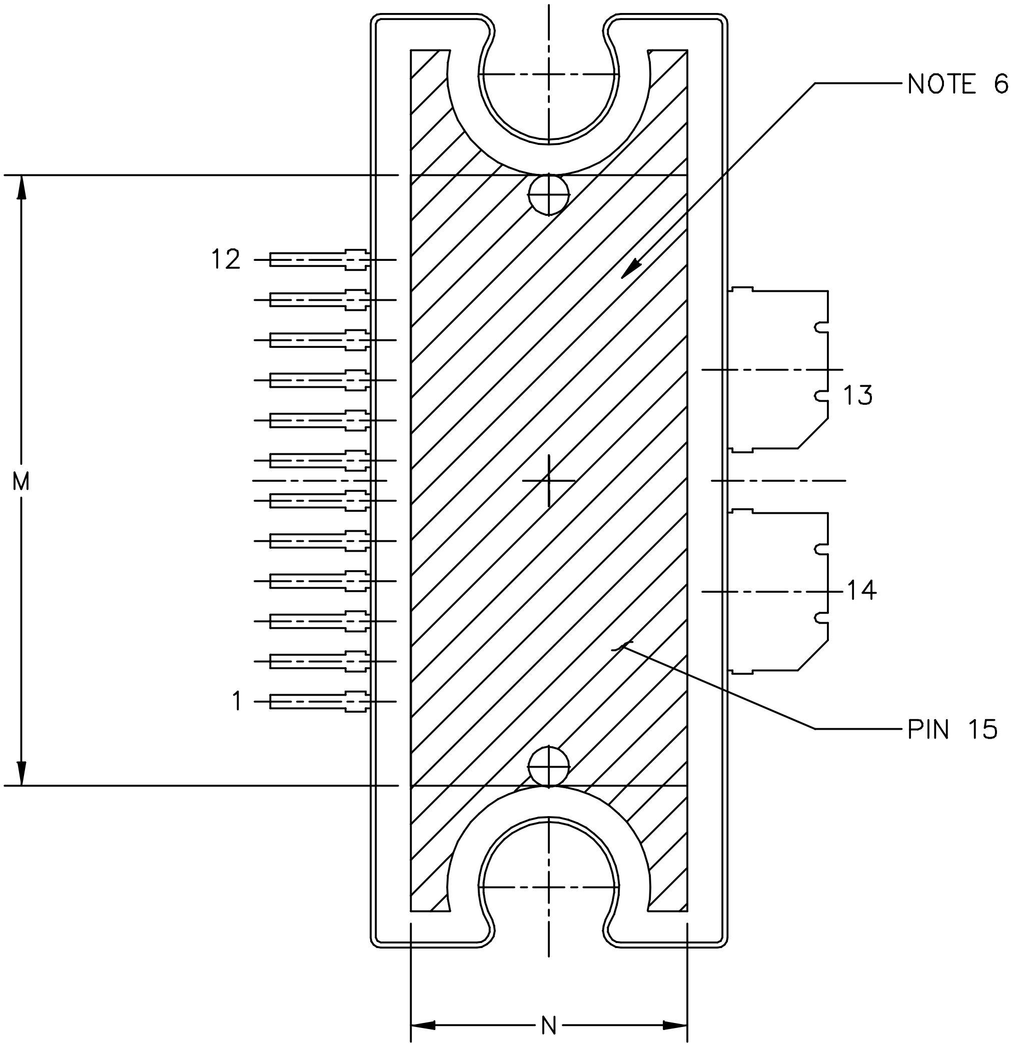

VIEW Y–Y

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	CASE NUMBER: 1617–02		27 JUN 2007
	STANDARD: NON–JEDEC		

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 (0.15) PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.

5. DIMENSIONS "b" AND "b1" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b" AND "b1" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.

6. HATCHING REPRESENTS THE EXPOSED AREA OFTHE HEAT SLUG.

7. DIM A2 APPLIES WITHIN ZONE "J" ONLY.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	b	.154	.160	3.91	4.06
A1	.039	.043	0.99	1.09	b1	.010	.016	0.25	0.41
A2	.040	.042	1.02	1.07	c1	.007	.011	0.18	0.28
D	.928	.932	23.57	23.67	e	.020 BSC		0.51 BSC	
D1	.810 BSC		20.57 BSC		e1	.040 BSC		1.02 BSC	
E	.551	.559	14.00	14.20	e2	.1105 BSC		2.807 BSC	
E1	.353	.357	8.97	9.07	r1	.063	.068	1.6	1.73
E2	.346	.350	8.79	8.89					
F	.025 BSC		0.64 BSC		aaa	.004		0.10	
M	.600	----	15.24	----					
N	.270	----	6.86	----					

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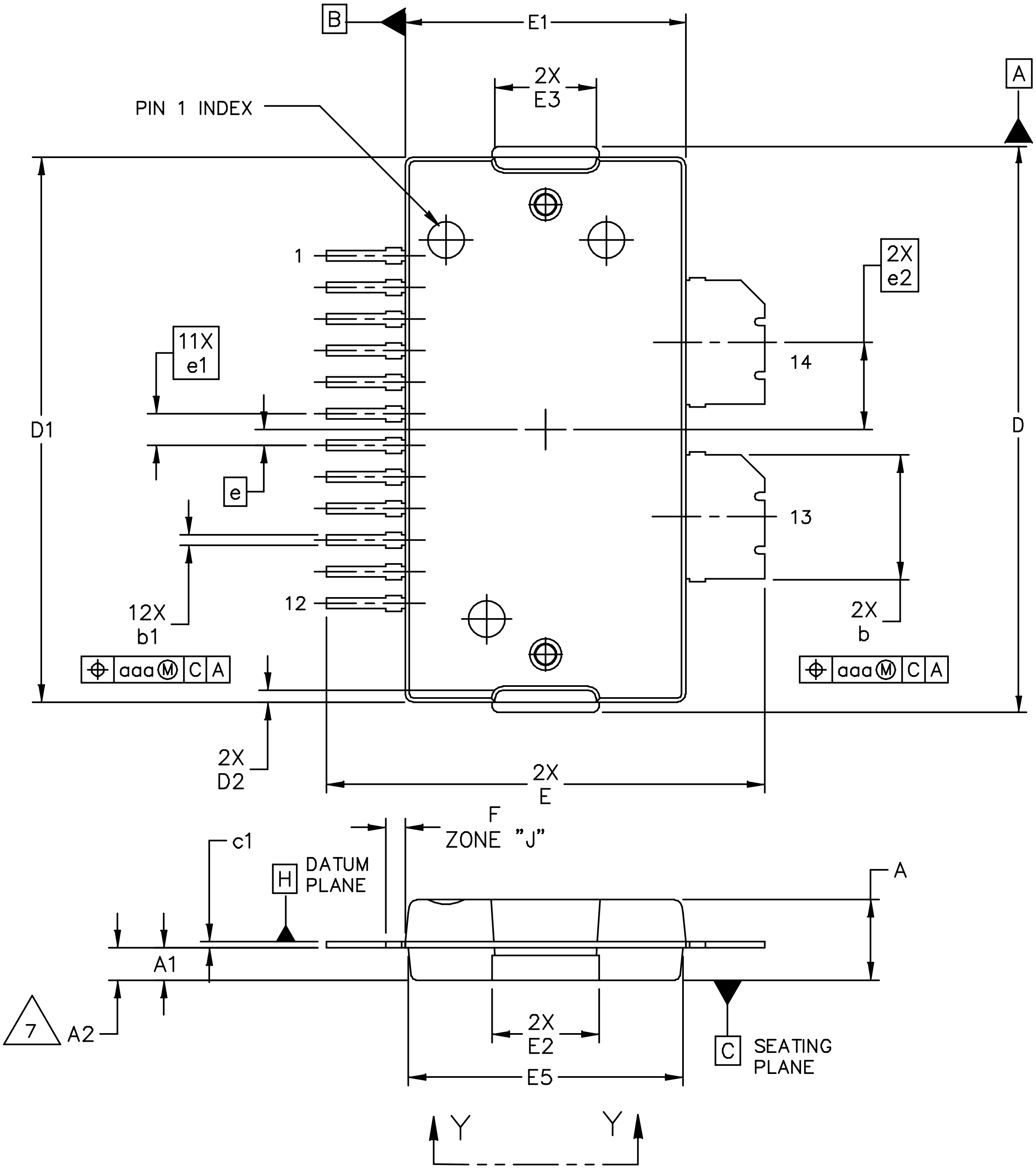

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	CASE NUMBER: 1618–02	19 JUN 2007
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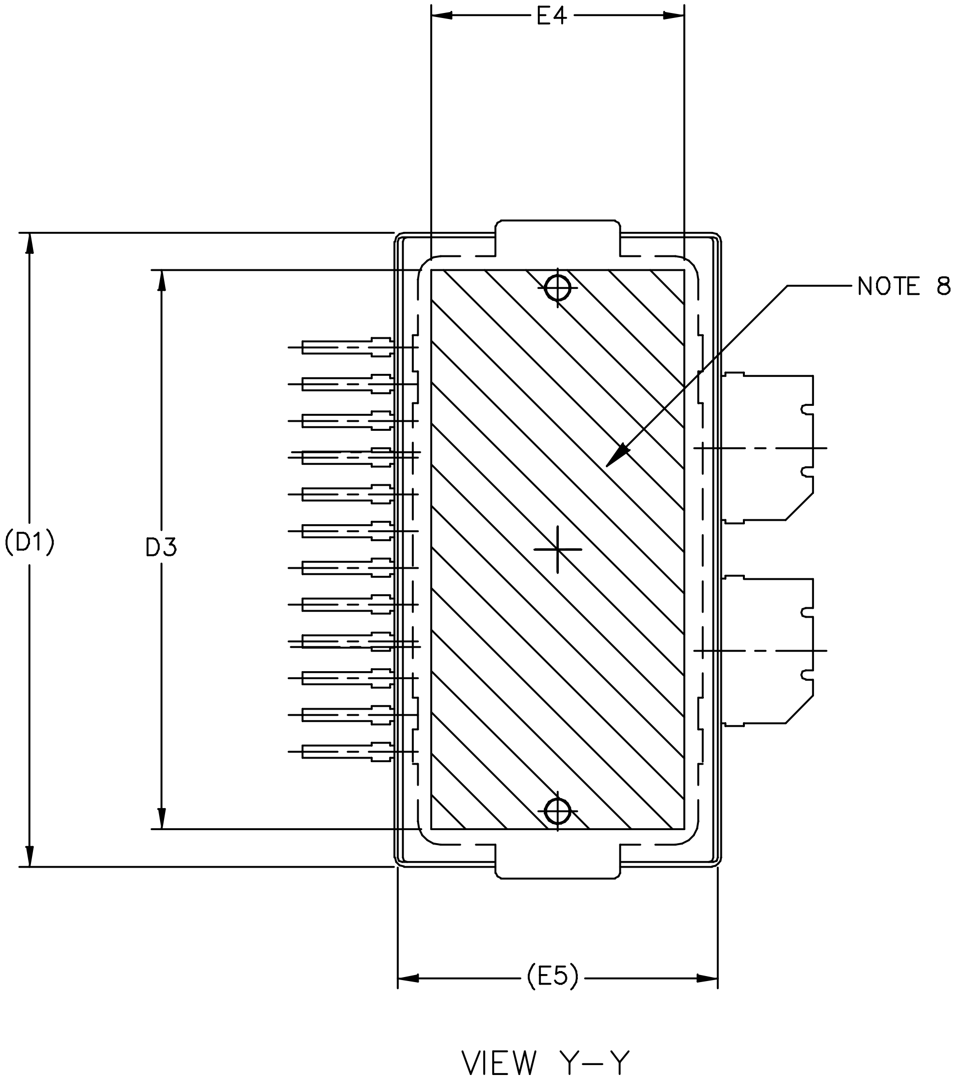

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	CASE NUMBER: 1618–02		19 JUN 2007
	STANDARD: NON–JEDEC		

NOTES:

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2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M−1994.
3. DATUM PLANE −H− IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE −H−.
5. DIMENSIONS "b" AND "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b" AND "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS −A− AND −B− TO BE DETERMINED AT DATUM PLANE −H−.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	F	.025 BSC		0.64 BSC	
A1	.039	.043	0.99	1.09	b	.154	.160	3.91	4.06
A2	.040	.042	1.02	1.07	b1	.010	.016	0.25	0.41
D	.712	.720	18.08	18.29	c1	.007	.011	.18	.28
D1	.688	.692	17.48	17.58	e	.020 BSC		0.51 BSC	
D2	.011	.019	0.28	0.48	e1	.040 BSC		1.02 BSC	
D3	.600	−−−	15.24	−−−	e2	.1105 BSC		2.807 BSC	
E	.551	.559	14	14.2					
E1	.353	.357	8.97	9.07	aaa	.004		.10	
E2	.132	.140	3.35	3.56					
E3	.124	.132	3.15	3.35					
E4	.270	−−−	6.86	−−−					
E5	.346	.350	8.79	8.89					

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
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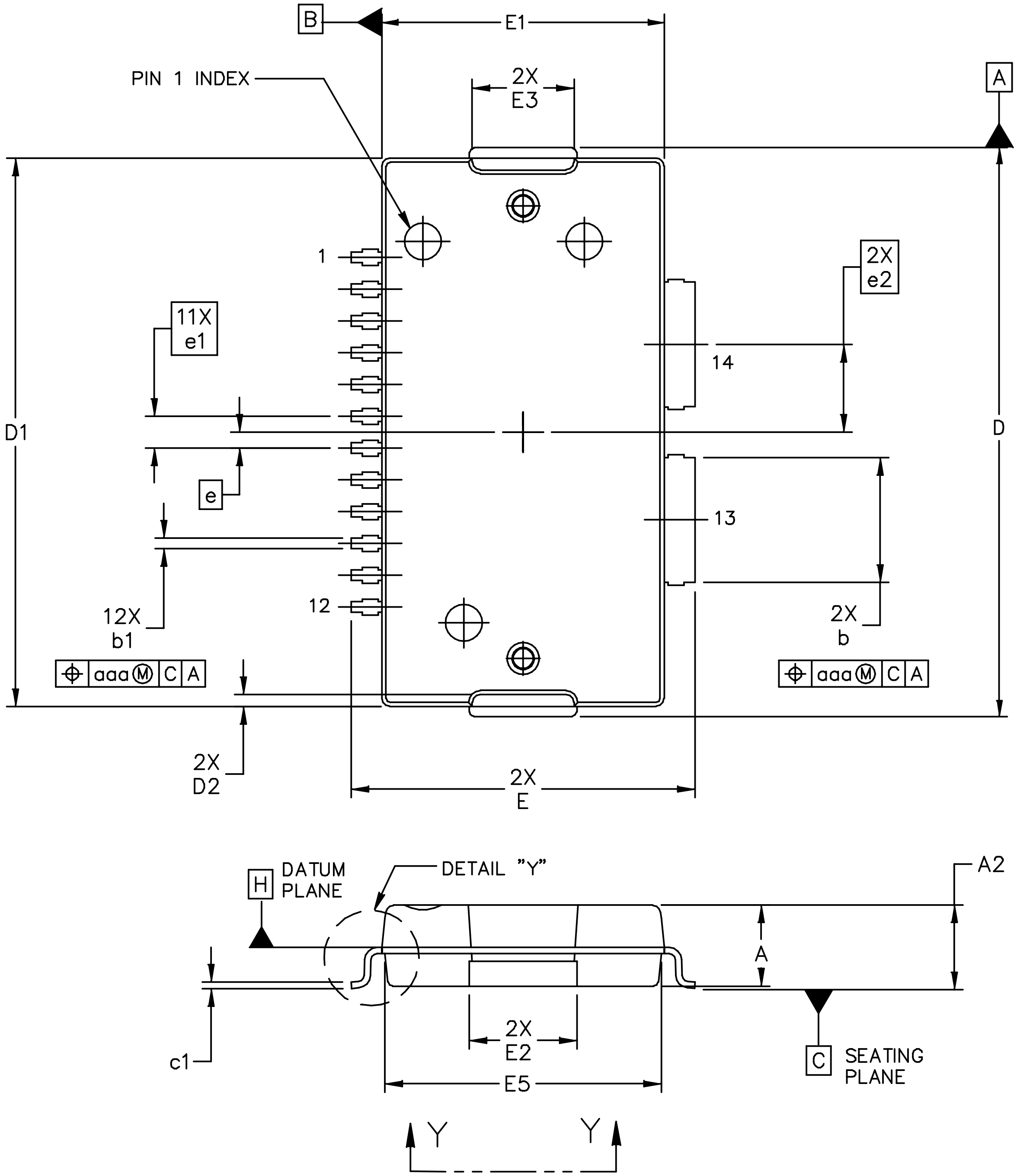

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	CASE NUMBER: 1621–02	19 JUN 2007
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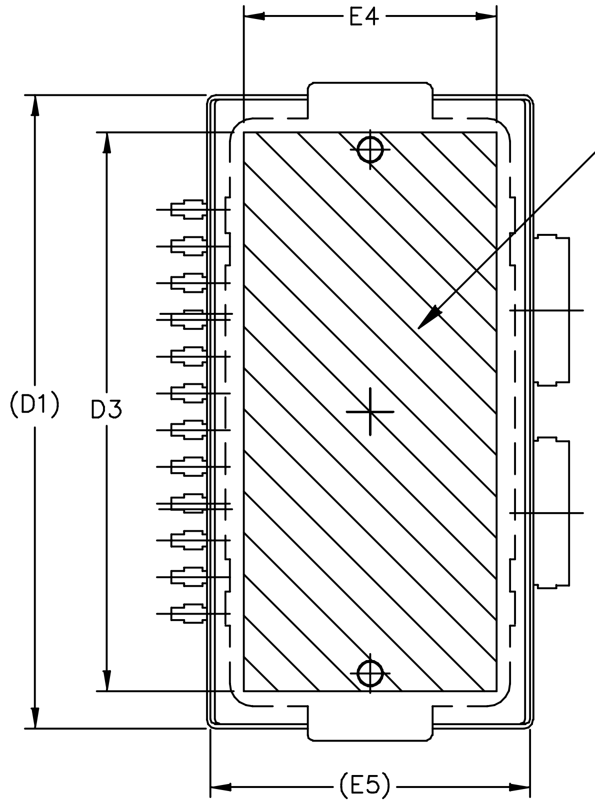
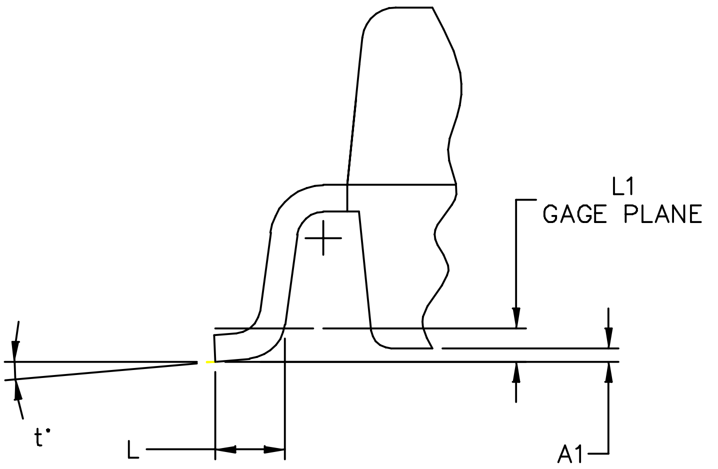


VIEW Y–Y



DETAIL "Y"

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	CASE NUMBER: 1621–02	19 JUN 2007
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NOTES:

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3. DATUM PLANE –H– IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS "b" AND "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b" AND "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS –A– AND –B– TO BE DETERMINED AT DATUM PLANE –H–.
7. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	L	.018	.024	0.46	0.61
A1	.001	.004	0.02	0.10	L1	.010 BSC		0.25 BSC	
A2	.099	.110	2.51	2.79	b	.154	.160	3.91	4.06
D	.712	.720	18.08	18.29	b1	.010	.016	0.25	0.41
D1	.688	.692	17.48	17.58	c1	.007	.011	.18	.28
D2	.011	.019	0.28	0.48	e	.020 BSC		0.51 BSC	
D3	.600	---	15.24	---	e1	.040 BSC		1.02 BSC	
E	.429	.437	10.9	11.1	e2	.1105 BSC		2.807 BSC	
E1	.353	.357	8.97	9.07	t	2°	8°	2°	8°
E2	.132	.140	3.35	3.56					
E3	.124	.132	3.15	3.35	aaa	.004		.10	
E4	.270	---	6.86	---					
E5	.346	.350	8.79	8.89					

MECHANICAL OUTLINE

PRINT VERSION NOT TO SCALE

TITLE:
TO–270 WIDE BODY
14 LEAD
GULL WING

DOCUMENT NO: 98ASA10653D

REV: A

CASE NUMBER: 1621–02

19 JUN 2007

STANDARD: NON–JEDEC

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following documents, software and tools to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Over-Molded Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN1977: Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family
- AN1987: Quiescent Current Control for the RF Integrated Circuit Device Family
- AN3263: Bolt Down Mounting Method for High Power RF Transistors and RFICs in Over-Molded Plastic Packages
- AN3789: Clamping of High Power RF Transistors and RFICs in Over-Molded Plastic Packages

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model

For Software and Tools, do a Part Number search at http://www.freescale.com, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	May 2008	• Initial Release of Data Sheet
1	Oct. 2008	• Corrected footnote reference in Typical Performances OFDM Signal - 10 MHz Bandwidth table, p. 3 • Updated Fig. 13, MTTF versus Junction Temperature, to correct a calculation error, p. 9
2	Feb. 2010	• Modified VSWR rating to show the 3 dB overdrive capability, p. 1 • Corrected maximum input power level to the tested value, from 13 dBm to 25 dBm in Maximum Ratings table, p. 2 • Fig. 3, Test Circuit Schematic, corrected Rogers RO4350B dielectric constant from 3.66 ε_r to 3.5 ε_r, p. 5 • Added AN3789, Clamping of High Power RF Transistors and RFICs in Over-Molded Plastic Packages to Product Documentation, Application Notes, p. 24
3	Mar. 2011	• Table 1, Maximum Ratings, increased Input Power from 25 dBm to 30 dBm to reflect the true capability of the device, p. 2
4	Oct. 2011	• Table 3, ESD Protection Characterization, removed the word “Minimum” after the ESD class rating. ESD ratings are characterized during new product development but are not 100% tested during production. ESD ratings provided in the data sheet are intended to be used as a guideline when handling ESD sensitive devices, p. 2 • Fig. 5, Test Circuit Schematic, corrected pin connections for pin numbers 2, 3, 10 and 11 to reflect actual pin functionality, p. 5 • Fig. 13, MTTF versus Junction Temperature removed, p. 9. Refer to the device’s MTTF Calculator available at freescale.com/RFpower. Go to Design Resources > Software and Tools.

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