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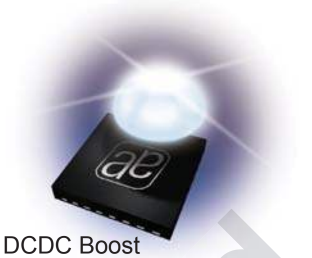
AS3648

2000mA High Current LED Flash Driver



1 General Description

The AS3648 is an inductive high efficient DCDC step up converter with two current sinks. The DCDC step up converter operates at a fixed frequency of 4MHz and includes soft startup to allow easy integration into noise sensitive RF systems. The two current sinks can operate in flash / torch / assist (=video) light modes.

The AS3648 includes flash timeout, overvoltage, overtemperature, undervoltage and LED short circuit protection functions. A TXMASK/TORCH function reduces the flash current in case of parallel operation to the RF power amplifier and avoids a system shutdown. Alternatively this pin can be used to directly operate the torch light directly.

The AS3648 is controlled by an I^2C interface and has a hardware automatic shutdown if SCL=0 for 100ms. Therefore no additional enable input is required for shutting down of the device once the system shuts down.

The AS3648 is available in a space-saving WL-CSP package measuring only 2.25x1.5x0.6mm and operates over the -30ºC to +85ºC temperature range.

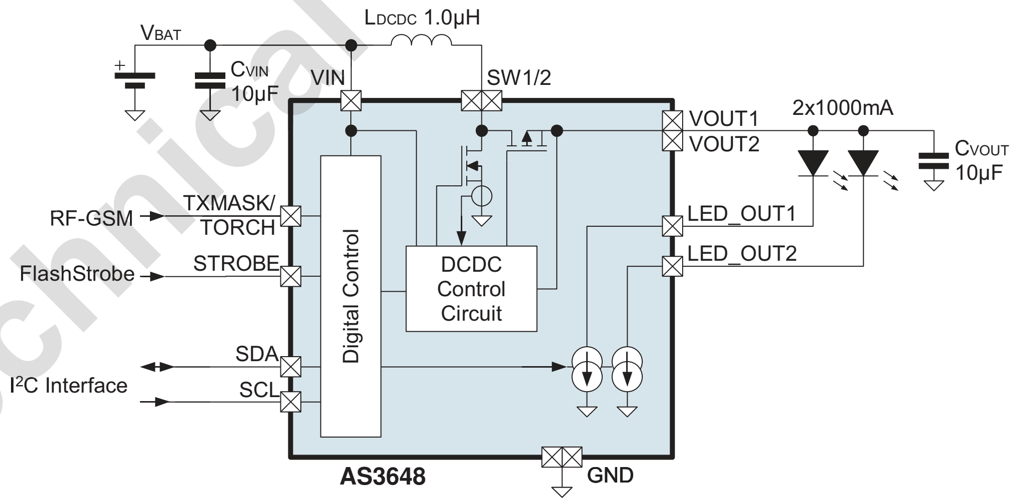
2 Key Features

- High efficiency 4MHz fixed frequency DCDC Boost converter with soft start allows small coils
  - Stable even in coil current limit
- LED current adjustable up to 2000mA
- Two LED operation or single LED operation (combine LED_OUT1 with LED_OUT2)
- Automatic current adjustment for low battery voltage
- PWM operation for lower output current for reliable light output of the LED; running at 31.25kHz to avoid audible noise
- Protection functions:
  Automatic Flash Timeout timer to protect the LED(s)
  Overvoltage and undervoltage Protection
  Overtemperature Protection
  LED short/open circuit protection
- I^2C Interface with automatic shutdown
- 5V constant voltage mode operation
- Available in tiny WL-CSP Package, 13 balls 0.5mm pitch 2.25x1.5x0.6mm, package size

3 Applications

Flash/torch/videolight for smartphones, feature-phones, tablets, DSCs, DVCs

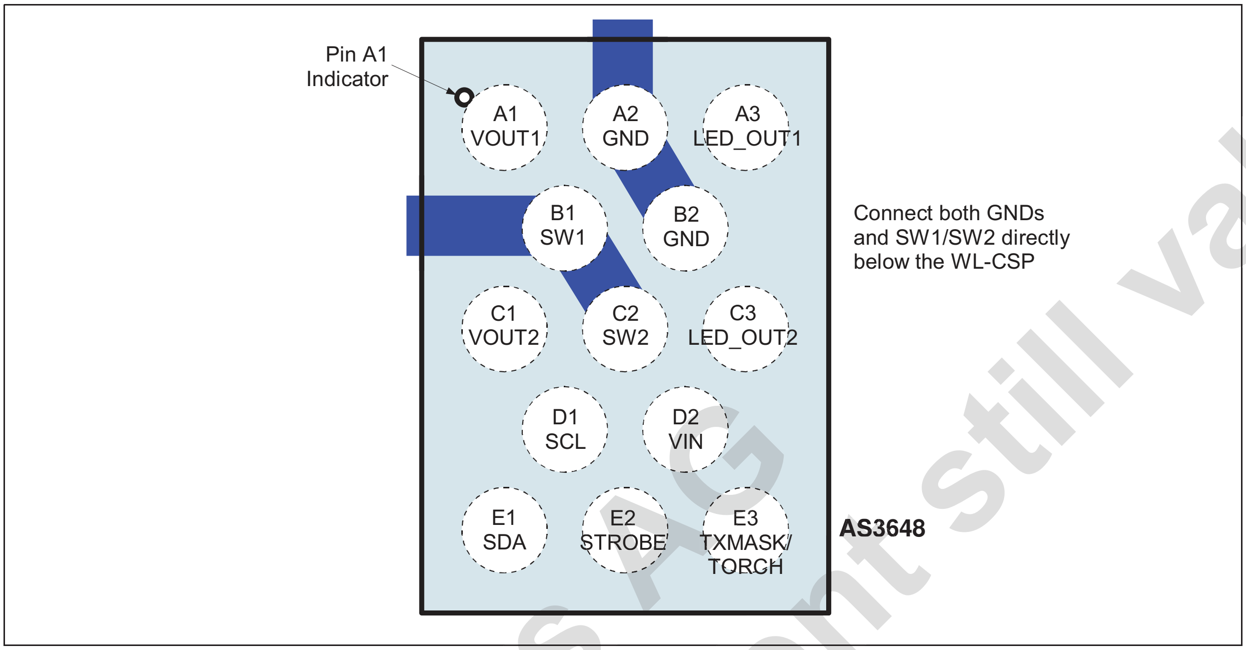
Figure 1. Typical Operating Circuit



4 Pinout

Pin Assignment

Figure 2. Pin Assignments (Top View)



Pin Description

Table 1. Pin Description for AS3648

Pin Number	Pin Name	Description
A1	VOUT1	DCDC converter output capacitor - make a short connection to C_{VOUT} / VOUT2
A2	GND	Power and analog ground; make a short connection between both balls
A3	LED_OUT1	Flash LED current sink
B1	SW1	DCDC converter switching node - make a short connection to SW2 / coil L_{DCDC}
B2	GND	Power and analog ground; make a short connection between both balls
C1	VOUT2	DCDC converter output capacitor - make a short connection to C_{VOUT} / VOUT1
C2	SW2	DCDC converter switching node - make a short connection to SW1 /coil L_{DCDC}
C3	LED_OUT2	Flash LED current sink
D1	SCL	serial clock input for I^2C interface
D2	VIN	Positive supply voltage input - connect to supply and make a short connection to input capacitor C_{VIN} and to coil L_{DCDC}
E1	SDA	serial data input/output for I^2C interface (needs external pullup resistor)
E2	STROBE	Digital input with pulldown to control strobe time for flash function
E3	TXMASK/ TORCH	Function 1: Connect to RF power amplifier enable signal - reduces currents during flash to avoid a system shutdown due to parallel operation of the RF PA and the flash driver Function 2: Operate torch current level without using the I^2C interface to operate the torch without need to start a camera processor (if the I^2C is connected to the camera processor

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 3 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Table 4, "Electrical Characteristics," on page 4 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
VIN to GND	-0.3	+7.0	V	
STROBE, TXMASK/TORCH, SCL, SDA to GND	-0.3	VIN + 0.3	V	max. +7V
SW1/2, VOUT1/2, LED_OUT1/2 to GND	-0.3	+7.0	V	
VOUT1/2 to SW1/2	-0.3		V	**Note:** Diode between VOUT1/2 and SW1/2
voltage between GND pins	0.0	0.0	V	short connection recommended
Input Pin Current without causing latchup	-100	+100 $+I_{IN}$	mA	Norm: EIA/JESD78
Continuous Power Dissipation (T_A = +70ºC)				
Continuous power dissipation		1230	mW	P_T at 70ºC[1]
Continuous power dissipation derating factor		16.7	mW/ºC	P_{DERATE}[2]
Electrostatic Discharge				
ESD HBM pins LED_OUT1/2[3]		±8000	V	Norm: JEDEC JESD22-A114F
ESD HBM		±2000	V	
ESD CDM		±500	V	Norm: JEDEC JESD 22-C101E
ESD MM		±100	V	Norm: JEDEC JESD 22-A115-B
Temperature Ranges and Storage Conditions				
Junction to ambient thermal resistance		60[4]	ºC/W	For more information about thermal metrics, see application note AN01 Thermal Characteristics
Junction Temperature		+150	ºC	Internally limited (overtemperature protection), max. 20000s
Storage Temperature Range	-55	+125	ºC	
Humidity	5	85	%	Non condensing
Body Temperature during Soldering		+260	ºC	according to IPC/JEDEC J-STD-020
Moisture Sensitivity Level (MSL)	MSL 1			Represents a max. floor life time of unlimited

1. Depending on actual PCB layout and PCB used measured on demoboard; for peak power dissipation during flashing see document 'AS3648 Thermal Measurements'
2. P_{DERATE} derating factor changes the total continuous power dissipation (P_T) if the ambient temperature is not 70ºC. Therefore for e.g. T_{AMB}=85ºC calculate P_T at 85ºC = P_T - P_{DERATE} * (85ºC - 70ºC)
3. Pins LED_OUT1 connected to LED_OUT2 and capacitor C_{VOUT} connected to VOUT1/2 and GND; both GND pins connected together
4. Measured on AS3648 Demoboard.

6 Electrical Characteristics

V_{VIN} = +2.7V to +4.4V, T_{AMB} = -30ºC to +85ºC, unless otherwise specified. Typical values are at V_{VIN} = +3.7V, T_{AMB} = +25ºC, unless otherwise specified.

Table 4. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
General Operating Conditions						
V_{VIN}	Supply Voltage	pin VIN	2.7	3.7	4.4	V
$V_{VINREDUCED\_FUNC}$	Supply Voltage	AS3648 functionally working, but not all parameters fulfilled	2.5		2.7	V
			4.4		5.5	
$I_{SHUTDOWN}$	Shutdown Current	TXMASK/TORCH=L, SCL=SDA=0V, V_{VIN}<3.7V		0.6	2.0	µA
I_{STANBY}	Standby Current	interface active, TXMASK/TORCH=L, V_{VIN}<3.7V[1]		1.0	10	µA
T_{AMB}	Operating Temperature		-30	25	85	ºC
Eta	Application Efficiency (DCDC and current sink)	L_{COIL}=0.6µH@3A, L_{ESR}=60mΩ, LED_OUT1,2=1300mA[2], t_{FLASH}<300ms		84		%
DCDC Step Up Converter						
V_{VOUT}	DCDC Boost output Voltage (pin VOUT1/2)		2.8		5.5	V
V_{VOUT5V}	DCDC Boost output Voltage (pin VOUT1/2)	constant voltage mode operation const_v_mode (see page 25)=1		5.0		V
R_{PMOS}	On-resistance	DCDC internal PMOS switch		70		mΩ
R_{NMOS}	On-resistance	DCDC internal NMOS switch		70		mΩ
f_{CLK}	Operating Frequency	All internal timings are derived from this oscillator	-7.5%	4.0	+7.5%	MHz
Current Sinks						
V_{LED}	LED forward voltage	two flash LEDs at 1800mA combined	2.8	3.5	3.95	V
		single flash LED at 1600mA	2.8		4.2	V
I_{LED_OUT}	LED_OUT1/2 current sinks output combined	dual flash LED, current_boost=1	0		2000[3]	mA
		dual flash LED, current_boost=0	0		1800	mA
		single flash LED			1600	mA
$I_{LED\_OUT\Delta}$	LED_OUT1/2 current sink accuracy	I_{LED_OUT}>=800mA or I_{LED_OUT}<500mA 0ºC < T_J < 100ºC	-7		+7	%
		500mA<I_{LED_OUT}<800mA, 0ºC < T_J < 100ºC	-5		+5	%
$I_{LED\_OUT\ RAMP}$	LED_OUT1/2 ramp time	Ramp-up During startup		250	1000	µs
		Ramp-down		500	1000	µs
$I_{LED\_OUT\ RIPPLE}$	LED_OUT current ripple	I_{LED_OUT} = 1000mA, BW=20MHz		20		mA_{PP}
V_{ILED_COMP}	LED_OUT current sink voltage compliance	Minimum voltage between pin LED_OUT1/2 and GND for operation of the current sink, current_boost=0		325		mV
		Minimum voltage between pin LED_OUT1/2 and GND for operation of the current sink, current_boost=1		360		mV

Table 4. Electrical Characteristics (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{LED\_OUTCOMP\_HYST}$	Comparators hysteresis	Hysteresis for comparators between LED_OUT1 and LED_OUT2 reporting signals led_out1above2 and led_out2above1		30		mV
V_{HIGH_VDS}	Comparator High VDS	low vds and high vds comparator - see 4MHz/ 1MHz Operating Mode Switching on page 11		900		mV
V_{LOW_VDS}	Comparator Low VDS			320		mV
$I_{LEAK\_LED\_OUT}$	LED_OUT1/2 Leakage Current	Pins LED_OUT1 and LED_OUT2	-1.0	0.0	+1.0	µA
Protection and Fault Detection Functions (see page 11)						
$V_{VOUTMAX}$	V_{VOUT} overvoltage protection	DCDC Converter Overvoltage Protection	5.0	5.3	5.6	V
I_{LIMIT}	Current Limit for coil L_{DCDC} (Pin SW) measured at 40% PWM duty cycle[4] maximum 40000s lifetime operation in overcurrent limit	coil_peak=00b	1.8	2.0	2.23	A
		coil_peak=01b	2.25	2.5	2.78	A
		default value; coil_peak (see page 23)=10b	2.7	3.0	3.34	A
		coil_peak=11b	3.15	3.5	3.9	A
$V_{LEDSHORT}$	Flash LED short circuit detection voltage	Voltage measured between pins VOUT1,2 and LED_OUT1,2		1.0		V
T_{OVTEMP}	Overtemperature Protection	Junction temperature		144		ºC
$T_{OVTEMPHYST}$	Overtemperature Hysteresis	Junction temperature		5		ºC
$t_{FLASHTIMEOUT}$	Flash Timeout Timer	Can be adjusted with register flash_timeout (page 26)	2		1280	ms
		accuracy	-7.5		+7.5	%
V_{UVLO}	Undervoltage Lockout	Falling V_{VIN}	2.25	2.4	2.5	V
		Rising V_{VIN}	V_{UVLO} +0.05	V_{UVLO} +0.1	V_{UVLO} +0.15	V
Digital Interface						
V_{IH}	High Level Input Voltage	Pins SCL, SDA. Pin TXMASK/TORCH in external torch mode (ext_torch_on=10)	1.26		V_{VIN}	V
V_{IL}	Low Level Input Voltage		0.0		0.54	V
$V_{IHFLASH}$	High Level Input Voltage	Pin STROBE. Pin TXMASK/TORCH for TxMask mode (ext_torch_on=01)[5]	0.7		V_{VIN}	V
$V_{ILFLASH}$	Low Level Input Voltage		0.0		0.54	V
V_{OL}	Low Level Output Voltage	pin SDA, I_{OL}=3mA			0.3	V
I_{LEAK}	Leakage current	Pins SCL, SDA	-1.0	0.0	+1.0	µA
I_{PD}	Pulldown current to GND[6]	Pins TORCH, STROBE and TXMASK/TORCH		36		µA
$t_{DEBTORCH}$	TORCH debounce time		6.3	9	11.7	ms
$t_{TIMEOUT}$	SCL timeout	In indicator, assist or flash mode, if SCL is low longer than this timeout, the AS3648 automatically enters shutdown mode	35		100	ms

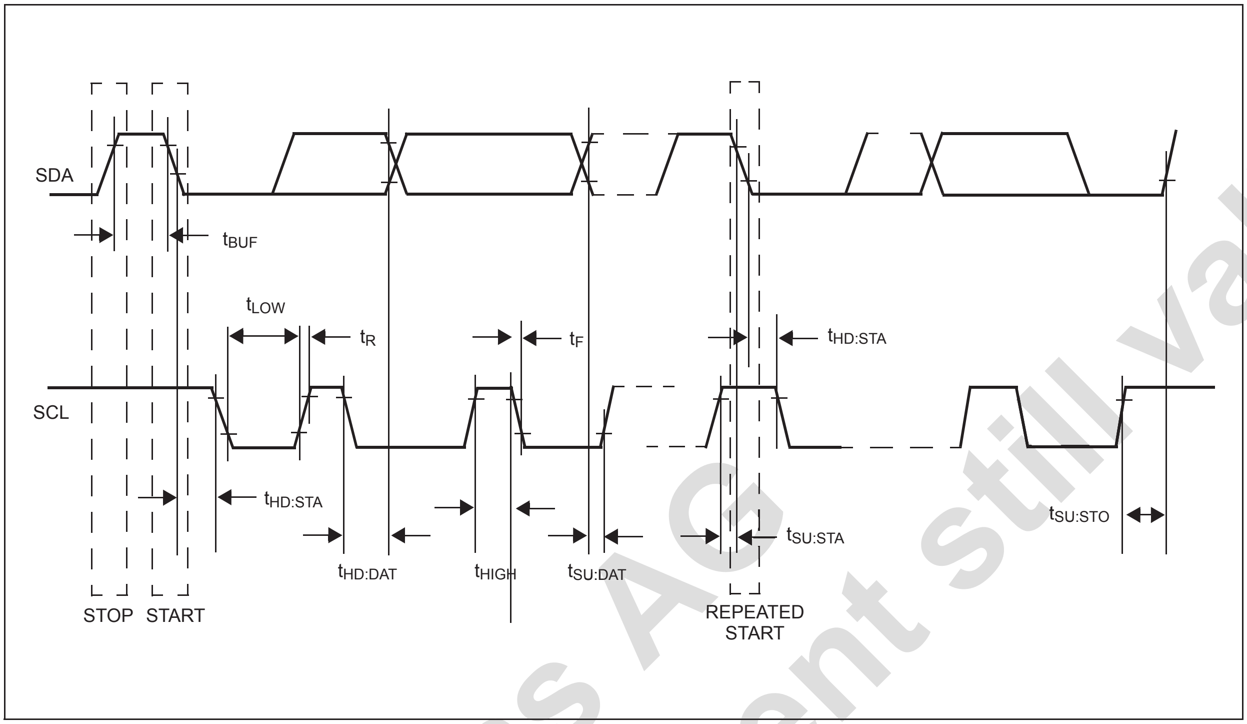
Table 4. Electrical Characteristics (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I^2C mode timings - see Figure 3 on page 7						
f_{SCLK}	SCL Clock Frequency		$1/t_{TIMEOUT}$		400	kHz
t_{BUF}	Bus Free Time Between a STOP and START Condition		1.3			µs
$t_{HD:STA}$	Hold Time (Repeated) START Condition[7]		0.6			µs
t_{LOW}	LOW Period of SCL Clock		1.3			µs
t_{HIGH}	HIGH Period of SCL Clock		0.6			µs
$t_{SU:STA}$	Setup Time for a Repeated START Condition		0.6			µs
$t_{HD:DAT}$	Data Hold Time[8]		0		0.9	µs
$t_{SU:DAT}$	Data Setup Time[9]		100			ns
t_R	Rise Time of Both SDA and SCL Signals		$20 + 0.1C_B$		300	ns
t_F	Fall Time of Both SDA and SCL Signals		$20 + 0.1C_B$		300	ns
$t_{SU:STO}$	Setup Time for STOP Condition		0.6			µs
C_B	Capacitive Load for Each Bus Line	C_B — total capacitance of one bus line in pF			400	pF
$C_{I/O}$	I/O Capacitance (SDA, SCL)				10	pF

1. For VBAT=4.5V, SCL=1.8V, SDA=1.8V maximum I_{STANBY} is <16µA.
2. To improve efficiency at low output currents, the active part of the internal switching transistor PMOS is reduced in size to 1/5 its original size. This reduces the current required to drive the PMOS transistor and therefore improves overall efficiency at low output currents.
3. The maximum current driving capability depends on supply voltageV_{VIN}, LED forward voltage and coil peak current limit.
4. Due to slope compensation of the current limit, I_{LIMIT} changes with duty cycle - see Figure 16 on page 10.
5. The logic input levels V_{IH} and V_{IL} allow for 1.2V or 1.8V supplied driving circuit
6. A pulldown current of 36µA is equal to a pulldown resistor of 42kΩ at 1.5V
7. After this period, the first clock pulse is generated.
8. A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
9. A fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT}$ = to 250ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_R max + $t_{SU:DAT}$ = 1000 + 250 = 1250ns before the SCL line is released.

Timing Diagrams

Figure 3. I^2C mode Timing Diagram



7 Typical Operating Characteristics

VVIN = 3.7V, T_A = +25ºC (unless otherwise specified), LED: Osram Phaser 2 (VFLED=3.8V at 1A)

Figure 4. DCDC Efficiency vs. VVIN

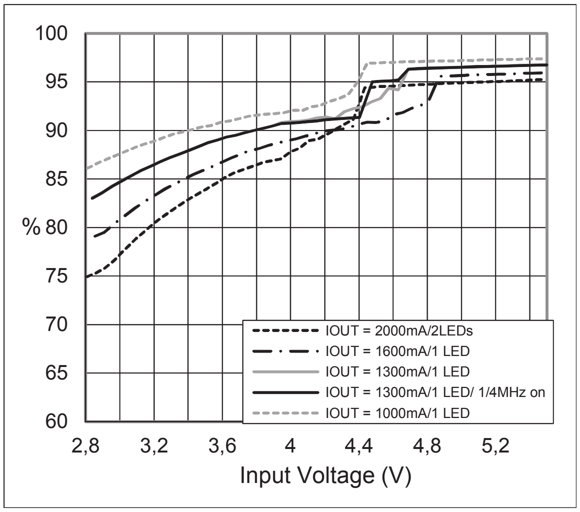


Figure 5. Application Efficiency (PLED/PVIN) vs. VVIN

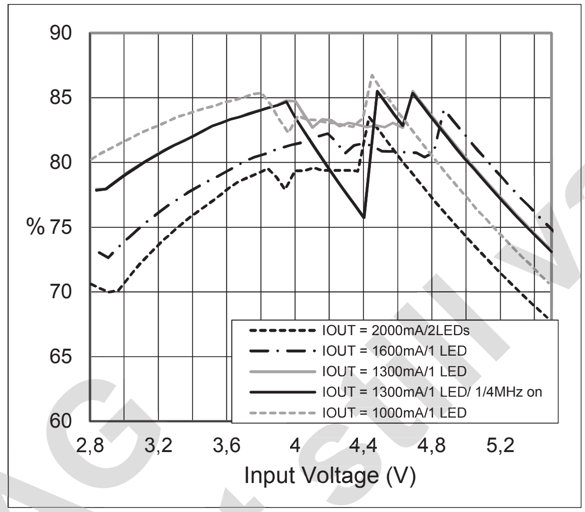


Figure 6. Battery Current vs. VVIN

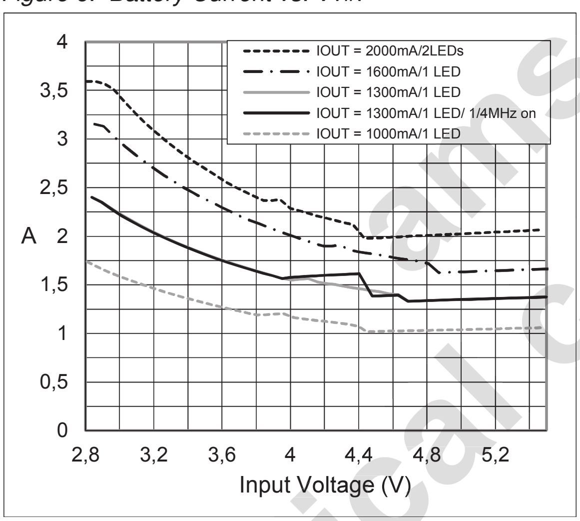


Figure 7. Efficiency at low currents (300mA)

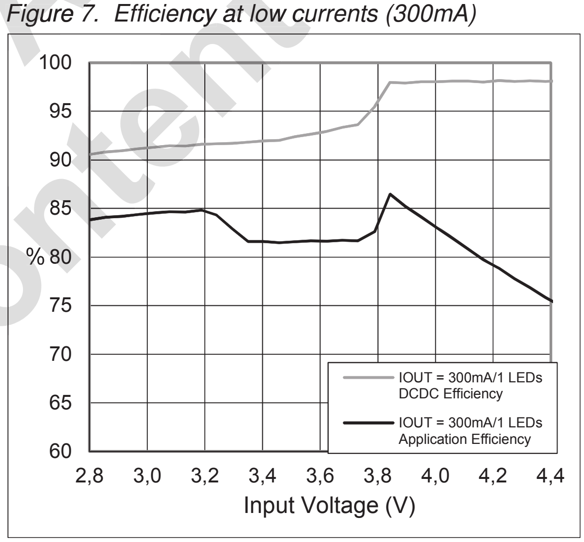


Figure 8. ILED Startup (ILED_OUT=1.0A)

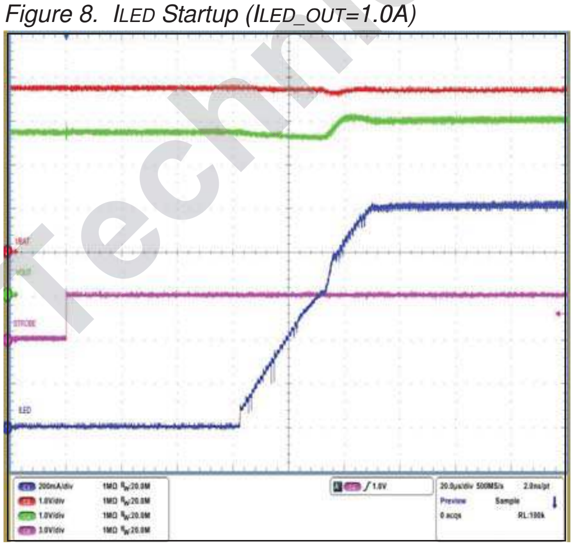


Figure 9. IVIN, ILED Startup (ILED_OUT=800mA)

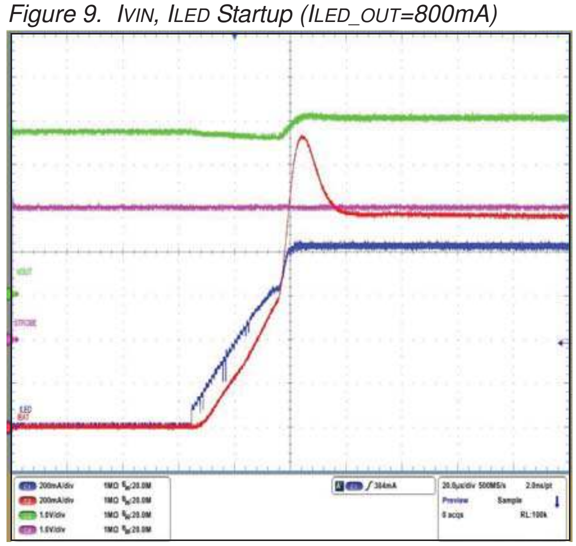


Figure 10. ILED Startup (ILED_OUT=60mA)

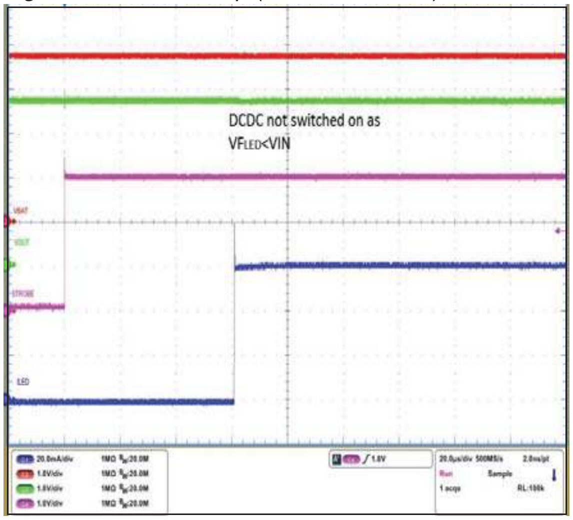


Figure 11. VOUT / ILED_OUT ripple, ILED_OUT = 1.0A

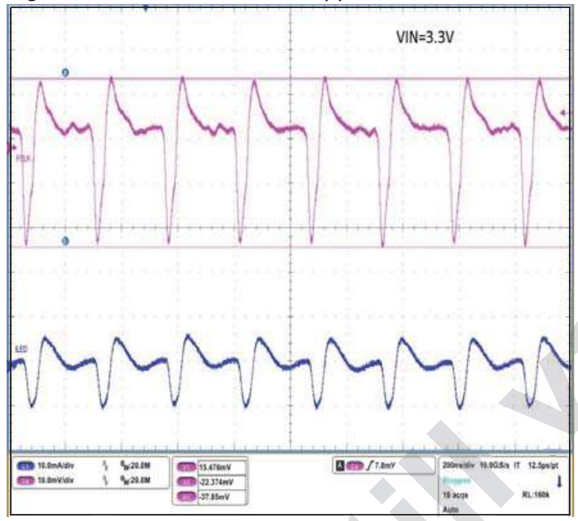


Figure 12. ILED Rampdown (ILED_OUT=1.0A)

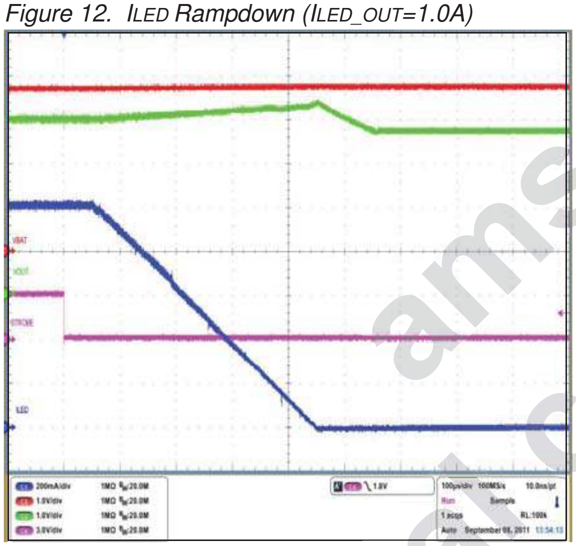


Figure 13. ILED_OUT vs. TAMB

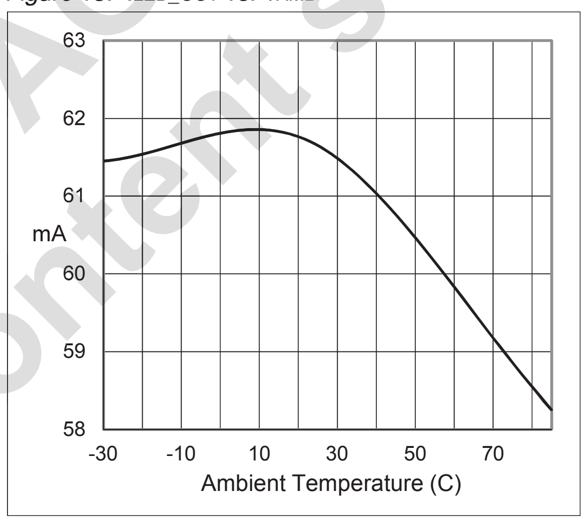


Figure 14. Oscillator frequency fCLK vs. TAMB

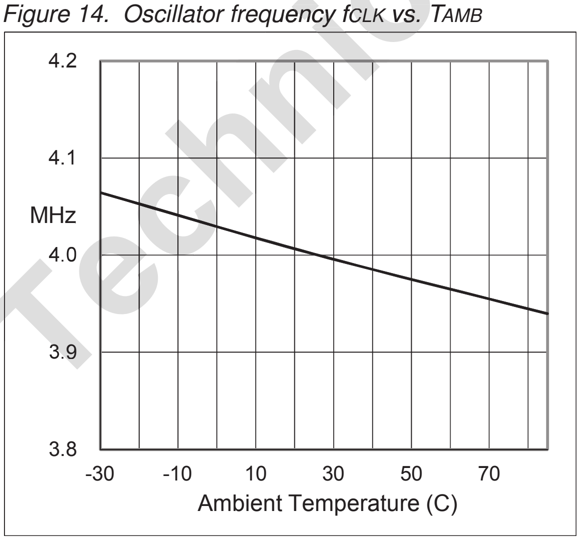
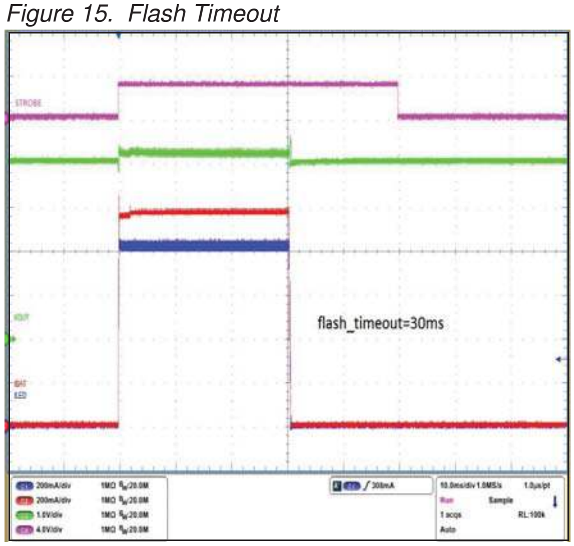


Figure 15. Flash Timeout



8 Detailed Description

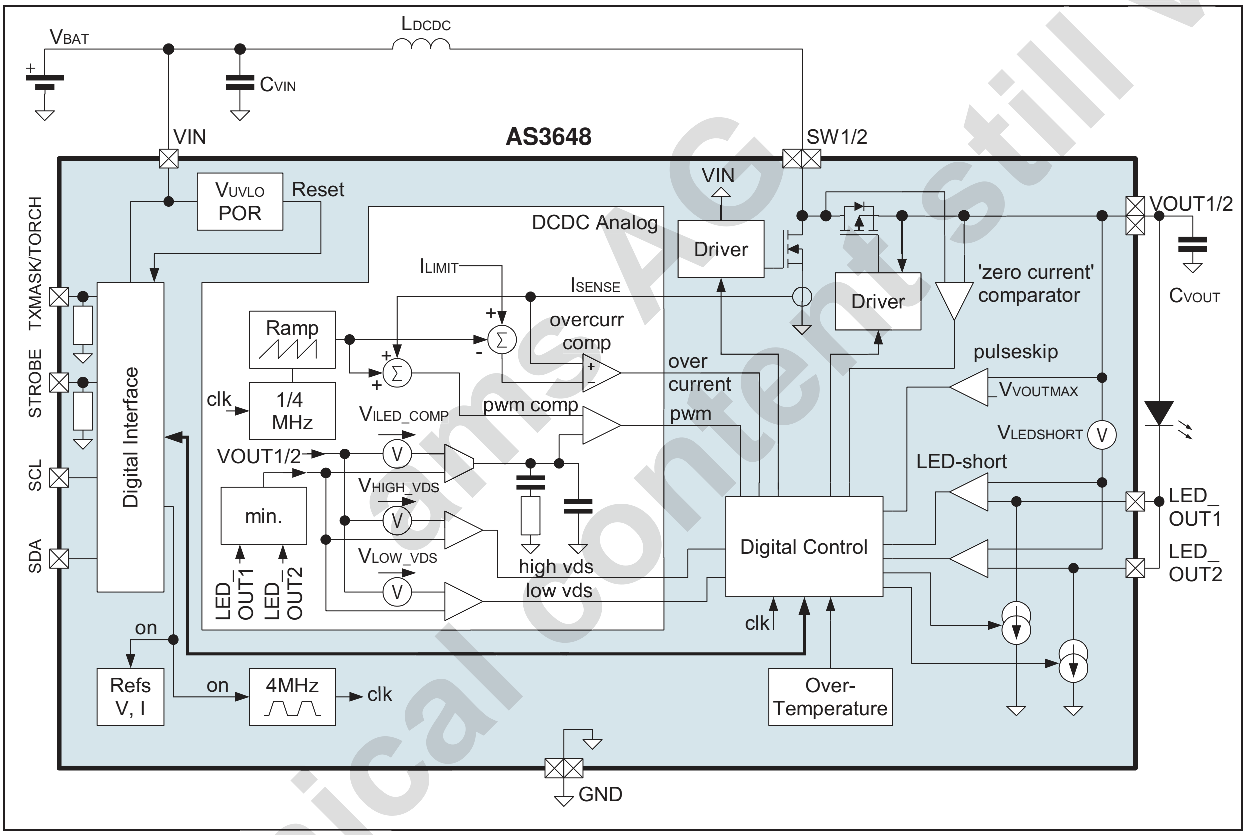
The AS3648 is a high performance DCDC step up converter with internal PMOS and NMOS switches. Its output is connected to one or two flash LEDs[1] with an internal current sink. The device is controlled by the pins SDA and SCL in I^2C mode.

The actual operating mode like standby, assist light, indicator or flash mode, can then be chosen by the interface. If not in standby mode, the device automatically enters shutdown mode by keeping SCL low for more than $t_{TIMEOUT}$[2].

The AS3648 includes a fixed frequency DCDC step-up with accurate startup control. Together with the current sink (on LED_OUT1/2) it includes several protection and safety functions.

Internal Circuit Diagram

Figure 16. Internal circuit Diagram



Softstart / Soft ramp down

During startup and ramp down the LED current is smoothly ramped up and ramped down. If the DCDC converter goes out of regulation (measured by monitoring the voltage across the current sinks), the ramp up is temporarily stopped in order for the DCDC to return to regulation[3].

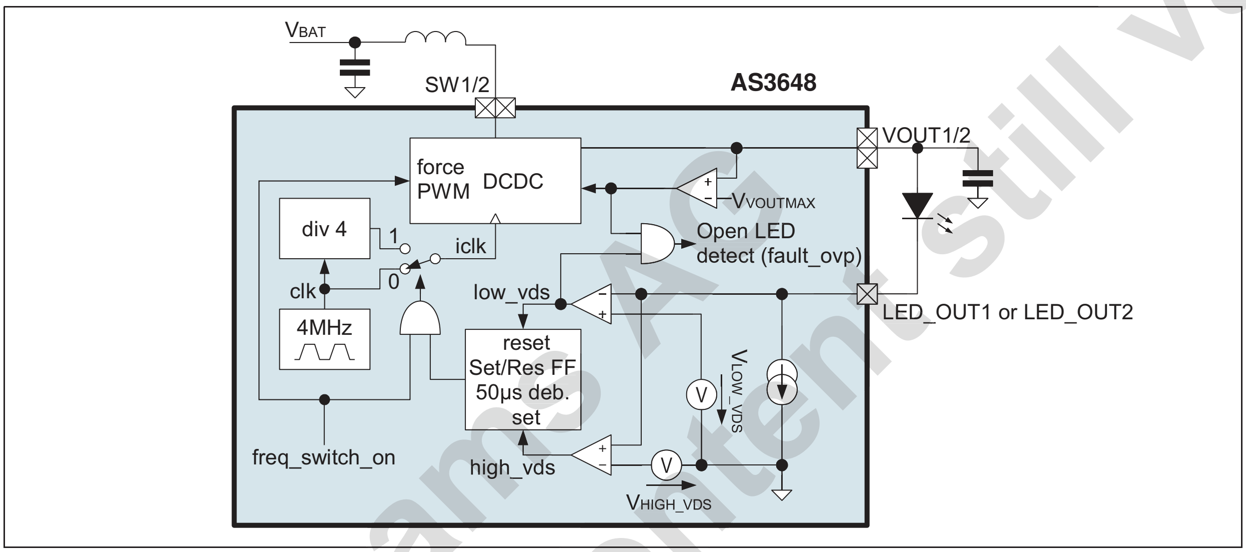
1. If two LEDs are connected, it is possible to operate each of the two LEDs individually as the LED current can be selected individually.
2. Following registers are reset to their default value if the timeout expires: out_on=0, ext_torch_on=00, mode_setting=00, const_v_mode=0.
3. The actual value of the LED current setting can be readout by the register led_current_actual (see page 29) to allow the camera processor to adopt to the actual operating conditions.

4MHz/1MHz Operating Mode Switching

If freq_switch_on (see page 28)=1 and in flash and assist light mode (indicator mode or low current mode using PWM mode -see mode_setting (page 26) - always will use pulseskip) if led_current1>=40h and led_current2>=40h and current_boost=0, the DCDC converter always operates in PWM mode (exception: PFM mode is allowed during startup) to reduce EMI in EMI sensitive systems. For flash and assist light mode and high duty cycles close to 100% on-time (maximum duty cycle) of the PMOS, the DCDC converter can switch into a 1MHz operating mode and maximum duty cycle to improve efficiency for this load condition[4]. The DCDC converter returns back to its normal 4MHz operating frequency when load or supply conditions change. Due to this switching between two fixed frequencies the noise spectrum of the system is exactly defined and predictable. If improved efficiency is required, the fixed switching between 1MHz / 4MHz can be disabled by freq_switch_on (see page 28)=0. In this case pulseskip will be used.

The internal circuit for switching between these two frequencies is shown in Figure 17:

Figure 17. Internal circuit of 4MHz/1Mhz selection



Note: For simplicity Figure 17 shows only a single current sink.

Protection and Fault Detection Functions

The protection functions protect the AS3648 and the LED(s) against physical damage. In most cases a Fault register bit is set, which can be readout by the I²C interface. The fault bits are automatically cleared by a I²C readout of the fault register. Additionally the DCDC is stopped and the current sinks are disabled[5] by resetting out_on=0, mode_setting=00 and ext_torch_on=00.

Overvoltage Protection

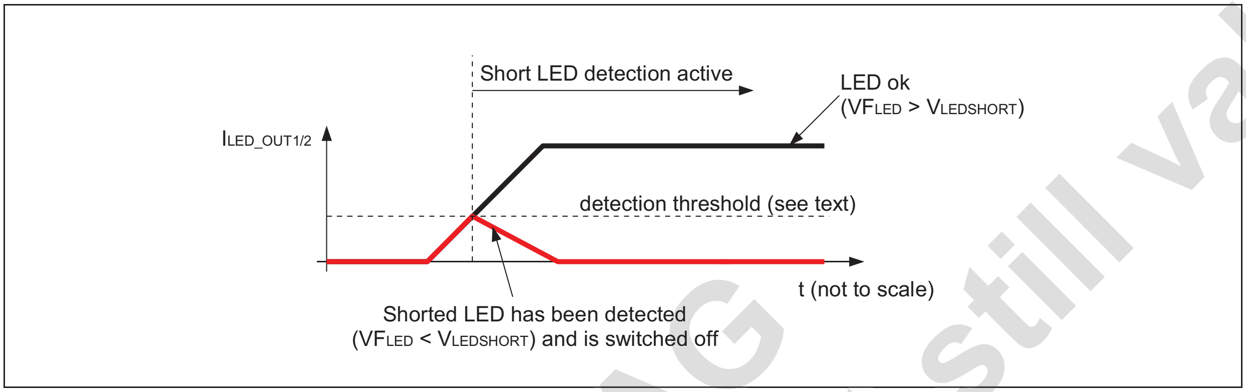
In case of no or a broken LED(s) at the pin LED_OUT1/2 and an enabled DCDC converter, the voltage on VOUT1/2 rises until it reaches $V_{VOUTMAX}$ (overvoltage condition) and the voltage across the current source is below low_vds[6]., the DCDC converter is stopped, the current sources are disabled and the bit fault_ovp (see page 28) is set[7].

4. Efficiency compared to a 4MHz only DCDC converter forced to operate with minimum duty cycle.
5. Applies for all faults except TXMASK event occurred
6. If overvoltage is reached, but none of the low_vds comparator(s) triggers, VOUT1/2 is still regulated below $V_{VOUTMAX}$.
7. In constant voltage mode (5V generation, register bit const_v_mode=1) this fault is disabled.

Short Circuit Protection

After the startup of the DCDC converter, the voltage on LED_OUT1/2 is continuously monitored and compared against $V_{LEDSHORT}$ if the LED current is above 14mA[8] (current_boost=0), 15.6mA (current_boost=1)[9](see Figure 18). If the voltage across the LED (VF_{LED} = VOUT1/2-LED_OUT1/2) stays below $V_{LEDSHORT}$, the DCDC is stopped (as a shorted LED is assumed), the current sinks are disabled and the bit fault_led_short (see page 28) is set. In a dual LED configuration for the AS3648, if a single shorted LED is detected, this LED is disabled and the device continuous operation with the other LED.

Figure 18. Short LED detection



Overtemperature Protection

The junction temperature of the AS3648 is continuously monitored. If the temperature exceeds T_{OVTEMP}, the DCDC is stopped, the current sinks are disabled (instantaneous) and the bit fault_overtemp (see page 28) is set. The driver is automatically re-enabled[10] once the junction temperature drops below T_{OVTEMP}-$T_{OVTEMPHYST}$.

TXMASK event occurred

If during flash, TXMASK current reduction is enabled (see TXMASK on page 14, configured by ext_torch_on=01) and a TXMASK event happened (pin TXMASK/TORCH=1), the fault register bit fault_txmask (see page 27) is set.

Flash Timeout

If the flash is started a timeout timer is started in parallel. If the flash duration defined by the STROBE input (strobe_on = 1 and strobe_type = 1, see Figure 26 on page 18) exceeds $t_{FLASHTIMEOUT}$ (adjustable by register flash_timeout (see page 26)), the DCDC is stopped and the flash current sinks (on pin LED_OUT1/2) are disabled and fault_timeout is set.

If the flash duration is defined by the timeout timer itself (strobe_on = 0, see Figure 24 on page 17), the register fault_timeout is set after the flash has been finished.

Supply undervoltage Protection

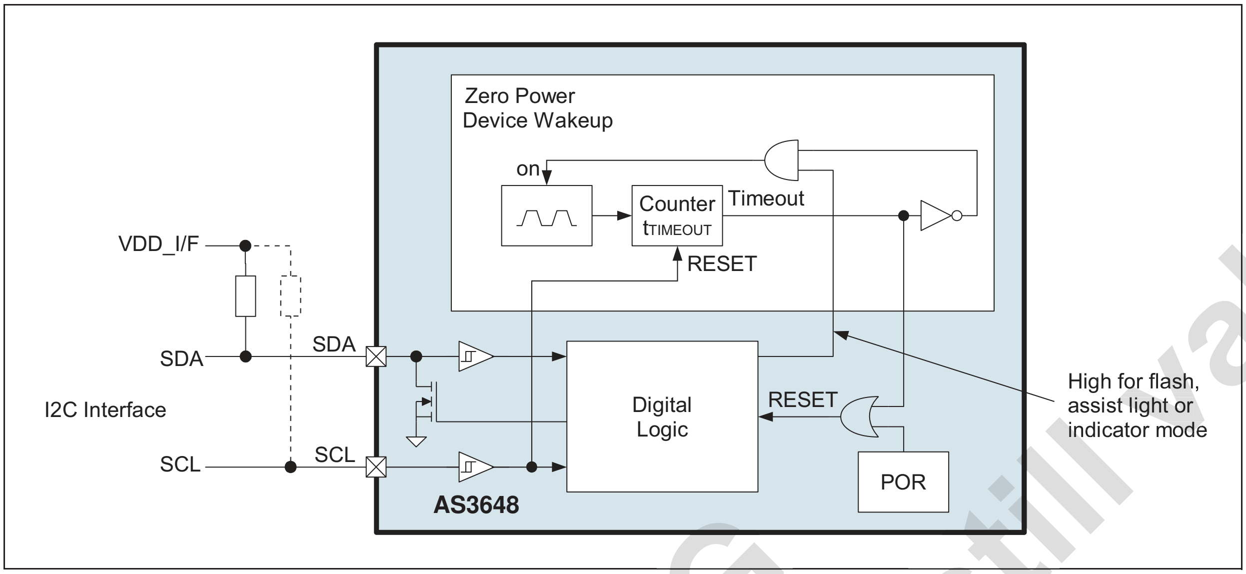
If the voltage on the pin VIN (=battery voltage) is or falls below V_{UVLO}, the AS3648 is kept in shutdown state and all registers are set to their default state.

Wakeup Circuit - Power off detection

In flash, assist light and indicator mode (register mode_setting (page 26)=01, 10 or 11) and out_on (page 27)=1, if SCL is L for more than $t_{TIMEOUT}$, shutdown mode is automatically entered. This feature automatically detects a power-off of the controlling circuit driving SCL and SDA (VDD_I/F goes to 0V e.g. due to a low power condition of the driving circuit) - the internal circuit is shown in Figure 19:

8. Measured for each LED_OUT1/2 pin
9. To avoid errors in short LED detection for LEDs with a high leakage current
10. In constant voltage mode (const_v_mode=1) the DCDC will not be automatically re-enabled.

Figure 19. Device Shutdown and Wakeup



In shutdown mode once pin SCL goes high for the first time, the internal counter shown in Figure 19 is immediately reset thus releasing the internal RESET (assuming VIN is above V_{UVLO}) signal and allows instant communication on the I^2C bus. Therefore no additional action is required to leave the shutdown mode and start I^2C communication.

Purpose of this circuit

The purpose of this circuit is an additional security mechanism.

Assume the user programmed torch or indicator operation (there is no timeout for these operating modes) and the battery slowly drops below the undervoltage limit of the system. The processor would get an reset by the PMIC and the LDO operating VDD_I/F is switched off, but the processor might not have been able to switch-off the torch/indicator operation of the AS3648. Due to the implemented security mechanism the AS3648 detects a power off of VDD_I/F and automatically enters shutdown.

Current consumption in standby/shutdown mode

The AS3648 is designed to draw minimum current in standby and shutdown mode. There is a small difference in current consumption between these two operating modes (typ. 300nA) only due to the internal level shifters (see the schmitt trigger input buffers connected to SCL and SDA in Figure 19) for shifting up the voltage on SCL/SDA (VDD_I/F e.g. 1.8V) to the supply voltage on VIN (e.g. 3.7V). If the AS3648 is driven with digital levels close to 0V/VIN, the current consumption for standby mode is identical to shutdown mode.

Operating Mode and Currents

The output currents and operating mode are selected according to the following table:

Table 5. Operating Mode and current settings

AS3648 configuration						operating mode and currents	
SCL and SDA	TORCH	STROBE	mode_setting (see page 26)	out_on (see page 27)	Condition	Mode	LED_OUT1/2 output current
SCL low for $t_{TIMEOUT}$[1]	X	X	X	X	if previous operating mode was indicator, assist light or flash mode	shutdown all registers are reset to their default values	0

Table 5. Operating Mode and current settings (Continued)

AS3648 configuration						operating mode and currents	
SCL and SDA	TORCH	STROBE	mode_setting (see page 26)	out_on (see page 27)	Condition	Mode	LED_OUT1/2 output current
I^2C commands are accepted	X	X	10, 01 or 11	0		standby	0
	X	X	00	X	ext_torch_on (see page 23) not 10		
	0	X			ext_torch_on =10		
	1	X			ext_torch_on =10	external torch mode	LED current is defined by the 7LSB[2] bits of led_current1 and led_current2
	X	X	01	1		indicator mode or low current pwm mode[3]	LED current is defined by the 6LSB bits (bits 5...0) of led_current1 and led_current2 pwm modulated with 31.25kHz defined by register inct_pwm (1/16...4/16)
	X	X	10	1		assist light mode	LED current is defined by the 7LSB[2] bits (6...0) of led_current1 and led_current2
	X	X	11	1	strobe_on (see page 27) = 0	flash mode; flash duration defined by flash_timeout (see page 26)	LED current is defined by led_current1 and led_current2 - the current can be reduced during flash, see Flash Current Reductions below
	X	0->1			strobe_on = 1 and strobe_type (see page 27) = 0		
	X	1			strobe_on = 1 and strobe_type = 1	flash mode; flash duration defined by STROBE input; timeout defined by flash_timeout	

1. SCL low for tTIMEOUT and operating mode is indicator, assist or flash mode then shutdown mode is entered.
2. The MSB bit of this register not used to protect the LED; therefore the maximum assist / torch light current = half the maximum flash current
3. The low current mode is a general purpose PWM mode to drive less current through the LED in average, but keep the actual pulsed current in a range where the light output from the LED is still specified. As only the 6 LSBs of led_current1 and led_current2 are used the maximum current is limited to 1/4 of the maximum flash current.

Flash Current Reductions

TXMASK

Usually the flash current is defined by the register led_current1 and led_current2. If the TXMASK/TORCH input is used and (configured by ext_torch_on=01), the flash current is reduced to flash_txmask_current if TXMASK/TORCH=1.

Current Reduction by VIN measurements in Flash Mode

Due to the high load of the flash driver and the ESR of the battery (especially critical at low temperatures), the voltage on the battery drops. If the voltage drops below the reset threshold of the system would reset. To prevent this condition the AS3648 monitors the battery voltage and keeps it above vin_low_v_run as follows:

Before a flash is started the voltage on VIN is measured. If the voltage is below the setting of vin_low_v the fault_uvlo (see page 27) is set and the flash is disabled (driver stays in shutdown) if vin_low_v_shutdown=1. The flash current is reduced to flash_txmask_current if vin_low_v_shutdown=0.

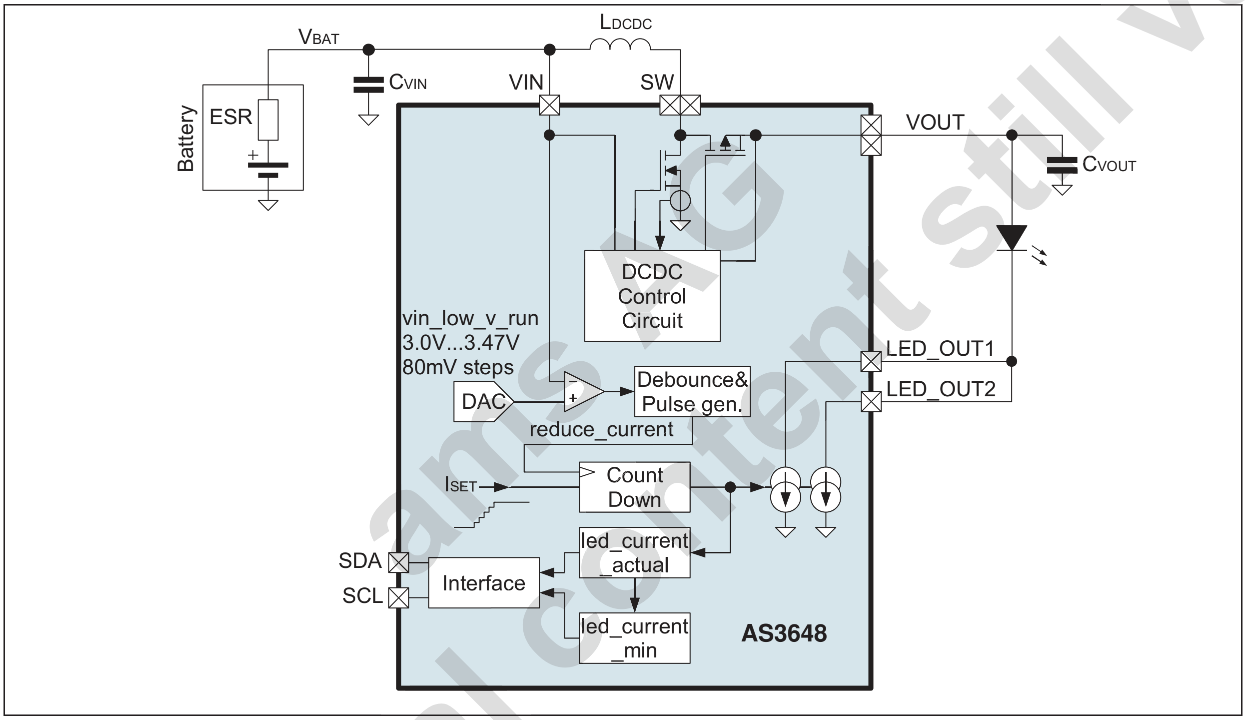
During flash, if the voltage on VIN drops below the threshold defined by vin_low_v_run, the flash current is reduced (or ramping of the current is stopped during flash current startup) and fault_uvlo is set. The timing for the reduction of the current is 8µs/LSB current change.

During the flash pulse the actual used current can be readout by the register led_current_actual.

After the flash pulse the minimum current can be readout by the register led_current_min - this allows to adjust the camera sensitivity (gain or iso-settings) for the subsequent flash pulse (e.g. when using a pre-flash and a main flash pulse).

The internal circuit for low voltage current reductions are shown in Figure 20:

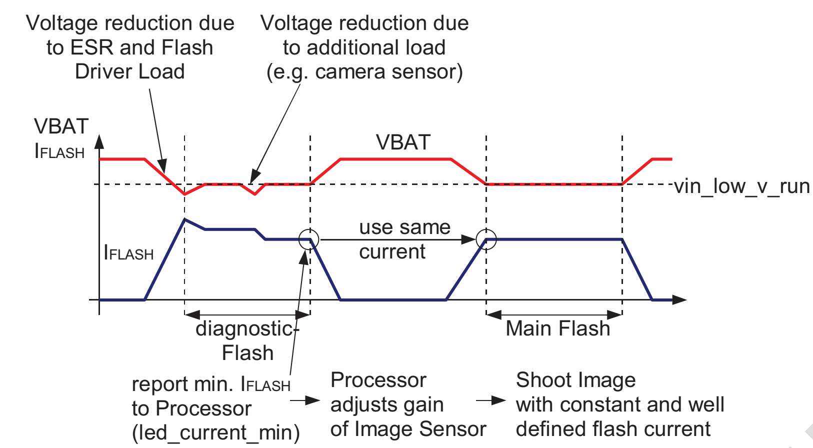
Figure 20. Low Voltage current Reduction Internal Circuit



A mobile phone camera flash system can trigger a diagnostic flash and a main-flash:

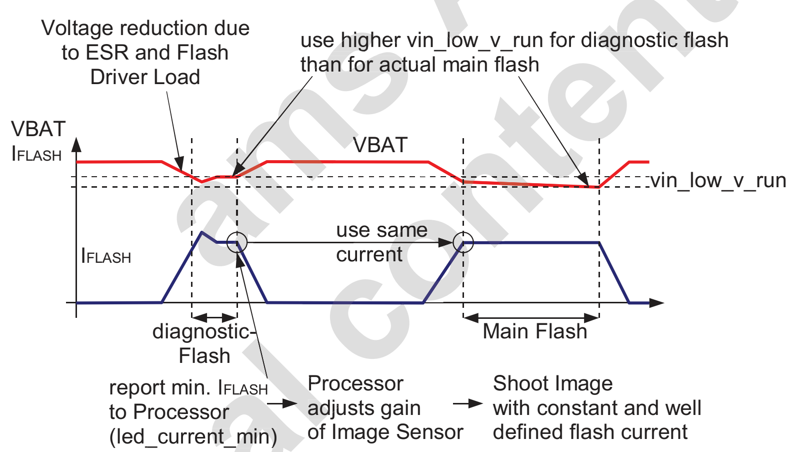
The diagnostic flash is initiated by the processor. After this diagnostic flash, the determined maximum flash current can be read back through the I^2C interface from register led_current_min (see page 29) and used for the setting for the main flash. Therefore the current in the main-flash is constant and additionally the camera system can use this current for picture quality adjustments - the waveforms for this concept are shown in Figure 21:

Figure 21. Low Voltage current Reduction Waveform with diagnostic-Flash and Main-Flash Phase



If the diagnostic flash should be short (e.g. 10ms) it is recommended to operate this diagnostic flash at slightly higher vin_low_v_run setting compared to the main flash as shown in Figure 22:

Figure 22. Low Voltage current Reduction Waveform with short diagnostic-Flash and Main-Flash Phase

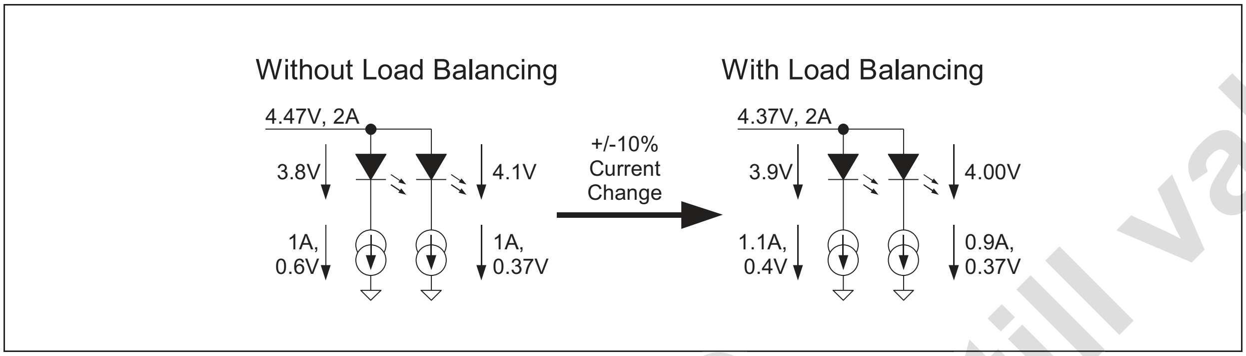


The different settings for vin_low_v_run allow a constant main flash current without dropping VIN below vin_low_v_run.

Load Balancing

To improve the efficiency of the AS3648 for LEDs with unmatched forward voltage and reduce the internal power dissipation of the AS3648, set the bit load_balance_on=1. This bit can change the currents through the LEDs by up to +/-15% (up to 115%/85% of set current between LED_OUT1 to LED_OUT2) to match the forward voltage of the LED better as shown in Figure 23:

Figure 23. Load Balancing



Flash Strobe Timings

The flash timing are defined as follows:

1. Flash duration defined by register flash_timeout and flash is started immediately when this mode is selected by the I^2C command (see Figure 24):
   set strobe_on = 0, start the flash by setting out_on = 1
2. Flash duration defined by register flash_timeout and flash started with a rising edge on pin STROBE (see Figure 25):
   set strobe_on = 1 and strobe_type = 0
3. Flash start and timing defined by the pin STROBE; the flash duration is limited by the timeout timer defined by flash_timeout (see Figure 26 and Figure 34):
   set strobe_on = 1 and strobe_type = 1

Figure 24. AS3648 flash duration defined by flash_timeout without using STROBE input

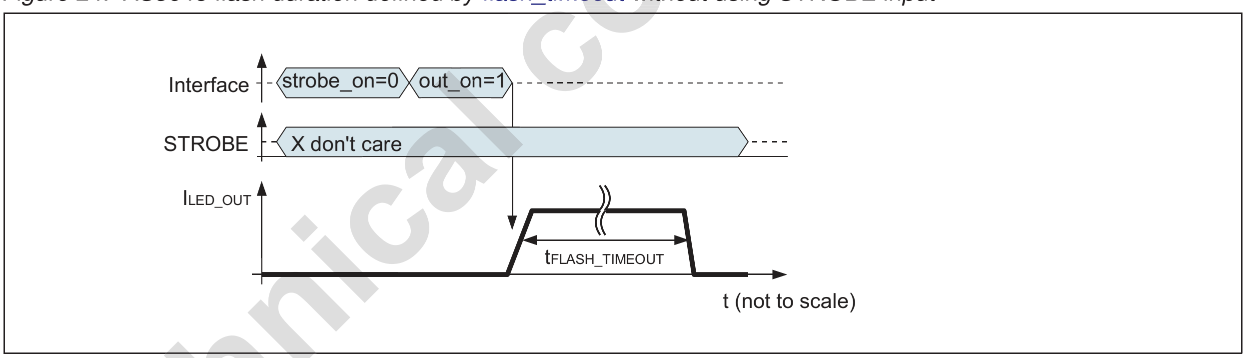


Figure 25. AS3648 flash duration defined by flash_timeout, starting flash with STROBE rising edge

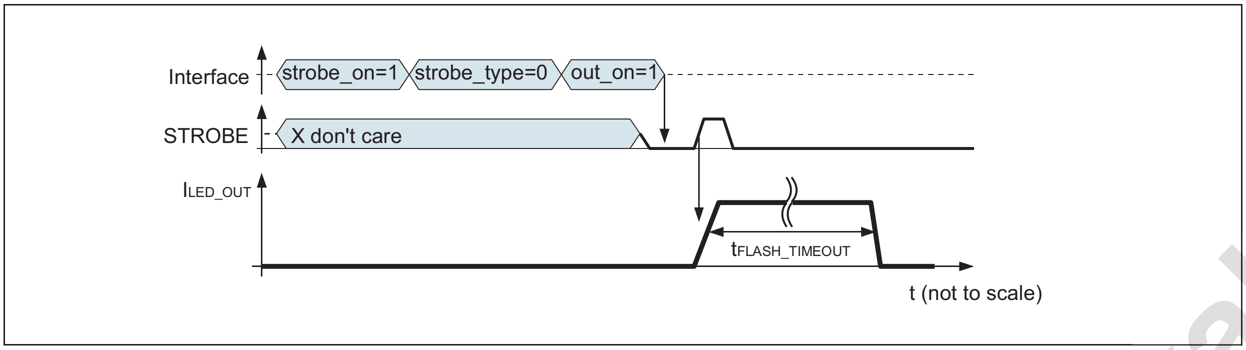


Figure 26. AS3648 flash duration and start defined by STROBE, limited by flash_timeout; timer not expired

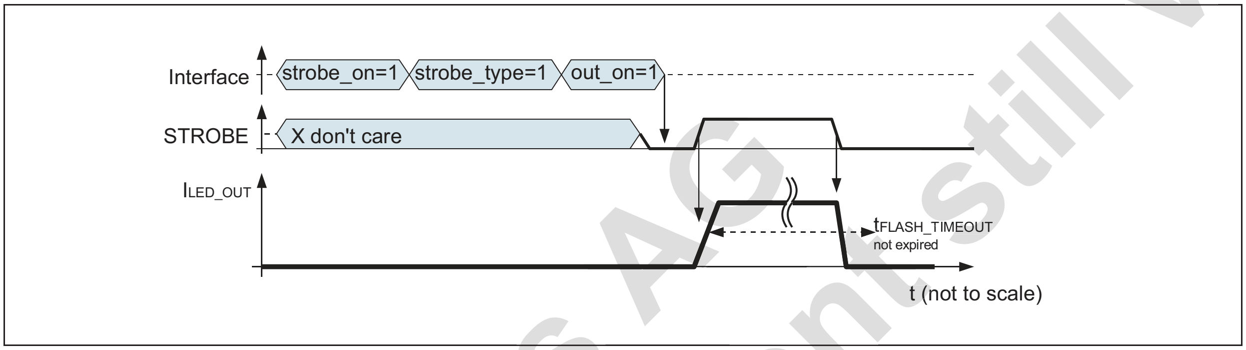
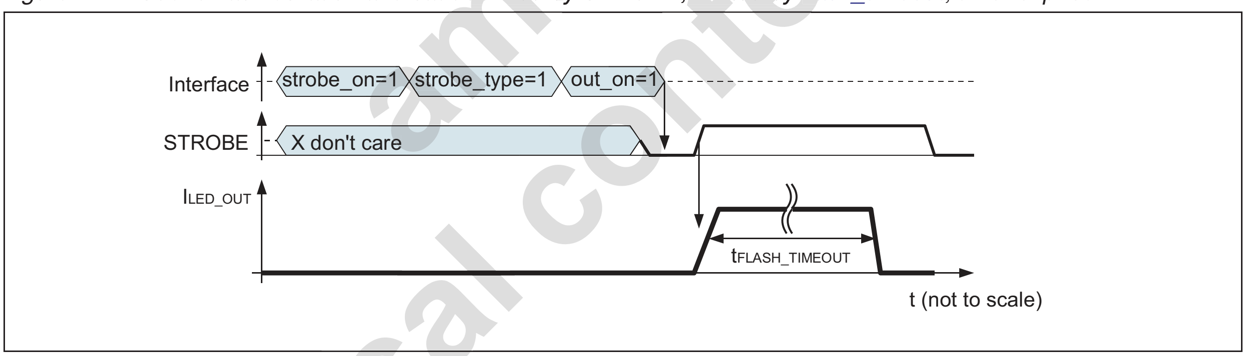


Figure 27. AS3648 flash duration and start defined by STROBE, limited by flash_timeout; timer expired



I²C Serial Data Bus

The AS3648 supports the I²C bus protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are referred to as slaves. A master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions must control the bus. The AS3648 operates as a slave on the I²C bus. Within the bus specifications a standard mode (100kHz maximum clock rate) and a fast mode (400kHz maximum clock rate) are defined. The AS3648 works in both modes. Connections to the bus are made through the open-drain I/O lines SDA and SCL.

The following bus protocol has been defined (Figure 28):

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus Not Busy

Both data and clock lines remain HIGH.

Start Data Transfer

A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop Data Transfer

A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data Valid

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

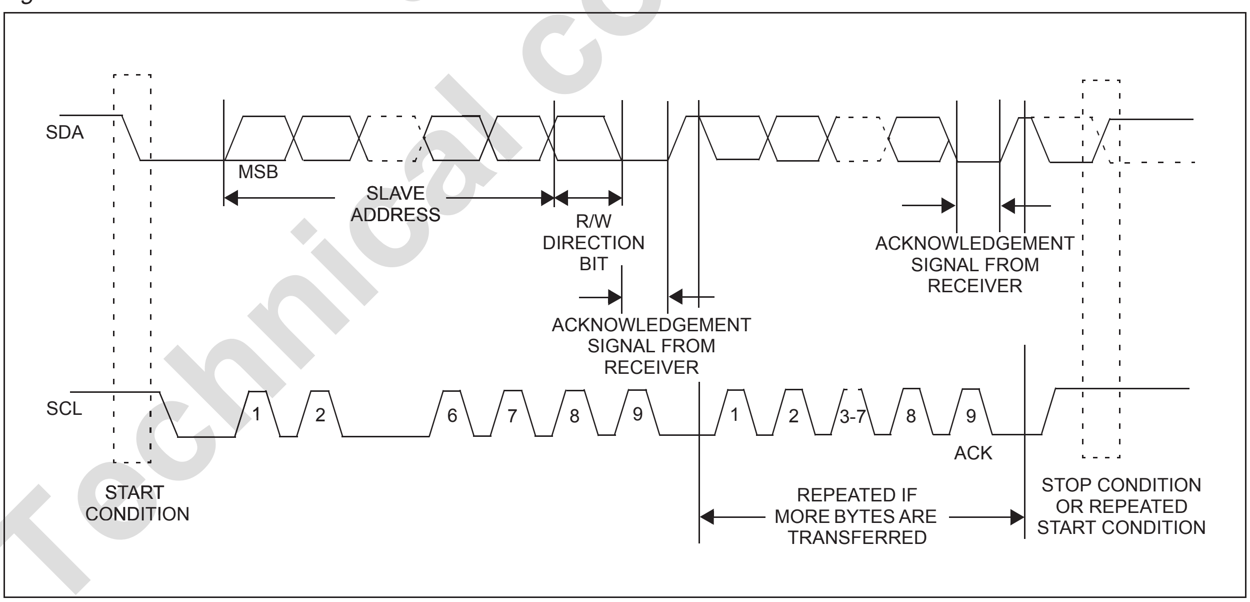
Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions are not limited, and are determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

Figure 28. Data Transfer on I²C Serial Bus



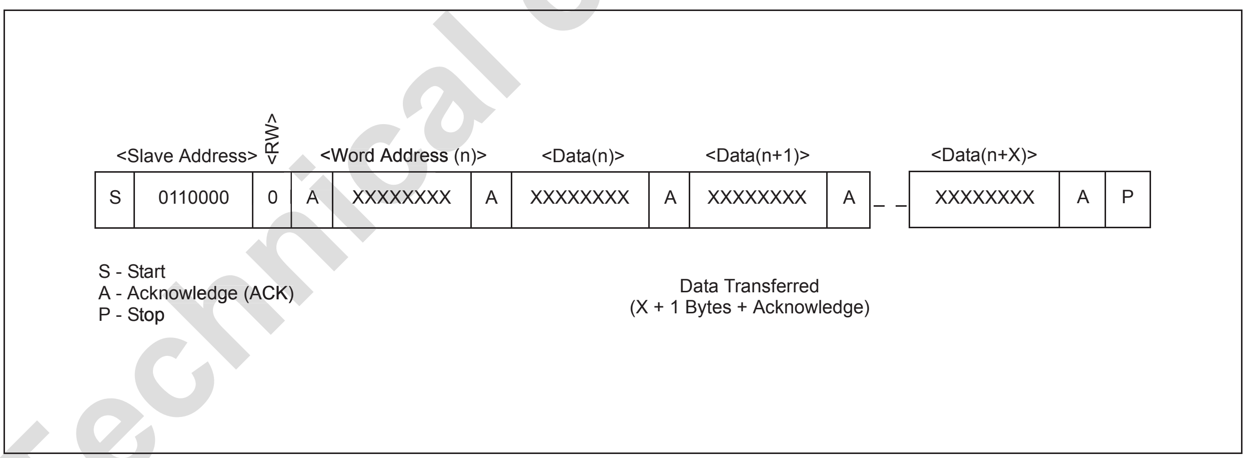
Depending upon the state of the R/W bit, two types of data transfer are possible:

1. **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first.
2. **Data transfer from a slave transmitter to a master receiver.** The master transmits the first byte (the slave address). The slave then returns an acknowledge bit, followed by the slave transmitting a number of data bytes. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a “not acknowledge” is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus is not released. Data is transferred with the most significant bit (MSB) first.

The AS3648 can operate in the following two modes:

1. **Slave Receiver Mode (Write Mode):** Serial data and clock are received through SDA and SCL. After each byte is received an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit (see Figure 29). The slave address byte is the first byte received after the master generates the START condition. The slave address byte contains the 7-bit AS3648 address, which is 0110000, followed by the direction bit (R/W), which, for a write, is 0.[11] After receiving and decoding the slave address byte the device outputs an acknowledge on the SDA line. After the AS3648 acknowledges the slave address + write bit, the master transmits a register address to the AS3648. This sets the register pointer on the AS3648. The master may then transmit zero or more bytes of data, with the AS3648 acknowledging each byte received. The address pointer will increment after each data byte is transferred. The master generates a STOP condition to terminate the data write.
2. **Slave Transmitter Mode (Read Mode):** The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the AS3648 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer (Figure 30 and Figure 31). The slave address byte is the first byte received after the master generates a START condition. The slave address byte contains the 7-bit AS3648 address, which is 0110000, followed by the direction bit (R/W), which, for a read, is 1.[12] After receiving and decoding the slave address byte the device outputs an acknowledge on the SDA line. The AS3648 then begins to transmit data starting with the register address pointed to by the register pointer. If the register pointer is not written to before the initiation of a read mode the first address that is read is the last one stored in the register pointer. The AS3648 must receive a “not acknowledge” to end a read.

Figure 29. Data Write - Slave Receiver Mode



11.The address for writing to the AS3648 is 60h = 01100000b
12.The address for read mode from the AS3648 is 61h = 01100001b

Figure 30. Data Read (from Current Pointer Location) - Slave Transmitter Mode

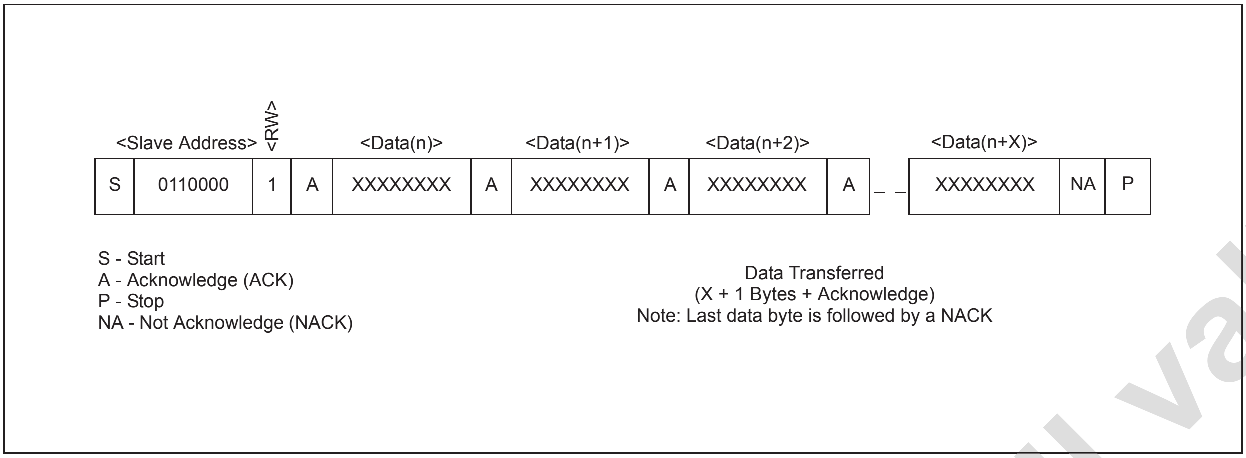
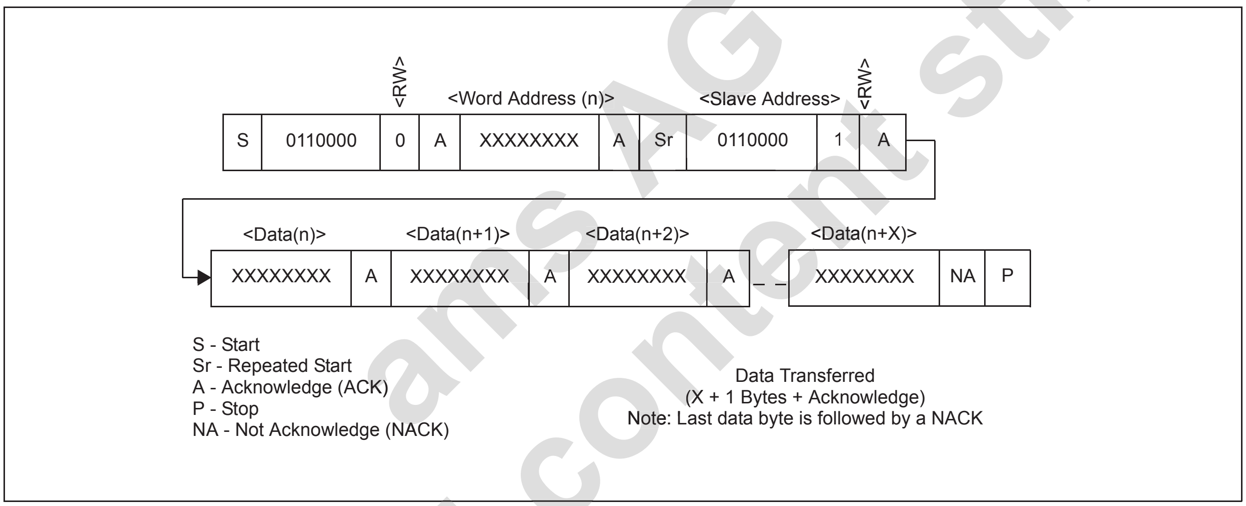


Figure 31. Data Read (Write Pointer, Then Read) - Slave Receive and Transmit



Register Description

Table 6. ChipID Register

Addr: 0		ChipID Register This register has a fixed ID		
Bit	**Bit Name**	**Default**	**Access**	**Description**
2:0	version	Xh	R	AS3648 chip version number
7:3	fixed_id	10110b	R	This is a fixed identification (e.g. to verify the I^2C communication)

Table 7. Current Set LED1 Register

Addr: 1		Current Set LED1 Register This register defines design versions			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7:0	led_current1	9Ch	R/W	**Caution:** Define the current on pin LED_OUT1assist mode uses bits 6:0 of this current setting (max. half of full current setting) indicator or low current pwm mode uses only 5:0 of this current setting (max. 1/4 of full current setting)	
				0h	0mA
				1h	3.5mA
				2h	7.1mA
				...	...
				3Fh	222.4mA (maximum current for indicator or low current pwm mode, mode_setting=01)
				...	...
				7Fh	448.2mA (maximum current for assist light mode, mode_setting=10)
				...	...
				9Ch	551mA - default setting
				...	...
				FEh	896.5mA (996.1mA[1] if current_boost=1)
				FFh	900mA (1000mA[1] if current_boost=1)

1. Do not use current_boost=1 for currents <= 900mA

Table 8. Current Set LED2 Register

Addr: 2		Current Set LED2 Register This register defines LED Currents			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7:0	led_current2	9Ch	R/W	Define the current on pin LED_OUT2 in flash mode assist mode uses bits 6:0 of this current setting (max. half of full current setting) indicator or low current pwm mode uses only 5:0 of this current setting (max. 1/4 of full current setting)	
				0h	0mA
				1h	3.5mA
				2h	7.1mA
				...	...
				3Fh	222.4mA (maximum current for indicator or low current pwm mode, mode_setting=01)
				...	...
				7Fh	448.2mA (maximum current for assist light mode, mode_setting=10)
				...	...
				9Ch	551mA - default
				...	...
				FEh	896.5mA (996.1mA[1] if current_boost=1)
				FFh	900mA (1000mA[1] if current_boost=1)

1. Do not use current_boost=1 for currents <= 900mA

Table 9. TXMask Register

Addr: 3		TXMask Register This register defines the TXMask settings and coil peak current			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
1:0	ext_torch_on	00	R/W	Defines operating mode for input pin TXMASK/TORCH	
				00	pin has no effect
				01	txmask-mode; during flash if TXMASK/TORCH=1, the LED current is set to flash_txmask_current - (see TXMASK on page 14)
				10	external torch mode: if TXMASK/TORCH=1 and mode_setting=00, the AS3648is set into external torch mode (LED current is defined by the 7LSB[1] bits of led_current1 and led_current2)
				11	don't use
3:2	coil_peak	10	R/W	Defines the maximum coil current (parameter I_{LIMIT})	
				00	I_{LIMIT} = 2.0A
				01	I_{LIMIT} = 2.5A
				10	I_{LIMIT} = 3.0A
				11	I_{LIMIT} = 3.5A

Table 9. TXMask Register (Continued)

Addr: 3		TXMask Register This register defines the TXMask settings and coil peak current			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7:4	flash_txmask_current[2]	6h	R/W	Define the current on pin LED_OUT1/2 in flash mode if ext_torch_on=01 and TXMASK/TORCH=1	
				0h	0mA
				1h	57mA (62.7mA if current_boost=1)
				2h	113mA (125.5mA if current_boost=1)
				3h	169mA (188.2mA if current_boost=1)
				4h	226mA (251mA if current_boost=1)
				5h	282mA (313.7mA if current_boost=1)
				6h	339mA (376.5mA if current_boost=1)- default
				7h	395mA (439.2mA if current_boost=1)
				8h	452mA (502mA if current_boost=1)
				9h	508mA (564.7mA if current_boost=1)
				Ah	565mA (627.5mA if current_boost=1)
				Bh	621mA (690.2mA if current_boost=1)
				Ch	678mA (752.9mA if current_boost=1)
				Dh	734mA (815.7mA if current_boost=1)
				Eh	791mA (878.4mA if current_boost=1)
				Fh	847mA (941.2mA if current_boost=1)

1. The MSB bit of this register not used to protect the LED; therefore the maximum current = half the maximum flash current
2. If current_boost=1, the LED current is increased by 11%.

Table 10. Low Voltage Register

Addr: 4		Low Voltage Register This register defines the operating mode with low battery voltages			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
2:0	vin_low_v_run	4h	R/W	Voltage level on VIN where current reduction triggers during operation (see Current Reduction by VIN measurements in Flash Mode on page 14) - only in flash mode; if VIN drops below this voltage during current ramp up, the current ramp up is stopped; during operation the current is decreased until the voltage on VIN rises above this threshold - fault_uvlo is set	
				0h	function is disabled
				1h	3.0V
				2h	3.07V
				3h	3.14V
				4h	3.22V - default
				5h	3.3V
				6h	3.38V
				7h	3.47V
5:3	vin_low_v	5h	R/W	Voltage level on VIN where driver will change current before startup (only in flash mode) if before startup (out_on set from 0 to 1), the voltage on VIN is below vin_low_v, the current is changed to flash_txmask_current (vin_low_v_shutdown=0) or 0=shutdown (vin_low_v_shutdown=1) and fault_uvlo is set	
				0h	function is disabled
				1h	3.0V
				2h	3.07V
				3h	3.14V
				4h	3.22V
				5h	3.3V - default
				6h	3.38V
				7h	3.47V
6	vin_low_v_shutdown	0	R/W	Enables Shutdown of current reduction under low voltage conditions	
				0	if before startup (out_on set from 0 to 1), the voltage on VIN is below vin_low_v, the current is changed to flash_txmask_current and fault_uvlo is set
				1	if before startup (out_on set from 0 to 1), the voltage on VIN is below vin_low_v, the operating mode stays in shutdown (zero LED current) and fault_uvlo is set
7	const_v_mode	0	R/W	Enables Constant output voltage mode	
				0	Normal operation defined by mode_setting
				1	5V constant voltage mode on VOUT1/2; reset registers mode_setting, out_on and ext_torch_on before setting this bit

Table 11. Flash Timer Register

Addr: 5		Flash Timer Register This register identifies the flash timer and timeout settings			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7:0	flash_timeout[1]	23h	R/W	Define the duration of the flash timer and timeout timer	
				0h	2ms
				1h	4ms
				2h	6ms
				...	...
				23h	72ms - default
				...	...
				7F	256ms
				80	264ms(now 8 ms LSB steps from here on)[2]
				81	272ms
				82	280ms
				...	...
				FEh	1272ms
				FFh	1280ms

1. At maximum output current the flash duration should be limited to 120ms (depending of VF of the LED, thermal design and ambient temperature) to avoid overheating of the AS3648.
2. Internal calculation for codes above 80h: flash timeout [ms] = (flash_timeout-127) * 8 + 256 [ms]

Table 12. Control Register

Addr: 6		Control Register This register identifies the operating mode and includes an all on/off bit			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
1:0	mode_setting	00	R/W	Define the AS3648 operating mode	
				00	shutdown or external torch mode if ext_torch_on (page 23)=10
				01	indicator mode (or low current mode using PWM) LED current is defined by the 6LSB bits of led_current1 and led_current2 pwm modulated with 31.25kHz defined by register inct_pwm (1/16...4/16)
				10	assist light mode: LED current is defined by the 7LSB[1] bits of led_current1 and led_current2
				11	flash mode: LED current is defined by led_current1 and led_current2 (out_on and mode_setting are automatically cleared after a flash pulse)
2	reserved	X	R	reserved - don't use, always write 0	

Table 12. Control Register (Continued)

Addr: 6		Control Register This register identifies the operating mode and includes an all on/off bit			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
3	out_on	0	R/W	Enables the output current sinks (pin LED_OUT1/2)	
				0	outputs disabled
				1	outputs enabled (out_on and mode_setting are automatically cleared after a flash pulse)

1. The MSB bit of this register not used to protect the LED; therefore the maximum assist light current = half the maximum flash current

Table 13. Strobe Signalling Register

Addr: 7		Strobe Signalling Register This register defines the flash current reducing and mode for STROBE			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
6	strobe_type	1	R/W	Defines if the STROBE input is edge or level sensitive; see also bit strobe_on (page 27)	
				0	STROBE input is edge sensitive
				1	STROBE input is level sensitive
7	strobe_on	1	R/W	Enables the STROBE input	
				0	STROBE input disabled
				1	STROBE input enabled in flash mode

Table 14. Fault Register

Addr: 8		Fault Register This register identifies all the different fault conditions and provide information about the LED detection			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	fault_uvlo	0	R/sC[1]	an undervoltage event has happened - see Current Reduction by VIN measurements in Flash Mode on page 14	
				0	No
				1	Yes
1	reserved	0	R	reserved - don't use	
2	reserved	0	R	reserved - don't use	
3	fault_txmask	0	R/sC[1]	TXMASK/TORCH event triggered during flash - see TXMASK event occurred on page 12	
				0	No
				1	Yes
4	fault_timeout	0	R/sC[1]	see Flash Timeout on page 12	
				0	No fault
				1	Flash timeout exceeded

Table 14. Fault Register (Continued)

Addr: 8		**Fault Register** — This register identifies all the different fault conditions and provide information about the LED detection			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
5	fault_overtemp	0	R/sC[1]	see Overtemperature Protection on page 12	
				0	No fault
				1	Junction temperature limit has been exceeded
6	fault_led_short	0	R/sC[1]	see Short Circuit Protection on page 12	
				0	No fault
				1	A shorted LED is detected (pin LED_OUT1/2)
7	fault_ovp	0	R/sC[1]	see Overvoltage Protection on page 11	
				0	No fault
				1	An overvoltage condition is detected (pin VOUT)

1. R/sC = Read, self clear; after readout the register is automatically cleared

Table 15. PWM and Indicator Register

Addr: 9		**PWM and Indicator Register** — This register defines the PWM mode (e.g. for indicator) and 4/1MHz mode switching			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
1:0	inct_pwm	00	R/W	Define the AS3648 PWM with 31.25kHz operation for indicator or low current mode (mode_setting=01)	
				00	1/16 duty cycle
				01	2/16 duty cycle
				10	3/16 duty cycle
				11	4/16 duty cycle
2	freq_switch_on	0	R/W	Exact frequency switching between 4MHz/1MHz for assist and flash modes for operation close to maximum pulsewidth	
				0	Pulseskip operation is allowed for all modes - results in better efficiency
				1	In flash and assist light mode (indicator mode or low current mode using PWM always will use pulseskip) if led_current1>=40h and led_current2>=40h and current_boost=0 , the DCDC is running at 4MHz or 1MHz (pulseskip is disabled) - results in improved noise performance;
3	led_out1above2	0	R	Measure the voltage difference between LED_OUT1 vs.LED_OUT2 during operation of the DCDC	
				0	
				1	V(LED_OUT1) > V(LED_OUT2) + $V_{LED\_OUTCOMP\_HYST}$

Table 15. PWM and Indicator Register (Continued)

Addr: 9				PWM and Indicator Register	
				This register defines the PWM mode (e.g. for indicator) and 4/1MHz mode switching	
Bit	**Bit Name**	**Default**	**Access**	**Description**	
4	led_out2above1	0	R	Measure the voltage difference between LED_OUT1 vs.LED_OUT2 during operation of the DCDC	
				0	
				1	V(LED_OUT2) > V(LED_OUT1) + $V_{LED\_OUTCOMP\_HYST}$
5	load_balance_on	0	R/W	Balance the current sinks (up to +/-10% of set current) to improve application efficiency for unmatched LED forward voltages - see Load Balancing on page 17	
				0	disabled
				1	enabled

Table 17. Minimum LED Current Register

Addr: Eh				Minimum LED Current Register
				This register reports the minimum LED current from the last operation cycle
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	led_current_min[1,2,3]	00h	R	Minimum current through the current sink (only including all current reductions as described in Current Reduction by VIN measurements in Flash Mode excluding current reductions caused by TXMASK)

1. Only the current through LED_OUT1 is reported.
2. As the internal change of this register is asynchronous to the readout, it is recommended to readout the register after the flash pulse. The register will store the minimum current through the LED after e.g. a previous flash. This current can be used for a subsequent flash pulse for a safe operating range.
3. This register is only set if an actual current reduction happens (fault_uvlo (see page 27)=1) otherwise led_current_min=0.

Table 18. Actual LED Current Register

Addr: Fh				Actual LED Current Register
				This register reports the actual set LED current
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	led_current_actual[1,2]	00h	R	Actual set current through the current sink (including all current reductions as described in Flash Current Reductions including LED current ramp up/down)

1. Only the current through LED_OUT1 is reported.
2. As the internal change of this register is asynchronous to the readout, it is recommended to readout the register twice and compare the results.

Table 19. Password Register Register

Addr: 80h		Password Register Register Password Protection for register Current Boost		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	password	NA	W	Write A1h into this register to enable access to register 81h

Table 20. Current Boost Register

Addr: 81h		Current Boost Register Increase output current by 11%			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	current_boost[1]	0	R/W	Boost all LED currents by 11%	
				0	all LED current are as described in the tables
				1	all LED current are increased by 11%

1. Write A1h into register password (0x80) to enable access to this register (password unlocking is only valid for a single I^2C access) - required on any read or write access to this register

Register Map

Table 21. Register Map [1]

Register Definition	Addr	Default	Content							
Name			**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
ChipID	0	Bxh	fixed_id					version		
Current Set LED1	1	9Ch	led_current1							
Current Set LED2	2	9Ch	led_current2							
TXMask	3	68h	flash_txmask_current				coil_peak		ext_torch_on	
Low Voltage	4	2Ch	const_v_mode	vin_low_v_shutdown	vin_low_v			vin_low_v_run		
Flash Timer	5	23h	flash_timeout							
Control	6	00h					out_on	reserved	mode_setting	
Strobe Signalling	7	C0h	strobe_on	strobe_type						
Fault	8	00h	fault_ovp	fault_led_short	fault_overtemp	fault_timeout	fault_txmask	reserved	reserved	fault_uvlo
PWM and Indicator	9	00h			load_balance_on	led_out2above1	led_out1above2	freq_switch_on	inct_pwm	
Minimum LED Current	Eh	00h	led_current_min							
Actual LED Current	Fh	00h	led_current_actual							
Password Register	80h	00h	password							
Current Boost	81h	00h								current_boost

1. Always write'0' to undefined register bits (e.g. to bits 4..7 of register 6)

9 Application Information

External Components

Input Capacitor C_{VIN}

Low ESR input capacitors reduce input switching noise and reduce the peak current drawn from the battery. Ceramic capacitors are required for input decoupling and should be located as close to the device as is practical.

Table 22. Recommended Input Capacitor

Part Number	C	TC Code	Rated Voltage	Size	Manufacturer
GRM188R60J106ME47	10µ >3µF@4.5V >2µF@5.25V	X5R	6V3	0603	Murata www.murata.com
LMK107BBJ106MA	10µ >3µF@4.5V	X5R	6V3	0603	Taiyo Yuden www.t-yuden.com

If a different input capacitor is chosen, ensure similar ESR value and at least 3µF capacitance at the maximum input supply voltage. Larger capacitor values (C) may be used without limitations.

Add a smaller capacitor in parallel to the input pin VIN (e.g. Murata GRM155R61C104, >50nF @ 3V, 0402 size).

Output Capacitor C_{VOUT}

Low ESR capacitors should be used to minimize VOUT ripple. Multi-layer ceramic capacitors are recommended since they have extremely low ESR and are available in small footprints. The capacitor should be located as close to the device as is practical.

X5R dielectric material is recommended due to their ability to maintain capacitance over wide voltage and temperature range.

Table 23. Recommended Output Capacitor

Part Number	C	TC Code	Rated Voltage	Size	Manufacturer
GRM219R61A116U	10µF +/-10% >4.2µF@5V	X5R	10V	0805	Murata www.murata.com
GRM188R60J106ME84[1]	10µF +/-20% >4.2µF@4V	X5R	6.3V	0603 (1.6x0.8x0.85mm max. 0.95mm height)	

1. Use only for VLED < 3.75V

If a different output capacitor is chosen, ensure similar ESR values and at least 4.2µF capacitance at 5V output voltage.

Inductor L_{DCDC}

The fast switching frequency (4MHz) of the AS3648 allows for the use of small SMDs for the external inductor. The saturation current $I_{SATURATION}$ should be chosen to be above the maximum value of I_{LIMIT}[13]. The inductor should have very low DC resistance (DCR) to reduce the I^2R power losses - high DCR values will reduce efficiency.

Table 24. Recommended Inductor

Part Number	L	DCR	$I_{SATURATION}$	Size	Manufacturer
C3-P1.5R	1.5µH	58mΩ	2.4A@25ºC, 2.0A[1]	3x3x1.5mm (height is max.)	Mitsumi www.mitsumi.com
LQM32PN1R0MG0	1.0µH >0.6µH @ 3.0A	60mΩ	3.0A[2]	3.2x2.5x0.9 mm max 1.0mm height	Murata www.murata.com
LQM2HPN1R0MGC	1.0µH >0.6µH @ 2.0A	100mΩ	1.5A (2.0A)[3]	2.5x2.0x0.9 mm max 1.00mm height	
CIG32W1R0MNE	1.0µH >0.7µH @ 2.7A >0.6µH @ 3.0A	60mΩ +/-25%	3.0A	3.2x2.5mm max 1.0mm height	Samsung Electro-Mechancs www.sem.samsung.co.kr
NRH2412T1R0N	1.0µH >0.6µH @ 2.5A	77mΩ	2.5A[4]	2.4x2.4x1.2 mm (height is max.)	Taiyo Yuden www.t-yuden.com
CKP3225N1R0M	1.0µH >0.6µH @ 3.0A	<60mΩ	3.0A	3.2x2.5x0.9 mm max 1.0mm height	
MAMK2520T1R0M	1.0µH >0.6µH @ 2.75A	45mΩ	3.0A[5]	2.5x2.0x1.2 mm height is max	
MDMK2020T1R0M	1.0µH >0.6µH @ 2.75A	56mΩ	2.55A[6]	2.0x2.0x1.2 mm height is max	
MAKK2016T1R0M	1.0µH >0.6µH @ 2.75A	65mΩ	2.0A[7]	2.0x1.6x1.0 mm height is max	

1. Do not exceed maximum $I_{SATURATION}$ - can be ensured by setting coil_peak (will limit LED current)
2. Flash pattern: 200ms/3A, 200ms pause, 200ms/3A, 2s then repeat again (no limit on the number of total cycles) Alternative pattern with 1000ms/1.6A, 200ms pause, 200ms/3A, 200ms pause, 200ms/3A, 2s then repeat again. (no limit on the number of total cycles)
3. Set current limit to 2A (coil_peak=00b) - will limit maximum output current. Flash cycle limit: 150ms on, 500ms off; repeat maximum 50 times.
4. Set current limit to 2.5A (coil_peak=01b) - will limit maximum output current.
5. Set current limit to 3.0A (coil_peak=10b) - can limit maximum output current.
6. Set current limit to 2.5A (coil_peak=01b) - will limit maximum output current.
7. Set current limit to 2A (coil_peak=00b) - will limit maximum output current.

If a different inductor is chosen, ensure similar DCR values and at least0.6µH inductance at I_{LIMIT}.

13.Can be adjusted in I^2C mode with register coil_peak (see page 23)

PCB Layout Guideline

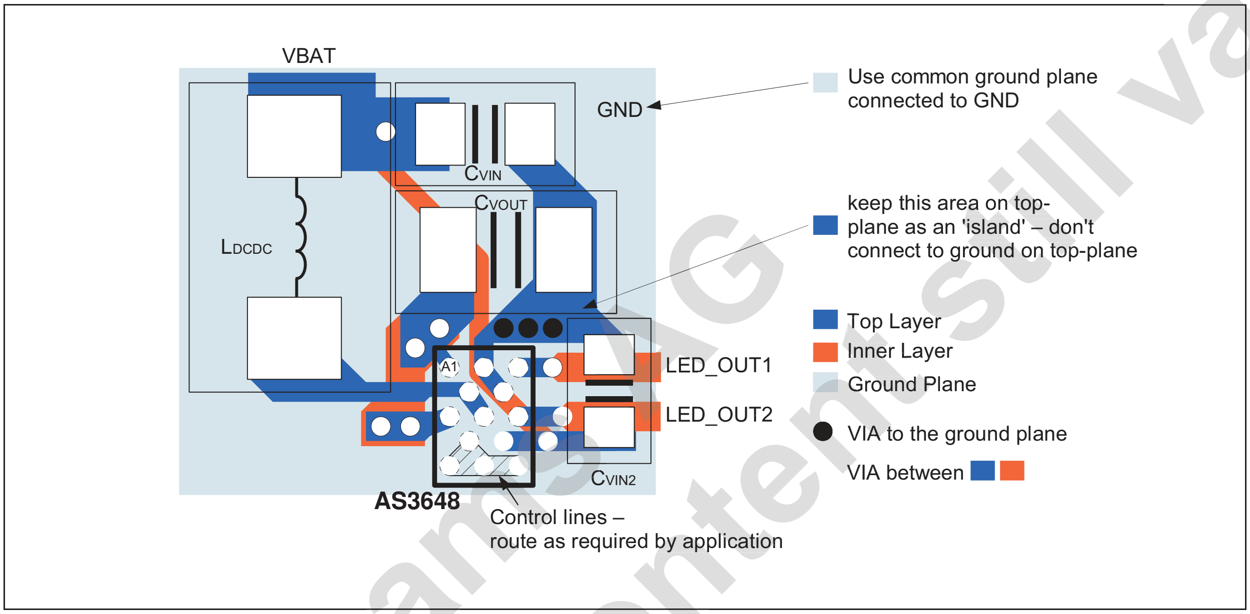
The high speed operation requires proper layout for optimum performance. Route the power traces first and try to minimize the area and wire length of the two high frequency/high current loops:

Loop1: CVIN/CVIN2 - LDCDC - pin SW1/2 - pin GND - CVIN/CVIN2

Loop2: CVIN/CVIN2 - LDCDC - pin SW1/2 - pin VOUT1/2 - CVOUT - pin GND - CVIN/CVIN2

At the pin GND a single via (or more vias, which are closely combined) connects to the common ground plane. This via(s) will isolate the DCDC high frequency currents from the common ground (as most high frequency current will flow between Loop1 and Loop2 and will not pass the ground plane) - see the 'island' in Figure 32.

Figure 32. Layout recommendation



Note: If component placement rules allow, move all components close to the AS3648 to reduce the area and length of Loop1 and Loop2.

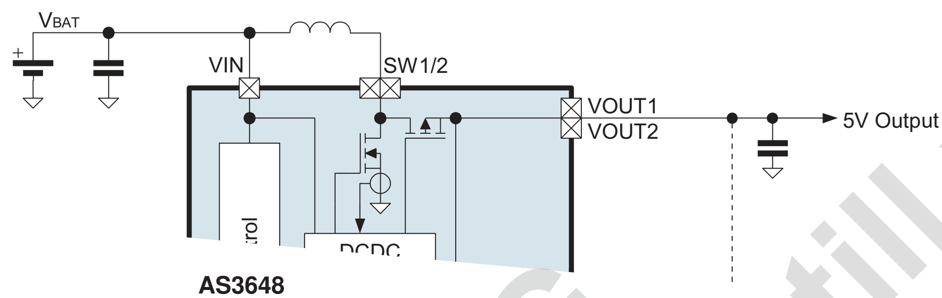
An additional 100nF (e.g. Murata GRM155R61C104, >50nF @ 3V, 0402 size) capacitor CVIN2 in parallel to CVIN is recommended to filter high frequency noise for the power supply of AS3648. This capacitor should be as close as possible to the GND/VIN pins of AS3648.

5V Operating Mode

The AS3648can be used to power a 5V system (e.g. audio amplifier). The operating mode is selected by setting register bit const_v_mode (page 25)=1. In this operating mode, the current sinks are disabled and cannot be switched on (no flash/torch operation is possible).

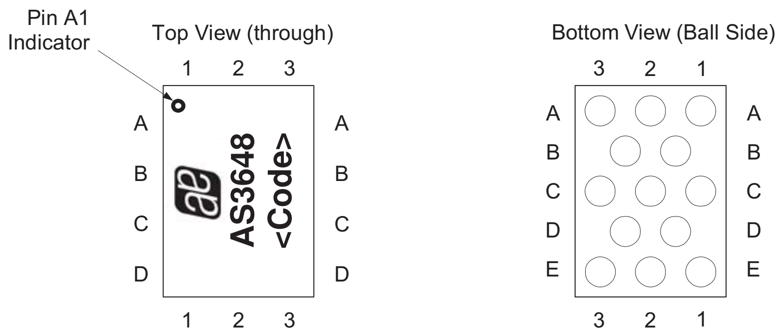
Note: There is always a diode between VIN and VOUT1/2 due to the internal circuit. Therefore VOUT1/2 cannot be completely switched off

Figure 33. 5V Operating Mode



10 Package Drawings and Markings

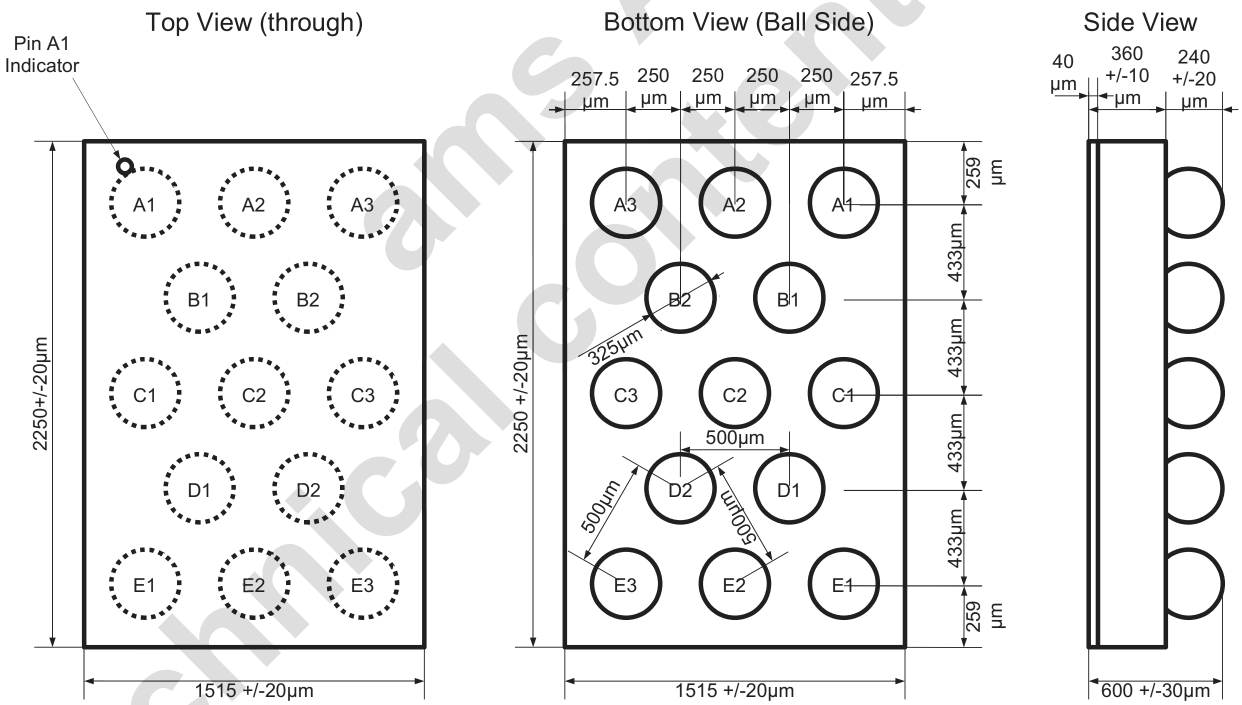
Figure 34. WL-CSP13 Marking



Note:

Line 1: austriamicrosystems logo
Line 2: AS3648
Line 3: <Code>
Encoded Datecode (4 characters)

Figure 35. WL-CSP13 Package Dimensions



The coplanarity of the balls is 40µm.

11 Ordering Information

The devices are available as the standard products shown in Table 25.

Table 25. Ordering Information

Model	Description	Delivery Form	Package
AS3648-ZWLT	2000mA High Current LED Flash Driver	Tape & Reel	13-pin WL-CSP (2.25x1.5x0.6mm) 0.5mm pitch RoHS compliant / Pb-Free / Green

Note: All products are RoHS compliant and austriamicrosystems green.
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For further information and requests, please contact us mailto:sales@austriamicrosystems.com
or find your local distributor at http://www.austriamicrosystems.com/distributor

Note: AS3648-ZWLT

AS3648-
Z Temperature Range: -30ºC - 85ºC
WL Package: Wafer Level Chip Scale Package (WL-CSP) 2.25x1.5x0.6mm
T Delivery Form: Tape & Reel

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