RE41

13.56 MHz Multi-standard RFID Reader IC

REV 0.1

Features Summary

Highlight Features

Supported Protocols

- ISO14443A/B, all bit rates
  - 106, 212, 424, 848 kbps
- ISO15693, all modes
  - Downlink: 1 of 4, 1 of 256
  - Uplink: 6.6,13,26,53 kbps with 1 & 2 subcarrier
- JIS-X-6319-4
  - 212 and 424 kbps
- NFC tag type 1,2,3,4A,4B,5
- Compatible to Crypto_M

Transmitter

- Proximity operation distance up to 10 cm (based in 3 x 4 cm^2 antenna)
- Modulation index adjustable by software
- Maximum driving current up to
  - 300mA @ 5V TVDD
  - 400mA @ 7V TVDD
- Accept external baseband signal for RF modulation
- Accept wide transmitter driver voltage from 2.7 – 7 V
- On-chip framing coder

Receiver

- Rx Sensitivity down to 1 mVpp
- Rx automatic gain control (AGC)
- EMD suppression
- Enhanced BPSK decoder with pattern recognition
- RxMultiple
- ISO14443A / ISO15693 SOF searching
- On-chip framing handler for supported protocols

Interface and peripheral

- Host interface: SPI (up to 10 Mbps)
- 64-byte send and receive FIFO buffer
- 64-byte addressing user-configurable registers
- 256-byte EEPROM
- Interrupt (IRQ) pin
- Programmable timer
- Low jitter on-chip oscillator buffer
- On-chip dual 80mA 3.3V regulators

Operating conditions

- Operating temperature: -40 °C to 85 °C
- Operating voltage: 2.7 -3.3 V
- Transmitter Voltage: 2.7 – 7V
- 6.0uA in power down mode
- 1.3mA in standby mode
- 8.0mA when all receiver blocks are active
- Package
  - QFN 5x5 32-pin with heat sink pad
  - TSSOP 28-pin

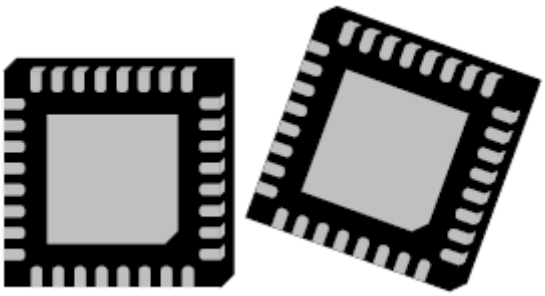
Applications

- Secure Access Control
- PC peripheral device
- Handheld RFID reader
- Midrange RFID reader
- Toy and games

Ordering information

Part No.	Description	Package	Marking	Operating Temp.
P002HRE41MQFN5-01	RE41, 13.56MHz RFID Reader IC, QFN 5x5 Package, ISO15693/14443AB Protocol support, IC	32-PIN QFN 5x5 mm	8IAYM	-40 °C to 85 °C
P002HRE41TSSOP28-01	RE41, 13.56MHz RFID Reader IC, TSSOP 28L Package, ISO15693/14443AB Protocol support, IC	28-pin TSSOP	6FAYM	-40 °C to 85 °C

General description



32-Pin QFN5x5 Package

The RE41 HiRead-R is a single-chip long-range reader ASIC for all popular 13.56-MHz RFID/contactless standard protocols. The HiRead-R supports and compatibles with all major global secured baseband ISO standards including ISO14443 Type A, Type B, Crypto_M cards, JIS-X-6391-4, and Smartlabel ISO15693. The HiRead-R provides a hi-speed SPI controller/host interface with a built-in 64-byte FIFO for smooth data transfer. Furthermore, the embedded codec is capable of handling all bit-level coding/encoding, encrypting/decrypting as well as frame-level manipulation for transmission and reception. The chip is well suited for mobile devices due to its low power consumption and low operating voltage from 2.7-3.3 V. The dual on-chip 3.3V regulators are provided to stabilize the chip's power, and simultaneously supply the power to the external companion microcontroller up to 80 mA.

The HiRead-R receiver circuit incorporates a full AGC loop allowing a wide dynamic range of RF input signal levels. The chip's excellent sensitivity performance enables detection of the input signals with amplitudes as low as 1mVpkpk without distorting the data integrity. The receiver filters can be selected optionally either to a predefined band in accordance with the generic required standard setup, or to an arbitrarily defined combination which gives flexibility to cope with various antenna variations/parameters. The baseband circuits permit the inbound/outbound configuration to accept various forms of customized protocols, incoming to the chip and outgoing to the external RF circuitry in the application specific-design system. The HiRead-R transmitter is capable of accepting a wide range of operating supply voltages to serve various applications, e.g., 5V for base stations or desktop readers, and 3.3V for handheld devices. The transmission controller is entirely used to support all operation status and requests, including FIFO status full/high/low and Transmission/Reception complete.

The transmitter drivers support a wide range of power supply voltages from 2.7 to 7 V. A high drive current up to 300 mA is guaranteed for demanding item-level mid-range reader designs. The dual high-powered transmitters can be flexibly configured in various configurations, e.g. differential driving, single-ended driving, and a mode to drive an external Class-E amplifier for improving the drive strength in the gate antenna setup.

To facilitate operation of the companion microcontroller, the HiRead-R is fully equipped with on-chip peripheral support devices such as an RF-trig timer: a host interrupt generator, and a clock divider. The chip's embedded 256-byte EPPROM stores predefined re-loadable register values for easy reader setup, and the crypto key for encryption mode. The RE41 is offered in a low-profile QFN package with excellent heat dissipation when self-mounted on PCB.

1. Block diagram and typical configuration

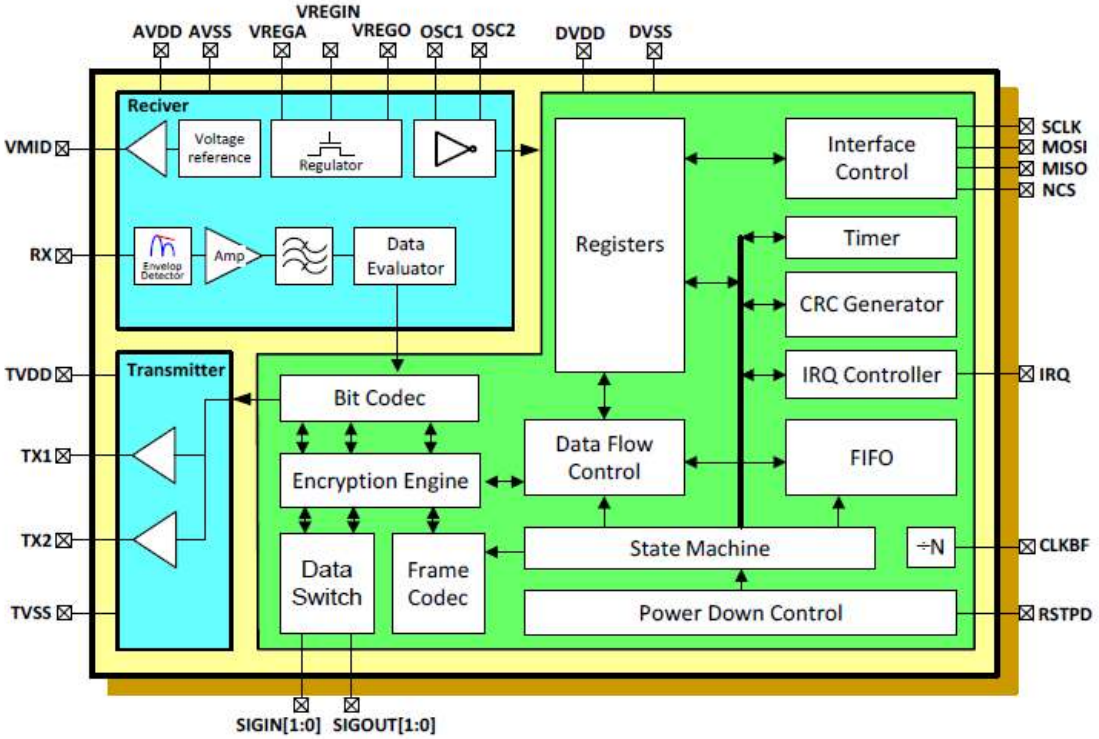


Figure 1 Functional Block Diagram

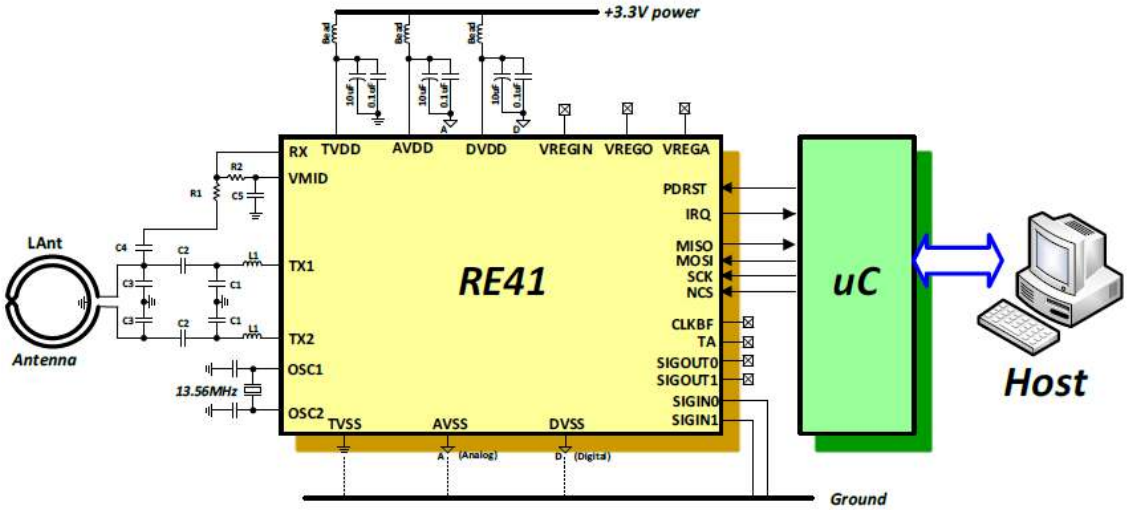


Figure 2 Typical operating circuit

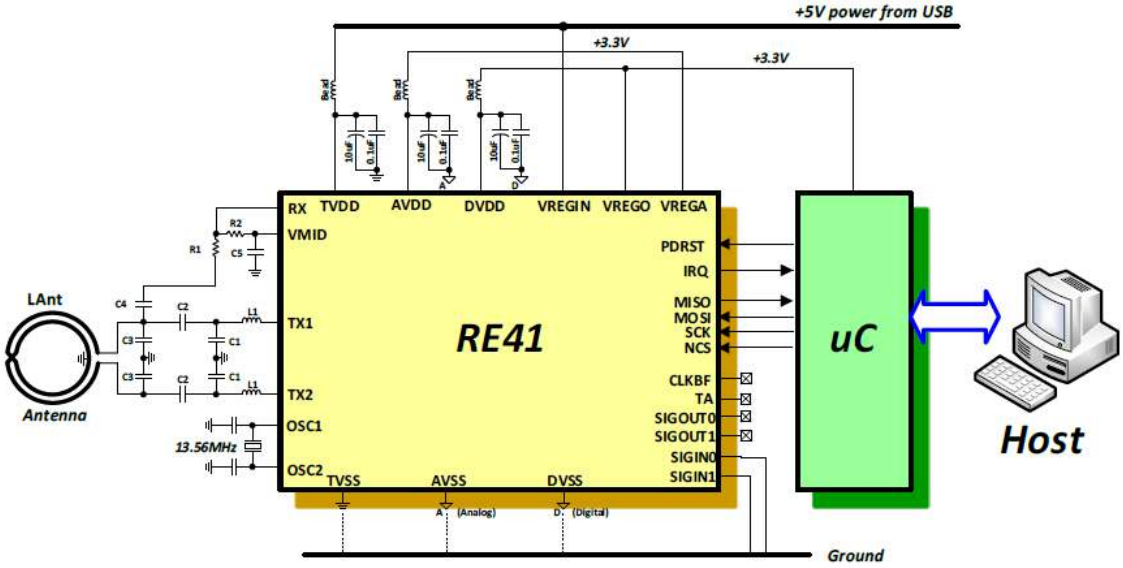


Figure 3 Typical configuration employing on-chip regulators

2. Pin configuration

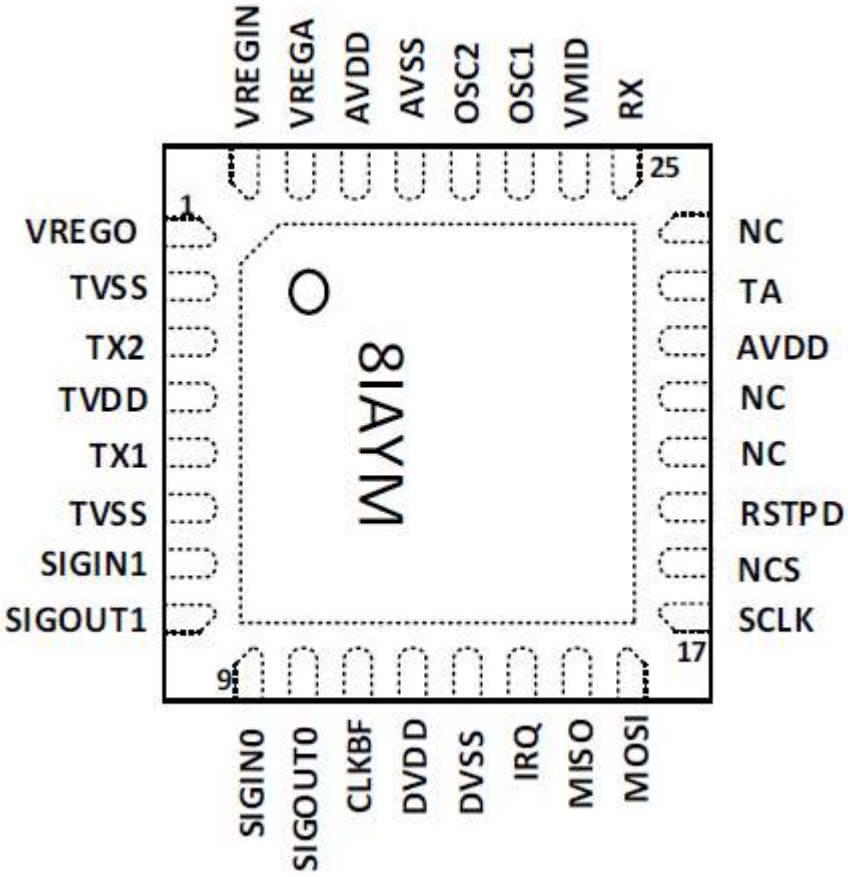


Figure 4 QFN pin Arrangement (Top view)

Y: Year Code
M: Month Code

Table 1 Pin description

Pin	Symbol	Type	Related Supply	Description
1	VREGO	Power	DVDD, DVSS	3.3V Regulator Output for Digital part
2	TVSS	Power	TVDD, TVSS	Transmitter Ground
3	TX2	OUT	TVDD, TVSS	Transmitter Output 2
4	TVDD	Power	TVDD, TVSS	Transmitter VDD
5	TX1	OUT	TVDD, TVSS	Transmitter Output 1
6	TVSS	Power	TVDD, TVSS	Transmitter Ground
7	SIGIN1	IN	DVDD, DVSS	Digital input signal for test mode. If this Pin is unused, tide gnd.
8	SIGOUT1	OUT	DVDD, DVSS	Digital output signal for test mode
9	SININ0	IN	DVDD, DVSS	Digital input signal for test mode. If this Pin is unused, tide gnd.
10	SINOUT0	OUT	DVDD, DVSS	Digital output signal for test mode
11	CLKBF	OUT	DVDD, DVSS	Buffered clock 13.56/6.78/3.39 MHz Output for external MCU
12	DVDD	Power	DVDD, DVSS	Digital and I/O VDD
13	DVSS	Power	DVDD, DVSS	Digital and I/O Ground
14	IRQ	OUT	DVDD, DVSS	Interrupt Request
15	MISO	OUT	DVDD, DVSS	SPI Master-In-Slave-Out
16	MOSI	IN	DVDD, DVSS	SPI Master-Out-Slave-In
17	SCLK	IN	DVDD, DVSS	SPI Clock Input
18	NCS	IN	DVDD, DVSS	SPI Chip Select (Active low)
19	RSTPD	IN	DVDD, DVSS	Reset and Power Down (Active High)
20	NC	-	-	Not Connected
21	NC	-	-	Not Connected
22	AVDD	PWR	AVDD, AVSS	Analog VDD (Optional)
23	TA	OUT	AVDD, AVSS	Analog Test Pin
24	NC	-	-	Not Connected
25	RX	IN	AVDD, AVSS	Receiver Input
26	VMID	IN	AVDD, AVSS	Mid Rail Reference Voltage
27	OSC1	IN	AVDD, AVSS	Xtal Oscillator input
28	OSC2	OUT	AVDD, AVSS	Xtal Oscillator Output
29	AVSS	Power	AVDD, AVSS	Analog Ground
30	AVDD	Power	AVDD, AVSS	Analog VDD
31	VREGA	Power	AVSS	3.3V Regulator Output for Analog part
32	VREGIN	Power	AVDD, AVSS	Regulator input

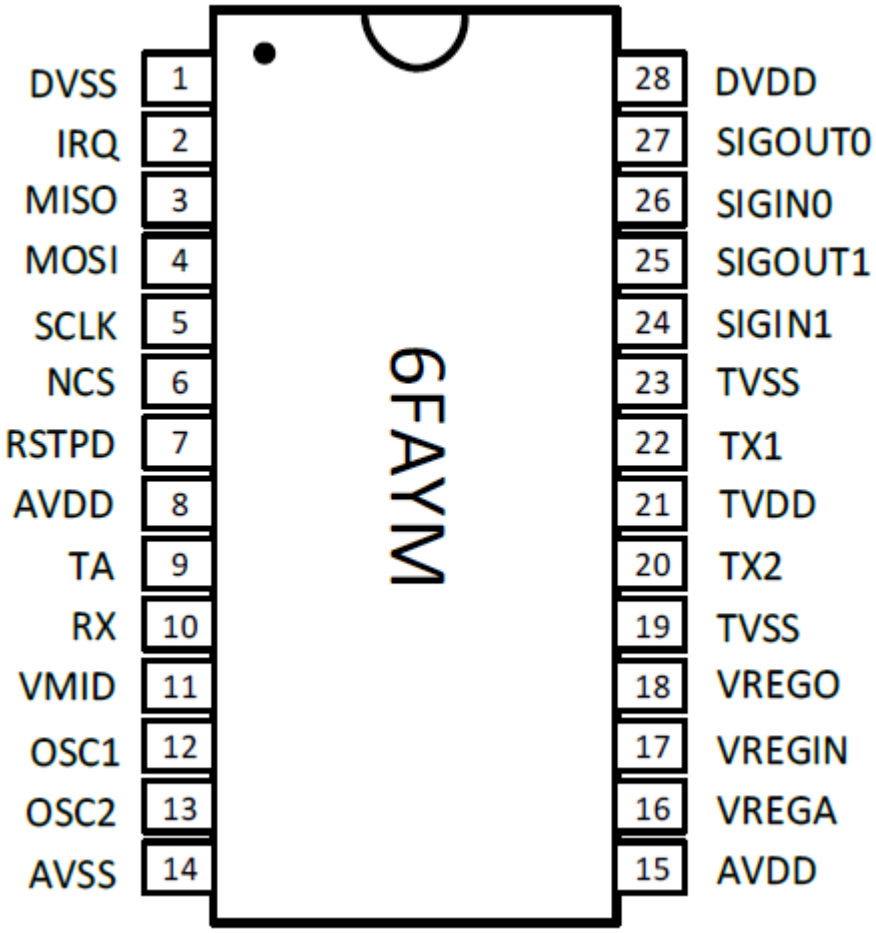


Figure 5 TSSOP pin arrangement (Top view)

Y: Year Code
M: Month Code

Table 2 TSSOP pin description

Pin	Symbol	Type	Related Supply	Description
1	DVSS	Power	DVDD, DVSS	Digital and I/O Ground
2	IRQ	OUT	DVDD, DVSS	Interrupt Request
3	MISO	OUT	DVDD, DVSS	SPI Master-In-Slave-Out
4	MOSI	IN	DVDD, DVSS	SPI Master-Out-Slave-In
5	SCLK	IN	DVDD, DVSS	SPI Clock Input
6	NCS	IN	DVDD, DVSS	SPI Chip Select (Active low)
7	RSTPD	IN	DVDD, DVSS	Reset and Power Down (Active High)
8	AVDD	PWR	AVDD, AVSS	Analog VDD (Optional)
9	TA	OUT	AVDD, AVSS	Analog Test Pin
10	RX	IN	AVDD, AVSS	Receiver Input
11	VMID	IN	AVDD, AVSS	Mid Rail Reference Voltage
12	OSC1	IN	AVDD, AVSS	Xtal Oscillator input
13	OSC2	OUT	AVDD, AVSS	Xtal Oscillator Output
14	AVSS	Power	AVDD, AVSS	Analog Ground
15	AVDD	Power	AVDD, AVSS	Analog VDD
16	VREGA	Power	AVSS	3.3V Regulator Output for Analog part
17	VREGIN	Power	AVDD, AVSS	Regulator input
18	VREGO	Power	DVDD, DVSS	3.3V Regulator Output for Digital part
19	TVSS	Power	TVDD, TVSS	Transmitter Ground
20	TX2	OUT	TVDD, TVSS	Transmitter Output 2
21	TVDD	Power	TVDD, TVSS	Transmitter VDD
22	TX1	OUT	TVDD, TVSS	Transmitter Output 1
23	TVSS	Power	TVDD, TVSS	Transmitter Ground
24	SIGIN1	IN	DVDD, DVSS	Digital input signal for test mode. If this Pin is unused, tide gnd.
25	SIGOUT1	OUT	DVDD, DVSS	Digital output signal for test mode
26	SIGIN0	IN	DVDD, DVSS	Digital input signal for test mode. If this Pin is unused, tide gnd.
27	SIGOUT0	OUT	DVDD, DVSS	Digital output signal for test mode
28	DVDD	Power	DVDD, DVSS	Digital and I/O VDD

3. Electrical specification

Table 3 Operating Condition

Parameter	Description	Min	Typ	Max	Unit	Rating
AVDD	Analog Power Supply Voltage	2.7	3.3	3.6	V	
DVDD	Digital Power Supply Voltage	2.7	3.3	3.6	V	
TVDD	Transmitter Power Supply Voltage	2.7	5.0	7.0	V	
ESD	Electrostatic discharge tolerance	2.0			kV	HBM model
VPOR	Reset Trigger voltage		2.4		V	

Table 4 Power Consumption

Parameter	Description	Min	Typ	Max	Unit	Conditions
IAVDD	Analog Power Supply Current		5.5		mA	All blocks active
			1.4		mA	Idle (Receiver Off)
			1.3		mA	Standby
			6.0	11.0	uA	Soft Power down
			0.5	1.0	uA	Hard Power down, (**RSTPD** = 1)
IDVDD	Digital Power Supply Current		2.5		mA	**CLKBF** is not enabled
			3.0		mA	**CLKBF** is enabled
			64		uA	Standby
			0.5	1	uA	Soft/Hard Power down

Table 5 Transmitter characteristic

Parameter	Description	Min	Typ	Max	Unit	Conditions
ITX1	Logic 1 Transmitter Source Current	300	340		mA	TVDD = 5V, 85℃
		380	440		mA	TVDD = 7V, 85℃
ITX0	Logic 0 Transmitter Sink Current	270	300		mA	TVDD = 5V, 85℃
		360	400		mA	TVDD = 7V, 85℃
ZTX	Tx Output impedance (**GsCfgCW** =0x3F)		3.5	5	Ohm	TVDD = 5V, 85℃
			2.5	4	Ohm	TVDD = 7V, 85℃
ITVDD	Transmitter Static Power supply Current		7		mA	**TX1**&**TX2** are Unconnected **RF1En** = 1, **RF2En** = 1 TVDD = 5 V
M	Adjustable Modulation index			60	%	TVDD = 5V, **100ASK** = 0
				100	%	TVDD = 5V, **100ASK** = 1

Table 6 Receiver characteristic

Parameter	Description	Min	Typ	Max	Unit	Conditions
VSEN	Receiver input sensitivity		1		mVpkpk	AVDD = 3.3V
PSRR	Power supply rejection ratio		40		dB	AVDD = 3.3V + 0.2*sin(1MHz)
VRx	Rx input voltage range	0.0		3.3	V	AVDD = 3.3 V, **BypassENV** = 0
		0.5		2.8	V	AVDD = 3.3 V, **BypassENV** = 1
VCarMin	Minimum Carrier for envelope detector		0.3		Vpkpk	
VVMID	VMID Voltage		1.65		V	**VMidsel** = 0, AVDD = 3.3 V
			1.24		V	**VMidsel** = 1, AVDD = 3.3 V
ZVMID	VMID output impedance @ 13.56 MHz		6		Ohm	CLoad(1) = 100nF, TVDD = 5 V
Gain	Gain (Measured from Rx to the output of the internal last amplifier)			48	dB	**Gain** = 11b, **Gain_ST3** = 000b
		12			dB	**Gain** = 00b, **Gain_ST3** = 000b
Gstep	Gain step		3		dB	**AGCEN** = 1
			12		dB	**AGCEN** = 0 Defined by **Gain[1:0]**
RxNoise	Intrinsic input referred noise in Rx		TBD		mVrms	

(1) CLoad: Load capacitance at `VMID` pin

Table 7 On-chip regulator

Parameter	Description	Min	Typ	Max	Unit	Conditions
VREGIN	Regulator input voltage	4.5	5	7	V	
VREGOUT	Regulator output voltage	3.10	3.25	3.40	V	IREGOUT = 0 mA
IREGIN	Input regulator current			160	mA	
IREGOUT	Output regulator current			80	mA	
$\Delta Vout_{LineReg}$	Line regulation (ΔVout)		0.5	1.0	mV/V	IREGOUT = 0 mA, 4.5V < **VREGIN** < 7V
$\Delta Vout_{LoadReg}$	Load regulation (ΔVout)		0.25		mV/mA	**VREGIN** = 5 V, 0 < IREGOUT < 80 mA
VREGDrop	Drop Out Voltage			40	mV	IREGOUT = 80 mA
IREGBias	Regulator Bias Current	170	200	220	uA	5 V < **VREGIN** < 7 V