TwinDie™ DDR3L SDRAM

MT41K1G4 – 64 Meg x 4 x 8 Banks x 2 Ranks

MT41K512M8 – 32 Meg x 8 x 8 Banks x 2 Ranks

Features

- Uses 2Gb Micron die
- Two ranks (includes dual CS#, ODT, CKE, and ZQ balls)
- Each rank has eight internal banks for concurrent operation
- $V_{DD} = V_{DDQ}$ = +1.35V (1.283V to 1.45V), backward compatible to $V_{DD} = V_{DDQ}$ = +1.5V ±0.075V
- 1.35V center-terminated push/pull I/O
- JEDEC-standard ball-out
- Low-profile package
- T_C of 0°C to 95°C
  - 0°C to 85°C: 8192 refresh cycles in 64ms
  - 85°C to 95°C: 8192 refresh cycles in 32ms

Description

The 4Gb (TwinDie™) DDR3L SDRAM (1.35V) uses Micron's 2Gb DDR3L SDRAM die (essentially two ranks of the 2Gb DDR3L SDRAM). Refer to Micron's 2Gb DDR3L SDRAM data sheet for the specifications not included in this document. Specifications for base part number MT41K512M4 correlate to TwinDie manufacturing part number MT41K1G4; specifications for base part number MT41K256M8 correlate to TwinDie manufacturing part number MT41K512M8.

Options	Marking
• Configuration	
– 64 Meg x 4 x 8 banks x 2 ranks	1G4
– 32 Meg x 8 x 8 banks x 2 ranks	512M8
• FBGA package (Pb-free)	
– 78-ball FBGA (9mm x 11.5mm x 1.2mm)	THD
– 78-ball FBGA (8mm x 11.5mm x 1.2mm)	THV
• Timing – cycle time[1]	
– 1.25ns @ CL = 11 (DDR3L-1600)	-125
– 1.5ns @ CL = 9 (DDR3L-1333)	-15E
– 1.87ns @ CL = 7 (DDR3L-1066)	-187E
• Self refresh	
– Standard	None
• Operating temperature	
– Commercial (0°C ≤ T_C ≤ 95°C)	None
• Revision	:D/:M

Note: 1. CL = CAS (READ) latency.

Table 1: Key Timing Parameters

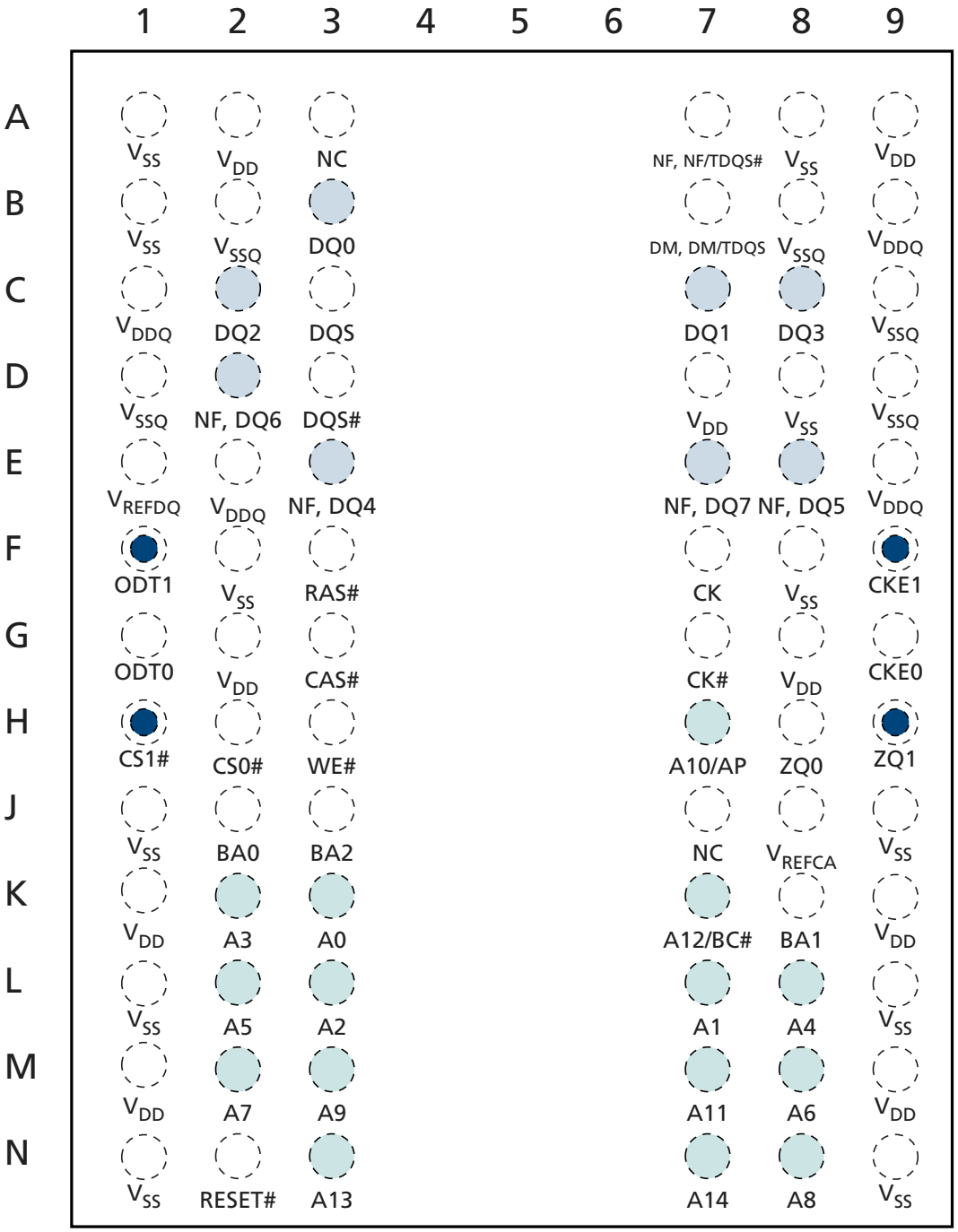
Speed Grade	Data Rate (MT/s)	Target ^{t}RCD-^{t}RP-CL	^{t}RCD (ns)	^{t}RP (ns)	^{t}CL (ns)
-125	1600	11-11-11	13.75	13.75	13.75
-15E	1333	9-9-9	13.5	13.5	13.5
-187E	1066	7-7-7	13.1	13.1	13.1

Table 2: Addressing

Parameter	1024 Meg x 4	512 Meg x 8
Configuration	64 Meg x 4 x 8 banks x 2 ranks	32 Meg x 8 x 8 banks x 2 ranks
Refresh count	8K	8K
Row address	32K A[14:0]	32K A[14:0]
Bank address	8 BA[2:0]	8 BA[2:0]
Column address	2K A[11, 9:0]	1K A[9:0]

Ball Assignments and Descriptions

Figure 1: 78-Ball FBGA Ball Assignments (Top View)



Note: 1. Dark balls (with ring) designate balls that differ from the monolithic versions.

Table 3: FBGA 78-Ball Descriptions

Symbol	Type	Description
A14, A13, A12/BC#, A11, A10/AP, A[9:0]	Input	**Address inputs:** Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. Address inputs are referenced to V_{REFCA}. A12/BC#: When enabled in the mode register (MR), A12 is sampled during READ and WRITE commands to determine whether burst chop (on-the-fly) will be performed (HIGH = burst length (BL) of 8 or no burst chop, LOW = burst chop (BC) of 4, burst chop).
BA[2:0]	Input	**Bank address inputs:** BA[2:0] define the bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command. BA[2:0] are referenced to V_{REFCA}.
CK, CK#	Input	**Clock:** CK and CK# are differential clock inputs. All command, address, and control input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data strobe (DQS, DQS#) is referenced to the crossings of CK and CK#.
CKE[1:0]	Input	**Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM. The specific circuitry that is enabled/disabled is dependent upon the DDR3L SDRAM configuration and operating mode. Taking CKE LOW provides PRECHARGE power-down and SELF REFRESH operations (all banks idle) or active power-down (row active in any bank). CKE is synchronous for power-down entry and exit and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CK, CK#, CKE, RESET#, and ODT) are disabled during power-down. Input buffers (excluding CKE and RESET#) are disabled during SELF REFRESH. CKE is referenced to V_{REFCA}.
CS#[1:0]	Input	**Chip select:** CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external rank selection on systems with multiple ranks. CS# is considered part of the command code.
DM	Input	**Input data mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with the input data, during a write access. Although the DM ball is input-only, the DM loading is designed to match that of the DQ and DQS balls. DM is referenced to V_{REFDQ}. DM has an optional use as TDQS on the x8.
ODT[1:0]	Input	**On-die termination:** ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3L SDRAM. When enabled in normal operation, ODT is only applied to each of the following balls: DQ[7:0], DQS, DQS#, and DM for the x8; DQ[3:0], DQS, DQS#, and DM for the x4. The ODT input is ignored if disabled via the LOAD MODE command. ODT is referenced to V_{REFCA}.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with CS#) define the command being entered and are referenced to V_{REFCA}.
RESET#	Input	**Reset:** RESET# is an active LOW CMOS input referenced to V_{SS}. The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH ≥ 0.8 × V_{DDQ} and DC LOW ≤ 0.2 × V_{DDQ}. RESET# assertion and desertion are asynchronous.
DQ[3:0]	I/O	**Data input/output:** Bidirectional data bus for x4 configuration. DQ[3:0] are referenced to V_{REFDQ}.

Table 3: FBGA 78-Ball Descriptions (Continued)

Symbol	Type	Description
DQ[7:0]	I/O	**Data input/output:** Bidirectional data bus for x8 configuration. DQ[7:0] are referenced to V_{REFDQ}.
DQS, DQS#	I/O	**Data strobe:** DQS and DQS# are differential data strobes: Output with read data; edge aligned with read data; input with write data; center-aligned with write data.
TDQS, TDQS#	I/O	**Termination data strobe:** Applies to the x8 configuration only. When TDQS is enabled, DM is disabled, and the TDQS and TDQS# balls provide termination resistance.
V_{DD}	Supply	**Power supply:** 1.35V (1.283V to 1.45V operational; compatible with 1.5V operation)
V_{DDQ}	Supply	**DQ power supply:** 1.35V (1.283V to 1.45V operational; compatible with 1.5V operation). Isolated on the device for improved noise immunity.
V_{REFCA}	Supply	**Reference voltage for control, command, and address:** V_{REFCA} must be maintained at all times (including self refresh) for proper device operation.
V_{REFDQ}	Supply	**Reference voltage for data:** V_{REFDQ} must be maintained at all times (including self refresh) for proper device operation.
V_{SS}	Supply	Ground.
V_{SSQ}	Supply	**DQ ground:** Isolated on the device for improved noise immunity.
ZQ[1:0]	Reference	**External reference ball for output drive calibration:** This ball is tied to an external 240Ω resistor (RZQ), which is tied to V_{SSQ}.
NC	–	**No connect:** These balls should be left unconnected (the ball has no connection to the DRAM or to other balls).
NF	–	**No function:** When configured as a x4 device, these balls are NF. When configured as a x8 device, these balls are defined as TDQS#, DQ[7:4].

Functional Description

The TwinDie DDR3L SDRAM is a high-speed, CMOS dynamic random access memory device internally configured as two 8-bank DDR3L SDRAM devices.

Although each die is tested individually within the dual-die package, some TwinDie test results may vary from a like-die tested within a monolithic die package.

The DDR3L SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is an 8*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O balls. A single read or write access consists of a single 8*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O balls.

The differential data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the DDR3L SDRAM input receiver. DQS is center-aligned with data for WRITEs. The read data is transmitted by the DDR3L SDRAM and edge-aligned to the data strobes.

Read and write accesses to the DDR3L SDRAM are burst oriented. Accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVATE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVATE command are used to select the bank and row to be accessed. The address bits (including CS*n*#, BA*n*, and A*n*) registered coincident with the READ or WRITE command are used to select the rank, bank, and starting column location for the burst access.

This data sheet provides a general description, package dimensions, and the package ballout. Refer to the Micron monolithic DDR3L data sheet for complete information regarding individual die initialization, register definition, command descriptions, and die operation.

Functional Block Diagrams

Figure 2: Functional Block Diagram (64 Meg x 4 x 8 Banks x 2 Ranks)

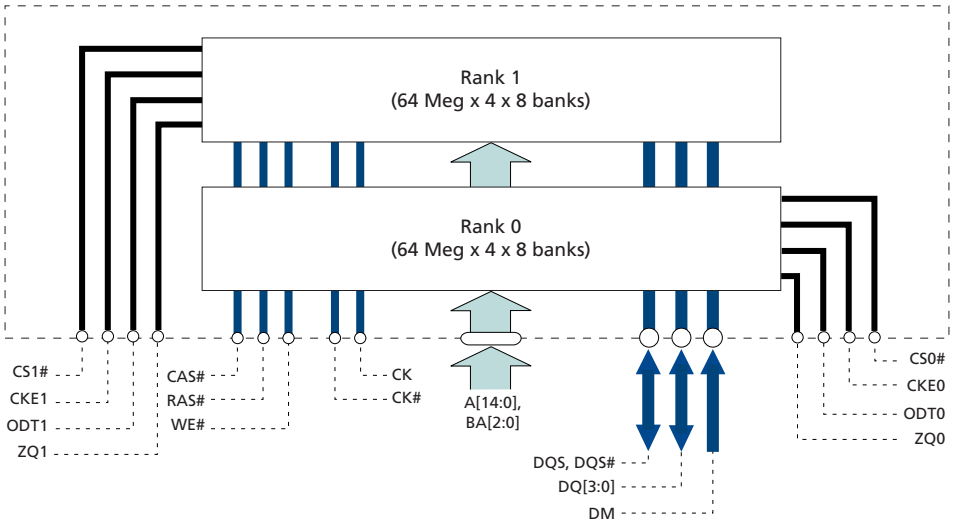
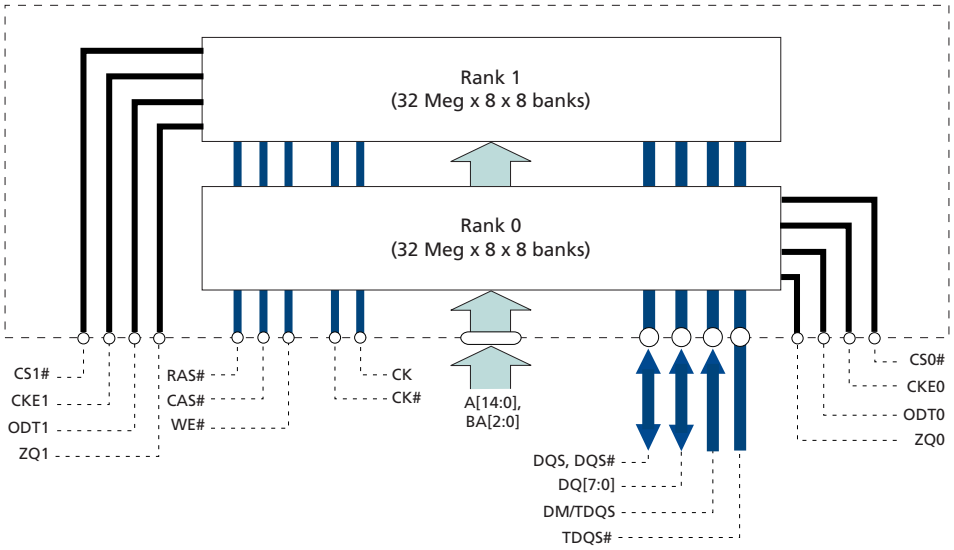


Figure 3: Functional Block Diagram (32 Meg x 8 x 8 Banks x 2 Ranks)



Electrical Specifications – Absolute Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions outside those indicated in the device data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 4: Absolute Maximum DC Ratings

Parameter	Symbol	Min	Max	Units	Notes
V_{DD} supply voltage relative to V_{SS}	V_{DD}	–0.4	1.975	V	1
V_{DD} supply voltage relative to V_{SSQ}	V_{DDQ}	–0.4	1.975	V	
Voltage on any ball relative to V_{SS}	V_{IN}, V_{OUT}	–0.4	1.975	V	
Input leakage current Any input 0V ≤ V_{IN} ≤ V_{DD}, V_{REF} pin 0V ≤ V_{IN} ≤ 1.1V (All other pins not under test = 0V)	I_I	–4	4	µA	
V_{REF} supply leakage current V_{REFDQ} = V_{DD}/2 or V_{REFCA} = V_{DD}/2 (All other pins not under test = 0V)	I_{VREF}	–2	2	µA	2
Operating case temperature	T_C	0	95	°C	3, 4
Storage temperature	T_{STG}	–55	150	°C	

Notes:
1. V_{DD} and V_{DDQ} must be within 300mV of each other at all times, and V_{REF} must not be greater than 0.6 × V_{DDQ}. When V_{DD} and V_{DDQ} are less than 500mV, V_{REF} may be ≤300mV.
2. The minimum limit requirement is for testing purposes. The leakage current on the V_{REF} pin should be minimal.
3. MAX operating case temperature. T_C is measured in the center of the package (see Figure 4 (page 9)).
4. Device functionality is not guaranteed if the DRAM device exceeds the maximum T_C during operation.

Temperature and Thermal Impedance

It is imperative that the DDR3L SDRAM device's temperature specifications, shown in the following table, be maintained in order to ensure the junction temperature is in the proper operating range to meet data sheet specifications. An important step in maintaining the proper junction temperature is using the device's thermal impedances correctly. The thermal impedances listed in Table 6 (page 9) apply to the current die revision and packages.

Incorrectly using thermal impedances can produce significant errors. Read Micron technical note TN-00-08, "Thermal Applications," prior to using the values listed in the thermal impedance table. For designs that are expected to last several years and require the flexibility to use several DRAM die shrinks, consider using final target theta values (rather than existing values) to account for increased thermal impedances from the die size reduction.

The DDR3L SDRAM device's safe junction temperature range can be maintained when the T_C specification is not exceeded. In applications where the device's ambient temperature is too high, use of forced air and/or heat sinks may be required to satisfy the case temperature specifications.

Table 5: Thermal Characteristics

Notes 1–3 apply to entire table

Parameter	Symbol	Value	Units	Notes
Operating temperature	T_C	0 to 85	°C	
		0 to 95	°C	4

Notes:
1. MAX operating case temperature T_C is measured in the center of the package, as shown below.
2. A thermal solution must be designed to ensure that the device does not exceed the maximum T_C during operation.
3. Device functionality is not guaranteed if the device exceeds maximum T_C during operation.
4. If T_C exceeds 85°C, the DRAM must be refreshed externally at 2X refresh, which is a 3.9µs interval refresh rate. The use of self refresh temperature (SRT) or automatic self refresh (ASR), if available, must be enabled.

Figure 4: Temperature Test Point Location

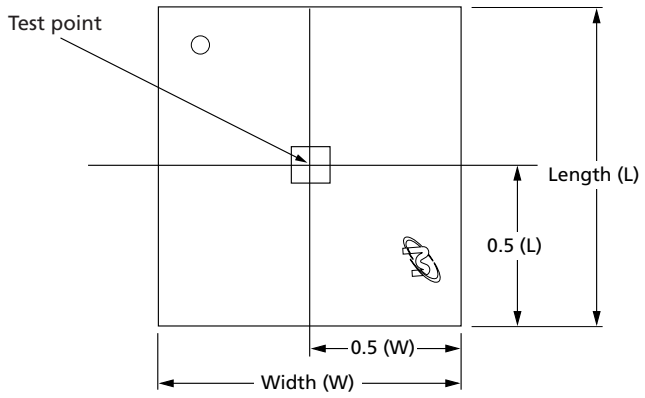


Table 6: Thermal Impedance

Die Rev	Package	Substrate	Θ JA (°C/W) Airflow = 0m/s	Θ JA (°C/W) Airflow = 1m/s	Θ JA (°C/W) Airflow = 2m/s	Θ JB (°C/W)	Θ JC (°C/W)	Notes
D	78-ball	2-layer	61.0	43.7	37.3	27.1	2.8	1
		4-layer	44.5	35.3	31.5	23.2		
M	78-ball	2-layer	TBD	TBD	TBD	TBD	TBD	1
		4-layer	TBD	TBD	TBD	TBD		

Note:
1. Thermal resistance data is based on a number of samples from multiple lots and should be viewed as a typical number.

Electrical Specifications – I_{CDD} Parameters

Table 7: DDR3L I_{CDD} Specifications and Conditions (Rev D)

Note 1 applies to the entire table

Combined Symbol	Individual Die Status	Bus Width	-187E	-15E	Units
I_{CDD0}	$I_{CDD0} = I_{DD0} + I_{DD2P0} + 5$	x4, x8	92	102	mA
I_{CDD1}	$I_{CDD1} = I_{DD1} + I_{DD2P0} + 5$	x4, x8	112	117	mA
I_{CDD2P0} (slow exit)	$I_{CDD2P0} = I_{DD2P0} + I_{DD2P0}$	x4, x8	24	24	mA
I_{CDD2P1} (fast exit)	$I_{CDD2P1} = I_{DD2P1} + I_{DD2P0}$	x4, x8	37	42	mA
I_{CDD2Q}	$I_{CDD2Q} = I_{DD2Q} + I_{DD2P0}$	x4, x8	42	47	mA
I_{CDD2N}	$I_{CDD2N} = I_{DD2N} + I_{DD2P0}$	x4, x8	44	49	mA
$I_{CDD2N\ T}$	$I_{CDD2NT} = I_{DD2NT} + I_{DD2P0}$	x4, x8	52	57	mA
I_{CDD3P}	$I_{CDD3P} = I_{DD3P} + I_{DD2P0}$	x4, x8	42	47	mA
I_{CDD3N}	$I_{CDD3N} = I_{DD3N} + I_{DD2P0}$	x4, x8	47	52	mA
I_{CDD4R}	$I_{CDD4R} = I_{DD4R} + I_{DD2P0} + 5$	x4	142	162	mA
		x8	157	177	
I_{CDD4W}	$I_{CDD4W} = I_{DD4W} + I_{DD2P0} + 5$	x4	152	172	mA
		x8	162	182	
I_{CDD5B}	$I_{CDD5B} = I_{DD5B} + I_{DD2P0}$	x4, x8	202	212	mA
I_{CDD6}	$I_{CDD6} = I_{DD6} + I_{DD6}$	x4, x8	24	24	mA
I_{CDD6ET}	$I_{CDD6ET} = I_{DD6ET} + I_{DD6ET}$	x4, x8	30	30	mA
I_{CDD7}	$I_{CDD7} = I_{DD7} + I_{DD2P0} + 5$	x4, x8	352	402	mA
I_{CDD8}	$I_{CDD8} = 2 \times I_{DD2P0} + 4$	x4, x8	32	32	mA

Note: 1. I_{CDD} values reflect the combined current of both individual die. I_{DDx} represents individual die values.

Table 8: DDR3L I_{CDD} Specifications and Conditions (Rev M)

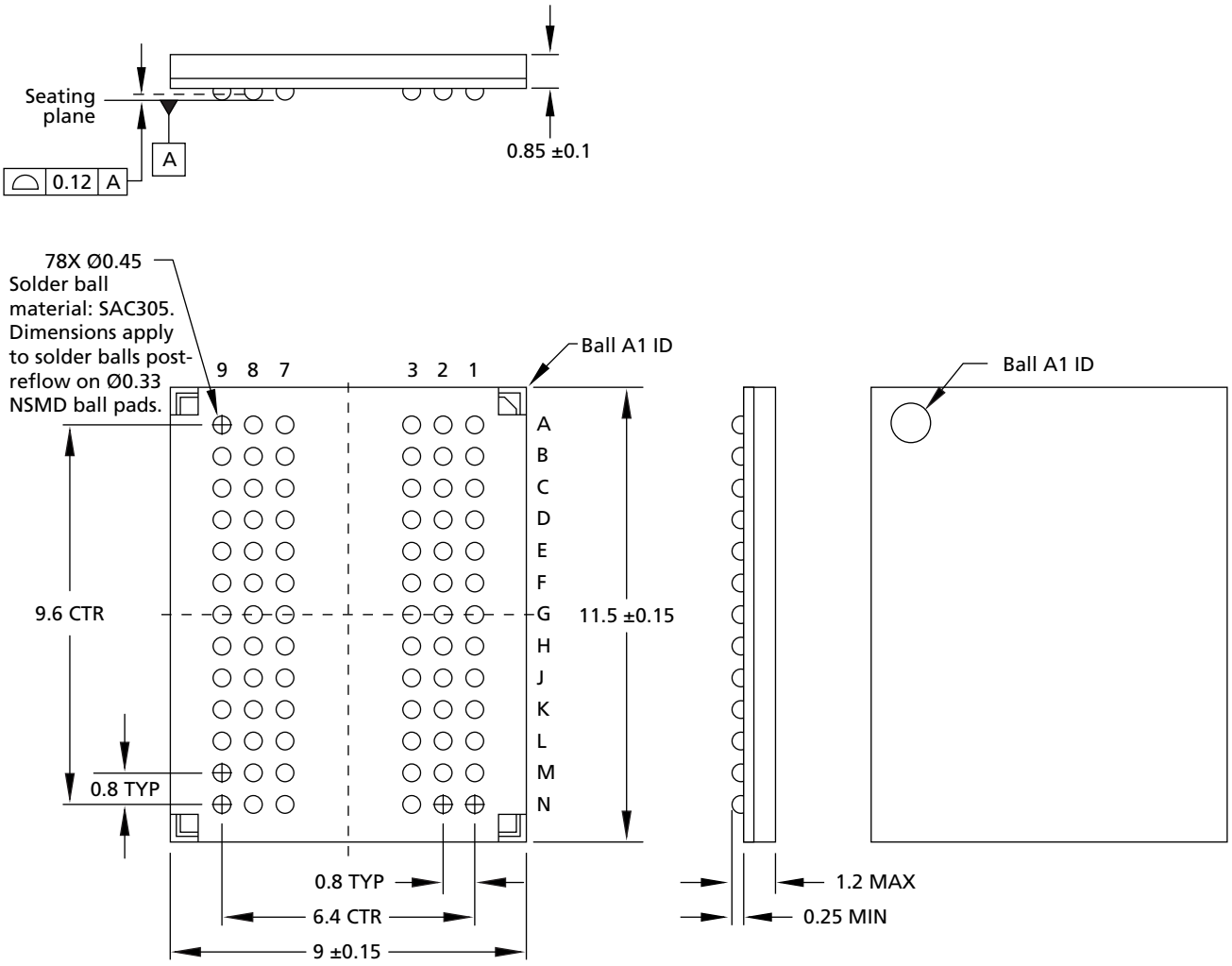
Note 1 applies to the entire table

Combined Symbol	Individual Die Status	Bus Width	-15E	-125	Units
I_{CDD0}	$I_{CDD0} = I_{DD0} + I_{DD2P0}$	x4, x8	67	72	mA
I_{CDD1}	$I_{CDD1} = I_{DD1} + I_{DD2P0}$	x4, x8	82	87	mA
I_{CDD2P0} (slow exit)	$I_{CDD2P0} = I_{DD2P0} + I_{DD2P0}$	x4, x8	24	24	mA
I_{CDD2P1} (fast exit)	$I_{CDD2P1} = I_{DD2P1} + I_{DD2P0}$	x4, x8	40	45	mA
I_{CDD2Q}	$I_{CDD2Q} = I_{DD2Q} + I_{DD2P0}$	x4, x8	40	45	mA
I_{CDD2N}	$I_{CDD2N} = I_{DD2N} + I_{DD2P0}$	x4, x8	42	47	mA
$I_{CDD2N\ T}$	$I_{CDD2NT} = I_{DD2NT} + I_{DD2P0}$	x4, x8	47	52	mA
I_{CDD3P}	$I_{CDD3P} = I_{DD3P} + I_{DD2P0}$	x4, x8	54	59	mA
I_{CDD3N}	$I_{CDD3N} = I_{DD3N} + I_{DD2P0}$	x4, x8	59	64	mA
I_{CDD4R}	$I_{CDD4RCDD4R} = I_{DD4R} + I_{DD2P0}$	x4	122	137	mA
		x8	137	152	
I_{CDD4W}	$I_{CDD4W} = I_{DD4W} + I_{DD2P0}$	x4	112	127	mA
		x8	122	137	
I_{CDD5B}	$I_{CDD5B} = I_{DD5B} + I_{DD2P0}$	x4, x8	197	202	mA
I_{CDD6}	$I_{CDD6} = I_{DD6} + I_{DD6}$	x4, x8	24	24	mA
I_{CDD6ET}	$I_{CDD6ET} = I_{DD6ET} + I_{DD6ET}$	x4, x8	30	30	mA
I_{CDD7}	$I_{CDD7} = I_{DD7} + I_{DD2P0}$	x4, x8	217	232	mA
I_{CDD8}	$I_{CDD8} = 2 \times I_{DD2P0} + 4$	x4, x8	28	28	mA

Note: 1. I_{CDD} values reflect the combined current of both individual die. I_{DDx} represents individual die values.

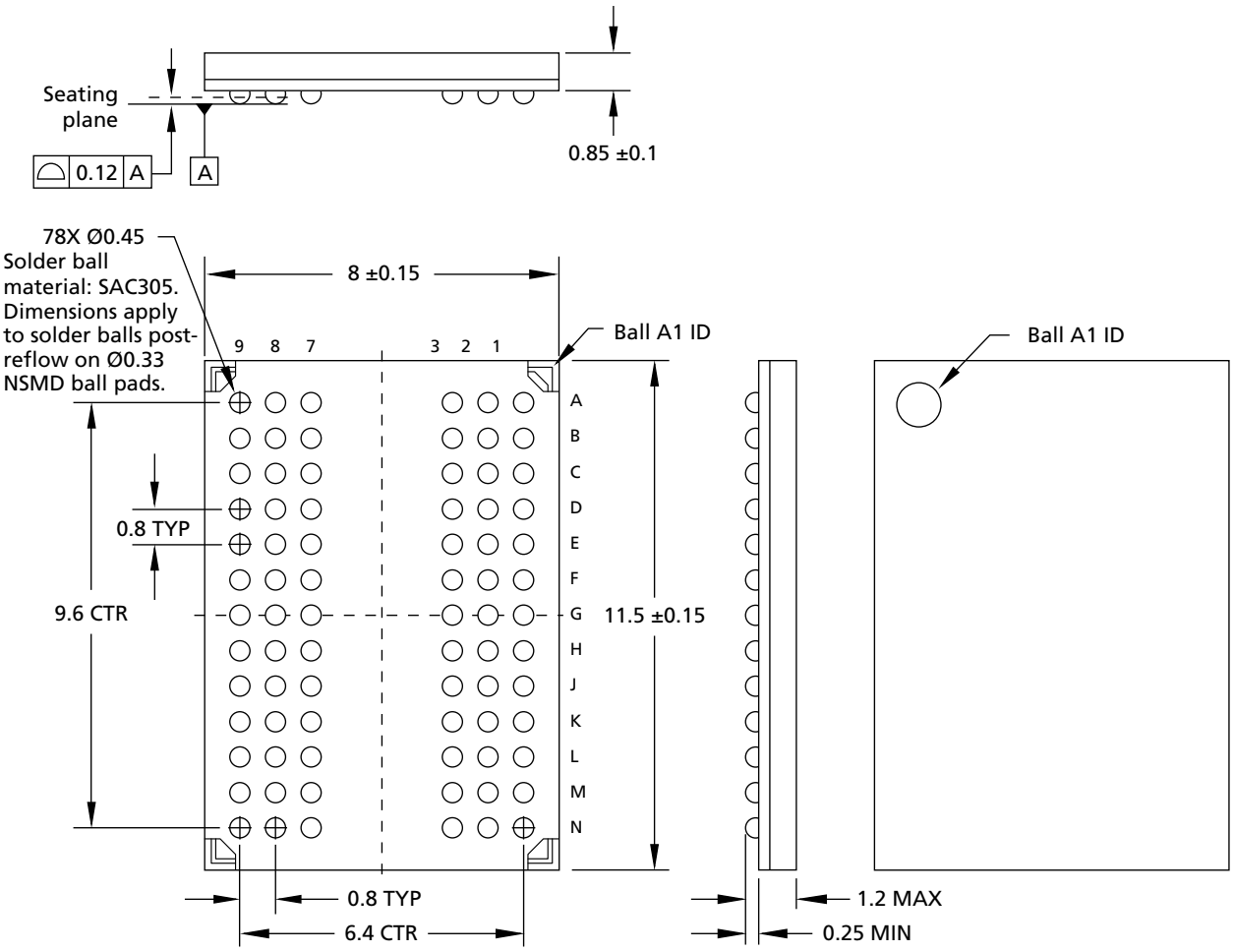
Package Dimensions

Figure 5: 78-Ball FBGA (package code THD)



Notes:
1. All dimensions are in millimeters.
2. Solder ball material: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu).

Figure 6: 78-Ball FBGA (package code THV)



Note: 1. All dimensions are in millimeters.