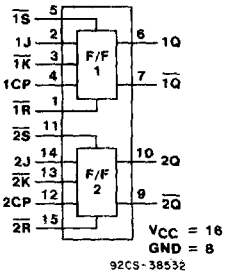
File Number **1667**

CD54/74HC109
CD54/74HCT109

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Dual J-$\bar{K}$ Flip-Flop with Set and Reset

Type Features:

- *Positive-Edge triggered*
- *Asynchronous Set and Reset*
- *60 MHz Typical Maximum Clock Frequency @ V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C*
- *Typical Propagation Delay = 18 ns @ V_{cc} = 5V, C_L = 15pF, T_A = 25°C*
- *Schmitt Trigger Clock Inputs*

The RCA-CD54/74HC109 and CD54/74HCT109 are dual J-$\bar{K}$ flip-flops with set and reset. The flip-flop changes state with the positive transition of Clock (1CP and 2CP).

The flip-flop is set and reset by active-low $\bar{S}$ and $\bar{R}$, respectively. A low on both the set and reset inputs simultaneously will force both Q and $\bar{Q}$ outputs high. However, both set and reset going high simultaneously results in an unpredictable output condition.

The CD54HC109 and CD54HCT109 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC109 and CD74HCT109 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
- *Bus Driver Outputs - 15 LSTTL Loads*
  Wide Operating Temperature Range:
  CD74HC/HCT: —40 to + 85°C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noice Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1$ uA @ V_{OL} V_{OH}

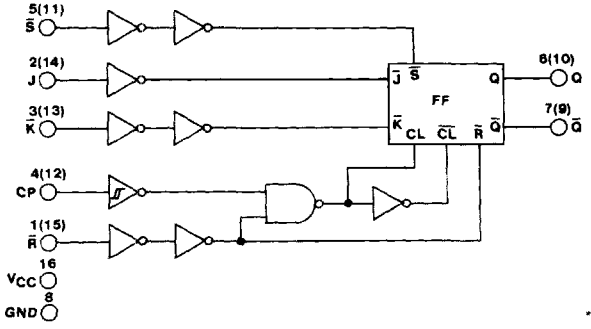


Fig. 1 - Logic diagram

TRUTH TABLE

Inputs					Outputs	
$\bar{S}$	$\bar{R}$	CP	J	$\bar{K}$	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⌒	L	L	L	H
H	H	⌒	H	L	TOGGLE	
H	H	⌒	L	H	NO CHANGE	
H	H	⌒	H	H	H	L
H	H	L	X	X	NO CHANGE	

*Unpredictable and unstable condition if both $\bar{S}$ and $\bar{R}$ go high simultaneously.

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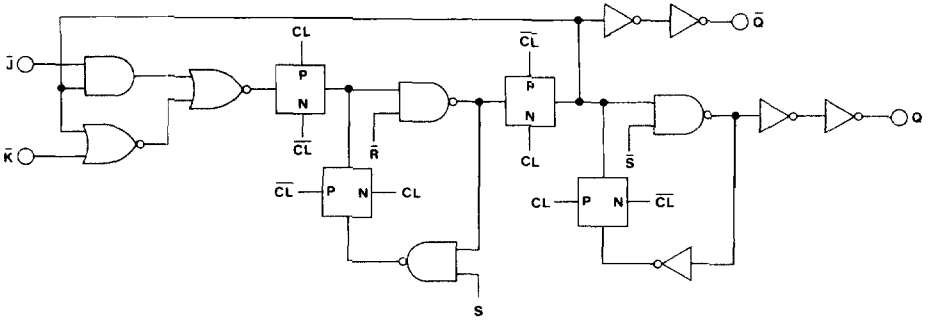

92CM-38536

DETAIL OF FLIP-FLOP

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) ..... -0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5V) ..... ± 20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC}$ +0.5 V) ..... ± 20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V < V_O < V_{CC} +0.5 V) ..... ± 25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC}): ..... ± 50 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) ..... **400 mW**
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... ***Derate Linearly at 6 mW/°C to 70 mW***
OPERATING -TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H ..... -55 to +125°C
PACKAGE TYPE E, M ..... -40 to + 85°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 +150°C
LEAD TEMPERATUARE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300°C

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC		LIMITS MIN.	LIMITS MAX.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*				
CD54/74HC Types		2	6	V
CD54/74HCT Types		4.5	5.5	
DC Input or Output Voltage V_I V_O		0	V_{CC}	V
Operating Temperature T_A:				
CD74 Types		-40	+85	
CD54 Types		-55	+125	°C
Input rise and Fall Times t_r, t_f				
All inputs Except CP	at 2 V	0	1000	
	at 4.5 V	0	500	ns
	at 6 V	0	400	
Input Rise and Fall Times tr, tf				
For CP	at 2 V	0	unlimited	µs
	at 4.5 V	0		
	at 6 V	0		

*Unless otherwise specified, all voltages are referenced to Ground.

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STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC109 / CD54HC109										CD74HCT109 / CD54HCT109									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
	V_I V	Io mA	V_{CC} V	+ 25°C			-40/ + 85°C		-55/ + 125°C		V_I V	V_{CC} V	+ 25°C			-40/ + 85°C		-55/ + 125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—		4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5		4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or VIH	-4	4.5	3.96	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	VIL or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	µA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	4	—	40	—	80	V_{CC} or Gnd	5.5	—	—	4	—	40	—	80	µA
Additional quiescent Device Current ΔI_{CC}* per input pin: 1 unit load											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	µA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
All	0.3

*Unit Load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 µA max. @ 25°C

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r,t_f = 6 ns)

CHARACTERISTIC		C_L (pF)	Typical 54/74HC	Typical 54/74HCT	UNITS
Propagation Delay, CP → Q, Q	t_{PLH} t_{PHL}	15	14	17	ns
$\overline{S}$ → Q	t_{PLH}	15	9	12	ns
$\overline{S}$ → $\overline{Q}$	t_{PHL}	15	13	19	ns
$\overline{R}$ → Q	t_{PHL}	15	15	19	ns
$\overline{R}$ → $\overline{Q}$	t_{PLH}	15	14	15	ns
CP Frequency	f_{MAX}	15	60	54	MHz
Power Dissipation Capacitance*	C_{PD}*	—	30	33	pF

*C_{PD} is used to determine the dynamic power consumption, per flip-flop.

$P_D = C_{PD} V_{CC}^2 f_i + \Sigma V_{CC}^2 C_L f_o$ where:

f_i = Input Frequency

C_L = Output Load Capacitance
V_{CC} = Supply Voltage
f_o = Output Frequency

PREREQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC		TEST CONDITION V_{CC} V	LIMITS 25°C HC Min.	HC Max.	HCT Min.	HCT Max.	-40°C to +85°C 74HC Min.	74HC Max.	74HCT Min.	74HCT Max.	-55°C to +125°C 54HC Min.	54HC Max.	54HCT Min.	54HCT Max.	UNITS
Set-up Time J, $\overline{K}$ to CP	t_{SU}	2	80		—		100		—		120		—		ns
		4.5	16		18		20		23		24		27		
		6	14		—		17		—		20		—		
Hold Time J, $\overline{K}$ to CP	t_h	2	5		—		5		—		5		—		ns
		4.5	5		3		5		3		5		3		
		6	5		—		5		—		5		—		
Removal Time $\overline{R}$, $\overline{S}$ to CP	t_{REM}	2	80		—		100		—		120		—		ns
		4.5	16		18		20		23		24		27		
		6	14		—		17		—		20		—		
Pulse Width CP, $\overline{R}$, $\overline{S}$	t_w	2	80		—		100		—		120		—		ns
		4.5	16		18		20		23		24		27		
		6	14		—		17		—		20	—			
CP Frequency	f_{MAX}	2	6		—		5		—		4		—		MHz
		4.5	30		27		25		22		20		18		
		6	35		—		29		—		23		—		

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SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC		V_{CC}	25°C				-40°C to + 85°C				-55°C to + 125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay, CP → Q, $\overline{Q}$	t_{PHL}	2		175		—		220		—		265		—	ns
	t_{PHL}	4.5		35		40		44		50		53		60	
		6		30		—		37		—		45		—	
$\overline{S}$ → Q	t_{PLH}	2		120		—		150		—		180		—	ns
		4.5		24		30		30		38		36		45	
		6		20		—		26		—		31		—	
$\overline{S}$ → $\overline{Q}$	t_{PHL}	2		155		—		195		—		235		—	ns
		4.5		31		45		39		56		47		68	
		6		26		—		33		—		40		—	
$\overline{R}$ → Q	t_{PHL}	2		185		—		230		—		280		—	ns
		4.5		37		45		46		56		56		68	
		6		31		—		39		—		48		—	
$\overline{R}$ → $\overline{Q}$	t_{PLH}	2		170		—		215		—		255		—	ns
		4.5		34		37		43		46		51		56	
		6		29		—		37		—		43		—	
Transition Times	t_{TLH}	2		75		—		95		—		110		—	ns
	t_{THL}	4.5		15		15		19		19		22		22	
		6		13		—		16		—		19		—	
Input Capacitance	C_I			—		—		—		—		—		—	pF
				10		10		10		10		10		10	
				—		—		—		—		—		—	

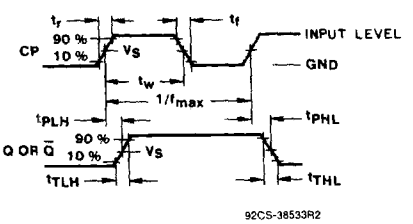

Fig. 2 - Clock to output delays and clock pulse width.

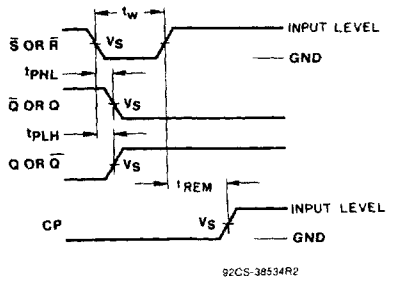

Fig. 3 - $\overline{Reset}$ or $\overline{Set}$ prerequisite and propagation delays.

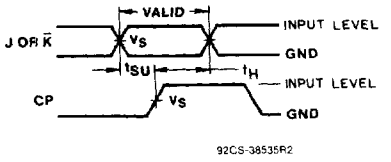

Fig. 4 - Data set-up and hold times.

	54/74 HC	54/74 HCT
Input Level	V_{CC}	3V
Switching Voltage, V_S	50% V_{CC}	1.3V