Radiation Tolerant 8-Channel Source Driver

Description

The AAHS298B is part of Microsemi's new family of Radiation Tolerant products aimed at the aerospace and defense markets. The AAHS298B is a Radiation-Tolerant source driver with eight non-inverting channels, with internal thermal shutdown.

Capable of providing an interface from TTL, 5V or 12V logic systems to relays, motors, solenoids, and other loads, this device adds the additional benefit of an internal thermal shutdown and output transient protection/clamp diodes with sustaining voltages to 75V.

Each output is capable of sourcing 700mA with a withstand voltage of 75V over the full military temperature range. The thermal shutdown is intended to protect against over-current and soft-start occurrences.

The AAHS298B is offered in 20-pin ceramic SOIC package with formed and flat leads. The AAHS298B has demonstrated tolerance to 100kRad (Si) total dose (min), 50kRad (Si) ELDRS (min), as well as immunity to latch-up and SEE tolerance.

Features

- 700mA Output Source Current
- Zero Quiescent Off Current
- Full Channel Isolation to Prevent Fault Propagation
- Internal Ground Clamp Diodes
- 75V Output Breakdown Voltage
- TTL, 5V and 12V Logic Compatible
- Internal Thermal Shutdown
- Radiation tolerant to 100kRad(Si) Total Dose, 50kRad (Si) ELDRS
- -55°C to +125°C Temperature Range
- Available in 20-pin Ceramic SOIC with formed and flat Leads
- QML listed with SMD 5962-15231

Applications

- Relay/Solenoid Drivers
- Lamp/LED Drivers
- Stepper and/or Servo Motor Drivers

Product Highlight

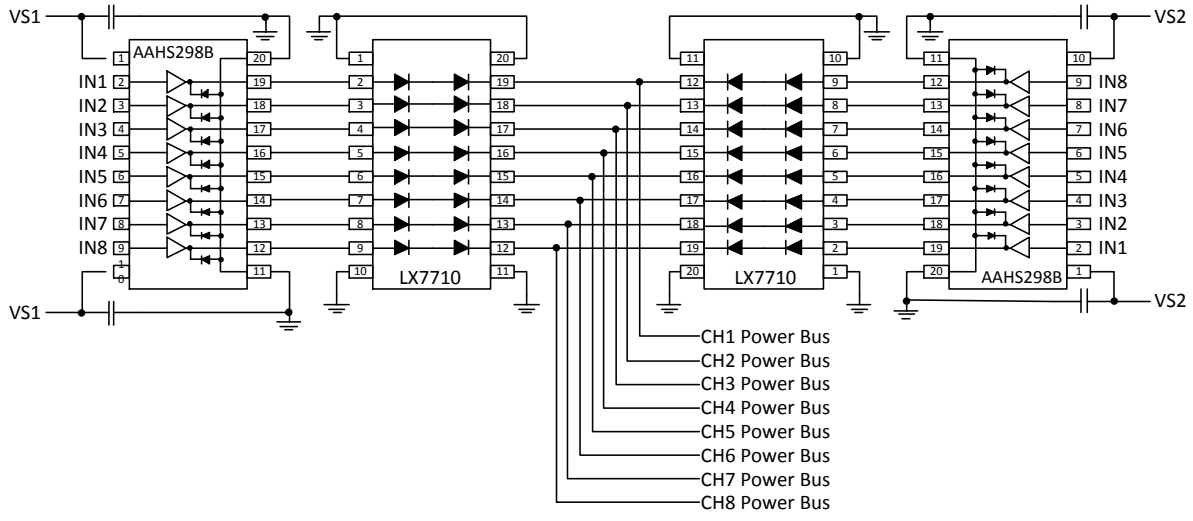
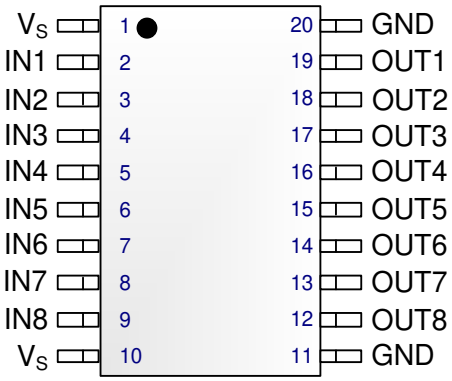


Figure 1 · Redundant Switchable Power Bus

Pin Configuration and Pinout



S20 PACKAGE

Ordering Information

Ambient Temperature	Type	Package	Part Number	Flow	Packaging Type
-55°C to 125°C	Hermetic	CSOIC 20L Flat Lead	AAHS298B-07-4020A-V SMD 5962-1523101VYC	QML-V	Tray
			AAHS298B-06-4020A-Q SMD 5962-1523101QYC	QML- Q	
-55°C to 125°C	Hermetic	CSOIC 20L	AAHS298B-S-S20B-S SMD 5962-1523101VXC	QML-V	
			AAHS298B-S-S20B-B SMD 5962-1523101QXC	QML- Q	
0°C to 70°C			AAHS298B-S-S20B-ENGR	Commercial	

Pin Description

Pin Number	Pin Designator	Description
1, 10	Supply Voltage	Input Supply Voltage, both pins should be externally connected on the PCB to improve the internal current distribution and allow the device to safely provide the maximum 2800mA of continuous supply current.
2-9	IN[1:8]	8 Logic Inputs, TTL, CMOS & High Voltage (12V) compatible. With all inputs low the device is in sleep mode.
11, 20	GND	Ground, both pins should be externally connected externally on the PCB to improve the internal current distribution and improve forward voltage of the flyback clamping diodes.
12-19	OUT[1:8]	700mA Source Outputs.

Block Diagram

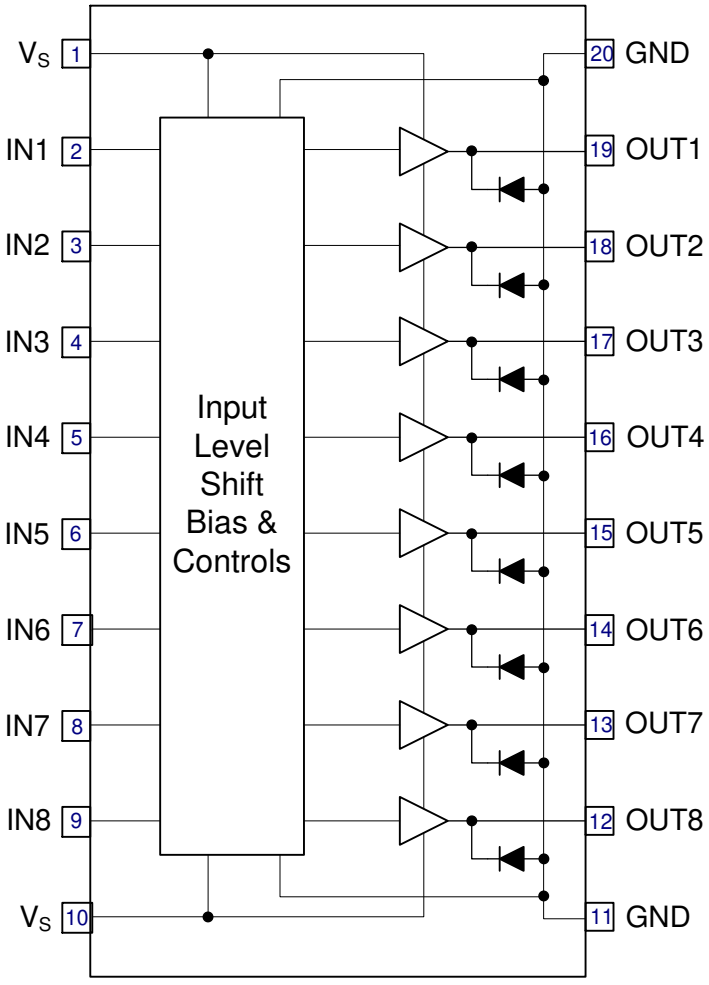


Figure 2 · AAHS298B Simplified Block Diagram

Absolute Maximum Ratings

Parameter	Value	Units
Supply Voltage (VS, Max voltage between VS and GND)	-0.5 to 75	V
Digital Inputs (IN[1:8], Max voltage between INPUT & GND)	-0.5 to 15	V
Output Voltage (OUT[1:8], Maximum voltage between OUT[1:8] and GND)	75	V
Single Output Continuous Current (OUT[1:8])	-700	mA
Single Output Peak Current (OUT[1:8], ≤ 1 second)	-1200	mA
Multiple Output Simultaneously Continuous Current (OUT[1:8])	-2800	mA
ESD (all pins, HBM)	2000	V
Operating Junction Range	-55 to 150	°C
Storage Temperature Range	-65 to 150	°C
Lead Temperature (Soldering, 10 Seconds)	300	°C
Peak Package Solder Reflow Temp. (40 sec. max. exp.)	260 (+0, -5)	°C
Lead Temperature. (Soldering 10 seconds)	300	°C

Exceeding these ratings could cause damage to the device. All voltages are with respect to GND. Currents are positive into, negative out of specified terminal. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” are not implied. Exposure to “Absolute Maximum Ratings” for extended periods may affect device reliability.

Thermal Data

Parameter	Value	Units
S20 Package:		
Thermal Resistance-Junction to Case, θ_{JC}	2.24	°C/W

Note: The θ_{JC} number is for conduction only to the ceramic base of the package. It assumes that the ceramic base has a thermal epoxy underneath the ceramic package to exhaust the heat from the package into the PCB, or other mounting surface.

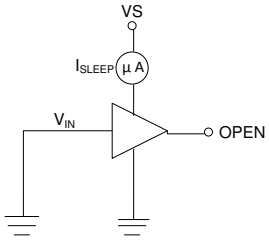
Electrical Characteristics

Unless otherwise stated the following specifications apply over operating ambient temperature of -55°C < Temp < 125°C, V_S = 50V, 100kRad (Si) TID (min), 50kRad (Si) ELDRS (min)

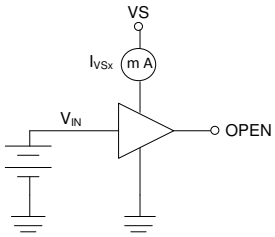
Symbol	Parameter	Test Condition	Test Setup	Min	Typ	Max	Units
Operating Supply Current							
I_{SLEEP}	Standby Supply Current	IN[1:8] = 0.0V, No Output Load	1		1	20	µA
$I_{VS2.5}$	Active Supply Current	IN[1:8] = 2.5V, No Output Load	2		5	25	mA
I_{VS5}	Active Supply Current	IN[1:8] = 5.0V, No Output Load			7	25	
AC Characteristics							
t_{on}	Output Turn On Delay Time	Load = 470Ω, 100pF, V_S = 45V V_{IL} = 0.8; V_{IH} = 2.5V				2	µs
t_{off}	Output Turn Off Delay Time					10	
t_R	Output Rise Time (10% to 90%)					2	
t_F	Output Fall Time (90% to 10%)					10	
DC Characteristics							
V_S	Supply Voltage Range			10		50	V
$THSD_{TRIP}$	Thermal Shutdown Trip Temperature			135	155	175	ºC
$THSD_{RST}$	Thermal Shutdown Reset Temperature	Restarts at 125ºC		125			
V_{IH}	Input High Level		3	2.5			V
V_{IL}	Input Low Level					0.8	
VCE_{SAT}	Output Saturation at 350mA	IN[1:8] = 2.5V	4		1.7	2.2	
VCE_{SAT}	Output Saturation at 500mA				1.8	2.3	
VCE_{SAT}	Output Saturation at 700mA				2.1	2.7	
I_{IH}	Input High Leakage	IN[1:8] = 5.0V	5		60	100	µA
I_{IL}	Input Low Leakage	IN[1:8] = 0.0V			0.1	10	
I_{OL}	Output Low Leakage	Output OFF, VOUTX = 0.0V	6		2	50	
V_F	Clamp Diode Forward Voltage	I_F = 200mA	7			2.5	V
		I_F = 700mA				3.0	
I_R	Clamp Diode Leakage Current	V_R = 50V	8			50	µA

Parameter Test Configurations

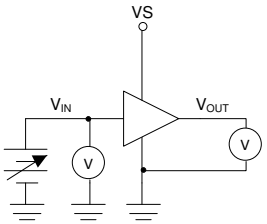
(See test setup numbers in Electrical Characteristics Table)



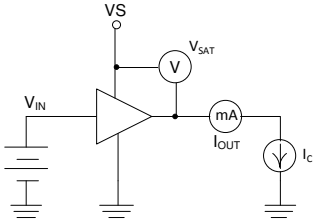
Test Setup 1
Standby Supply Current



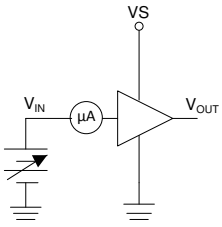
Test Setup 2
Active Supply Current



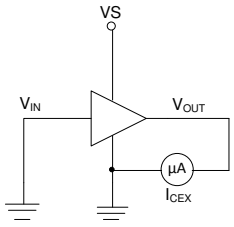
Test Setup 3
Input Threshold Voltage



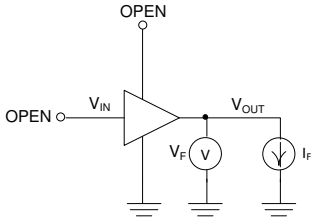
Test Setup 4
$V_{CE(sat)}$ Test Circuit



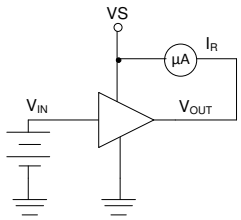
Test Setup 5
Input Bias Current



Test Setup 6
Output Leakage Current



Test Setup 7
Clamp Diode Forward Voltage



Test Setup 8
Clamp Diode Leakage Current

Single Channel Block Diagram

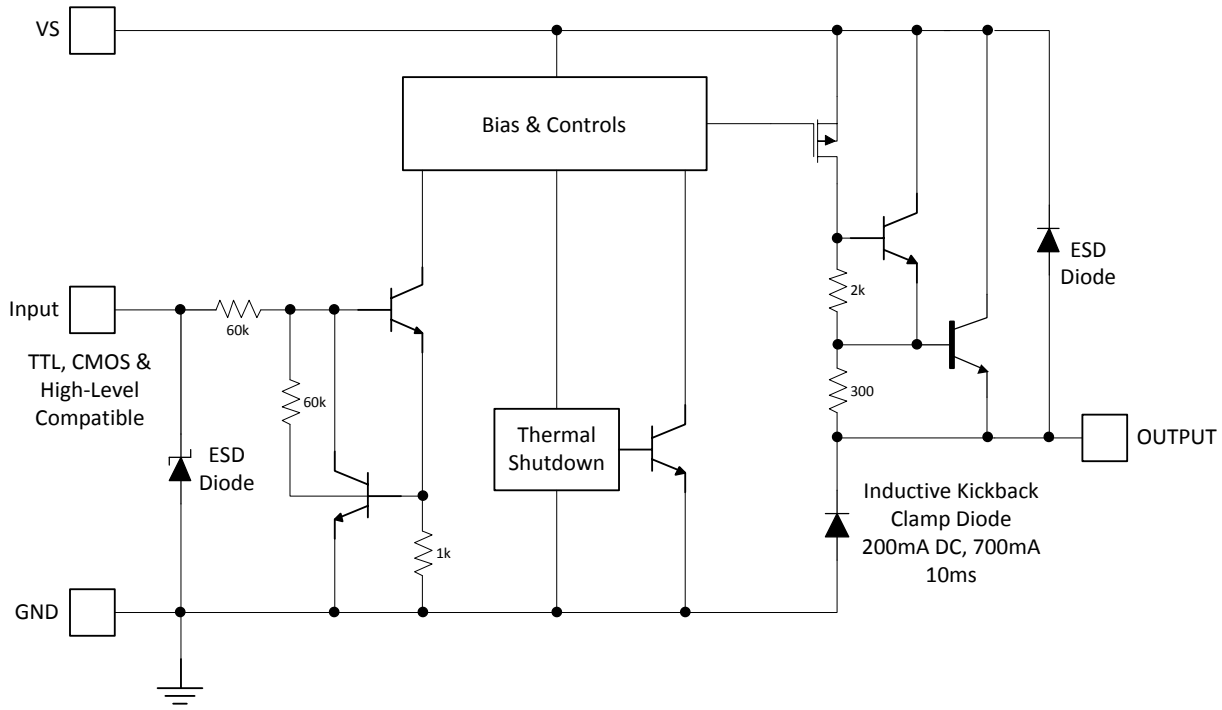


Figure 3 · AAHS298B Single Channel Simplified Block Diagram

Application Information

VS Pins

The AAHS298B has two VS (Input Supply) pins (pins 1, 10). The maximum 2800mA total supply current limit for the AAHS298B comes from the supply bond wires current capability, these bond wires will fuse open around 2A each. By externally connecting these two pins on the printed-circuit board the utilization of two pins one at each end of the package improves the internal current distribution. With only one VS pin connected, the saturation voltage would progressively increase from the near to the far channel due to internal IR losses in the die metallization, and the part will not be capable of the full 2800mA, only 1400mA.

IN Pins

The IN (Inputs) pins are compatible with TTL (5V), CMOS (3V) & High-Level (12V) logic levels and not only turn on their respective output but also provide bias to the device activating for instance the thermal shutdown circuitry. Conversely if all IN pins are low the device is off with no quiescent current, and the device is in sleep mode.

OUT Pins

The OUT (Output) pins are switched high-side drivers designed to output 700mA continuous current with a typical saturation voltage drop of 2.1V. See figure 4 for the typical saturation voltages with changes in output current and temperature. At the rated maximum continuous operating current which is 700mA, the saturation voltage still has a negative temperature coefficient as indicated in the chart. This is advantageous since it reduces the power dissipation when the device operates at elevated temperatures.

Above 700mA the saturation increases more rapidly and due to the design of the output transistors the output current self-limits itself around 1.4A, but could reach the bond-wire fusing current of 2A on a "dead" short-circuit condition in a matter of milliseconds. This is a protection feature designed to isolate a shorted output under overstress while allowing the remaining outputs to function normally. The 700mA per channel current was therefore determined to be around 50% of the drive maximum capability of the output transistors.

Thermal Shutdown

The thermal shut-down circuitry is located in the center of the die between channels 4 & 5. The die being relatively thick, and the silicon being a good conductor of heat, the temperature gradient at the surface of the die, say between channel #1 and #4 cannot exceed a few degrees centigrade.

When all channels are dissipating power, the Junction to Case Thermal Resistance is less than 3°C/W when measured between the junctions at the surface of the silicon and the bottom of the ceramic package. The Junction to Case thermal resistance for one channel only is less than 20°C/W.

When the package is mounted with a heat pad under it on a PCB equipped with an integral heat-sink, the Junction to PCB thermal resistance could be of the order of 10°C/W, and in this condition which we have verified, it is almost impossible for the thermal shut-down circuitry to trip.

On the contrary, if the part is simply mounted on the PCB with no heat sinking we have been able to make the thermal shutdown trip with the PCB at room temperature with 4 channels ON at full load (2800mA total creating approximately 6W of power dissipation).

There is a time constant associated with the thermal shut-down circuitry which measures in seconds and this is why we cannot rely on it to protect the part against "dead" short-circuits during which the current could exceed 2A and blow the bond wire in 10 to 20mS.

Clamp Diodes

Each output channel includes an integrated clamp diode to protect against possible inductive kick-backs. These diodes are rated for 200mA DC current at a maximum of 2.5V, and can withstand 700mA for about 10ms. Like the VS pins by externally connecting the two GND pins together on the printed-circuit board the utilization of both pins one at each end of the package improves the internal current distribution and losses.

It is very important to recirculate any flyback current close to the source to minimize noise issues. When using the AAHS298B's built-in output transient suppression diodes for this purpose the PCB layout or wiring should insure that the digital input side and output power sides do not share ground paths, and the conductors and/or traces are sized accordingly. When the proximity of the inductive load is some distance from the driver then an additional 'freewheel diode', or snubber circuit may be required to minimize noise and clamp voltage excursions. If using the internal diode causes other complications (delay times, etc.) a varistor or transorb may be used instead. Keeping the power and digital grounds separate and only connecting them at the one star ground point should minimize and ground loop or bounce issues.

Characteristic Curves

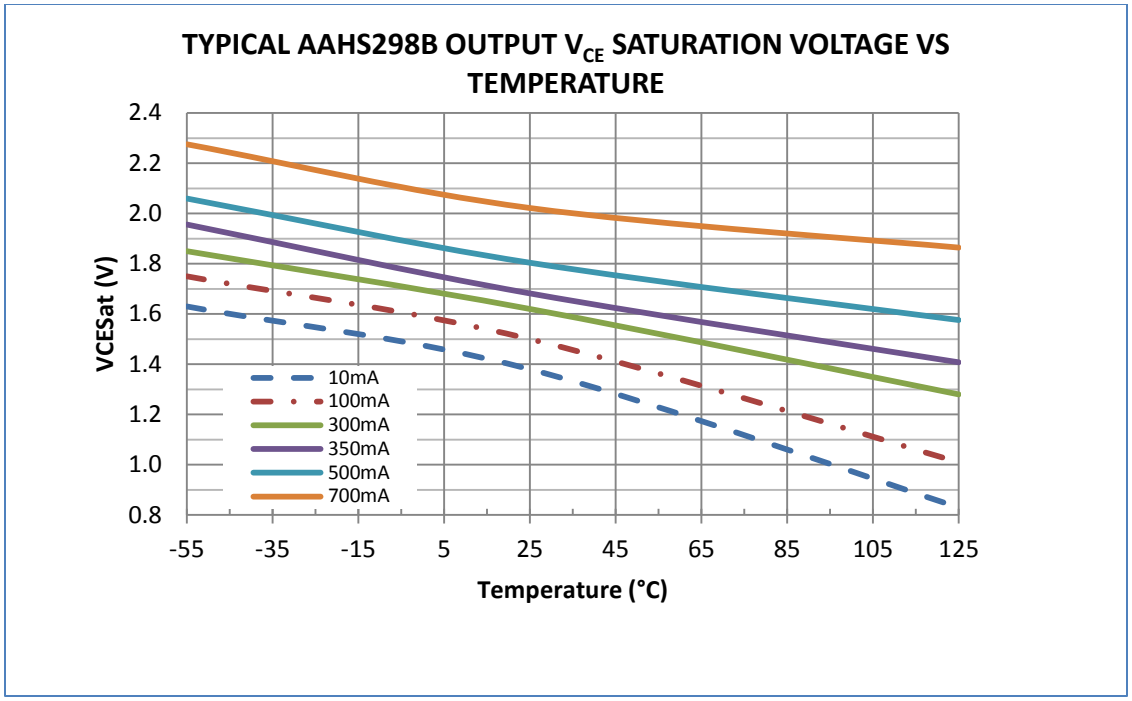


Figure 4 · Typical Output V_{CE} vs Saturation Voltage

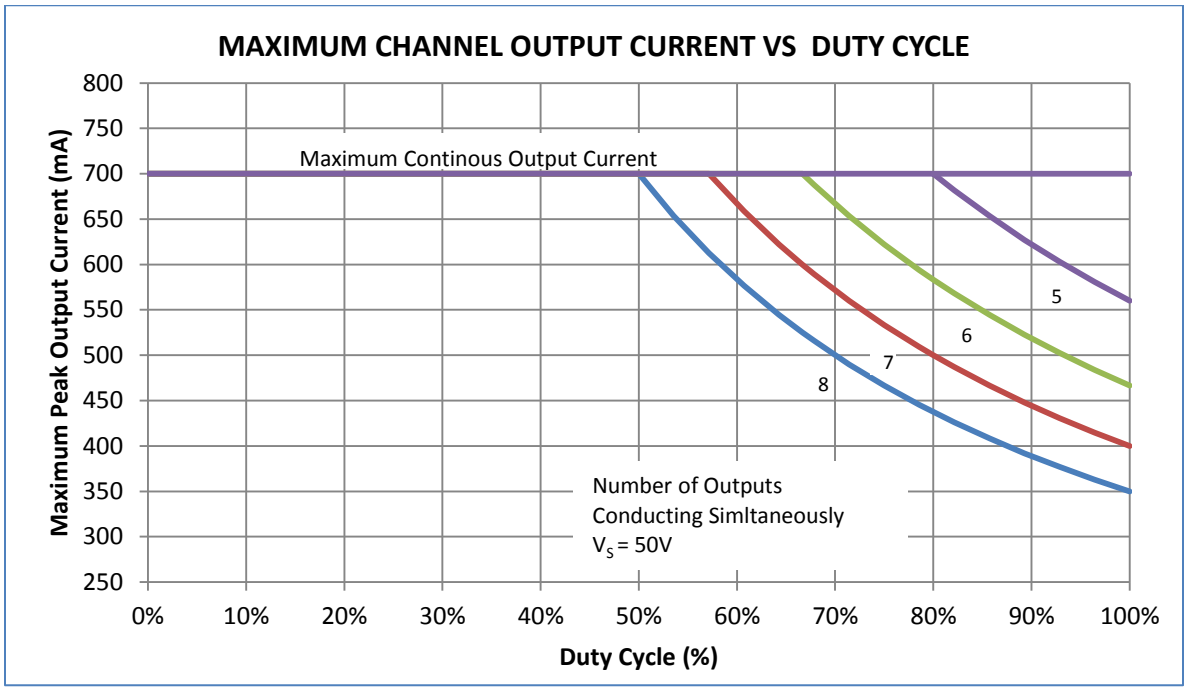
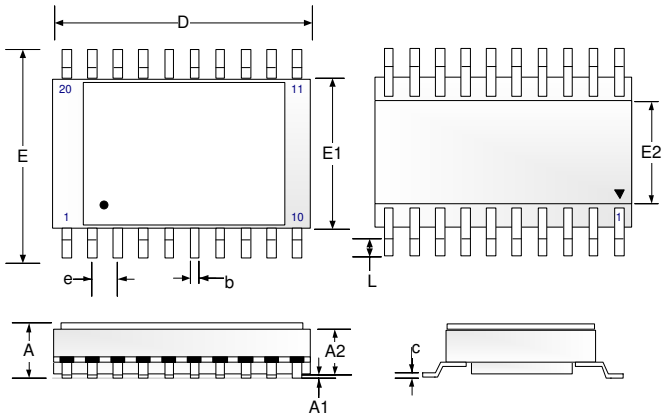


Figure 5 · Maximum Channel Output vs Duty Cycle
(≤ 4 channels may be operated continuously at maximum current within package power limitations)

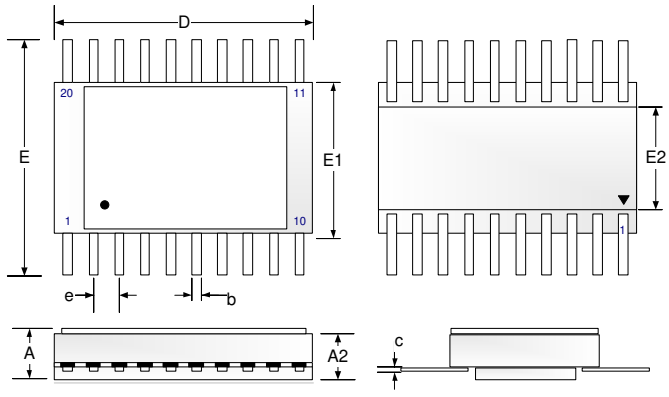
Package Outline Dimensions

Controlling dimensions are in inches, metric equivalents are shown for general information.



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.28	2.92	0.090	0.115
A1		0.38		0.015
A2	1.78	2.41	0.070	0.095
b	0.36	0.48	.0140	.0190
c	0.15	0.25	0.006	0.010
D	12.45	13.08	0.490	0.515
E	10.16	11.18	0.400	0.440
E1	7.24	7.62	0.285	0.300
E2	4.70 BSC		0.185 BSC	
e	1.27 BSC		0.050 BSC	
L	0.50	0.76	0.020	0.030

Figure 6 · S20 20-Lead Ceramic SOIC Package Dimensions



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.03	2.67	0.080	0.105
A2	1.78	2.41	0.070	0.095
b	0.36	0.48	.0140	.0190
c	0.15	0.25	0.006	0.010
D	12.45	13.08	0.490	0.515
E	21.00	24.00	0.827	0.945
E1	7.24	7.62	0.285	0.300
E2	4.70 BSC		0.185 BSC	
e	1.27 BSC		0.050 BSC	

Figure 7 · S20 20-Lead Ceramic SOIC Package with Flat Leads Dimensions

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA

Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

E-mail: sales.support@microsemi.com

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