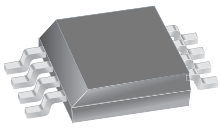
Dual Channel Switch Interface IC

FEATURES AND BENEFITS

- 4.75 to 26.5 V operation
- Low V_{IN}-to-V_{OUT} voltage drop
- $^1/_{10}$ current sense feedback
- Survive short-to-battery and short-to-ground faults
- Survive 40 V load dump
- >4 kV ESD rating on the output pins, >2 kV on all other pins
- Output current limiting
- Low operating and Sleep mode currents
- Integrates with Allegro A114x and A118x Hall effect two-wire sensor ICs

PACKAGE: 8-pin SOIC (suffix L)



Approximate Footprint 

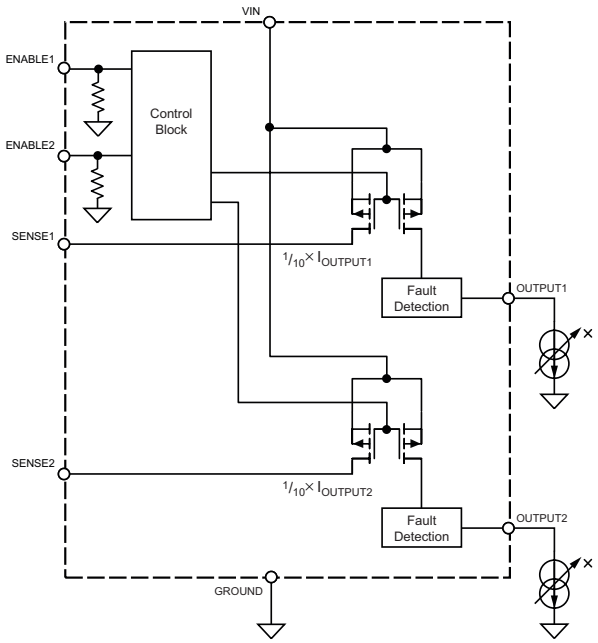
DESCRIPTION

The Allegro™ A6850 is designed to interface between a microprocessor and a pair of two-wire Hall effect sensor ICs. The A6850 uses protected high-side low resistance DMOS MOSFETs to switch the supply voltage to the two Hall effect devices. Each switch can be controlled independently via individual ENABLE pins and both switches are protected with current-limiting circuitry. The output switches are rated to operate to 26.5 V and will source at least 25 mA per channel before current limiting.

Typical two-wire Hall device applications require the user to measure the supply current to determine whether the Hall IC is switched on (magnetic field present) or switched off (no magnetic field present). This is usually accomplished by using an external series shunt resistor and protection circuits for the microprocessor. In many systems, the sensed voltage is used as the input to a microprocessor analog-to-digital (A-to-D) input. This provides the system with an indication of the status of the two-wire switch as well as provides the capability for diagnostic information if there is an open or shorted Hall device.

Continued on the next page…

Functional Block Diagram



Description (continued)

The A6850 eliminates the need for the external series shunt resistor in Hall device applications by incorporating an integrated current mirror which reports the Hall IC supply current as a $^{1}/_{10}$ value on the SENSE1 or SENSE2 output pin. A low current Sleep mode is available (<15 µA) by driving both ENABLE pins low. Also, the A6850 can be used to interface to mechanical switches.

The A6850 is supplied in an 8-pin Pb (lead) free SOIC package, with 100% matte tin leadframe plating.

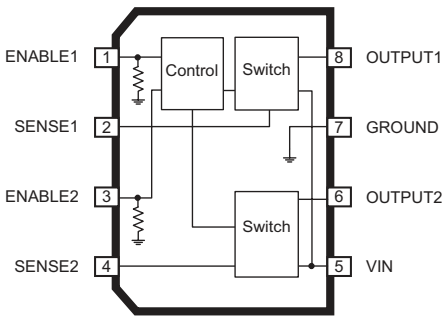
Selection Guide

Part Number	Packing
A6850KLTR-T	13-in. reel, 3000 pieces/reel

Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	V_{IN}		40	V
Output Voltage	$V_{OUTPUTx}$		–0.3 to 40	V
SENSE*x* Voltage Range	V_{SENSEx}		–0.3 to 7	V
ENABLE*x* Voltage Range	$V_{ENABLEx}$		–0.3 to 7	V
Operating Ambient Temperature	T_A		–40 to 150	ºC
Maximum Junction Temperature	T_J(max)		150	ºC
Storage Temperature	T_{stg}		–55 to 150	ºC
ESD Rating - Human Body Model	HBM	AEC-Q100-002; OUTPUT1 and OUTPUT2	4.5	kV
		AEC-Q100-002; all other pins	2.5	kV
ESD Rating - Charged Device Model	CDM	AEC-Q100-011; all pins	1050	V

Pinout Diagram



Terminal List Table

Name	Number	Description
ENABLE1	1	Digital input pulled to ground
SENSE1	2	Sensed current output
ENABLE2	3	Digital input pulled to ground
SENSE2	4	Sensed current output
VIN	5	Chip power supply voltage
OUTPUT2	6	Switchable voltage supply to sensor IC
GROUND	7	Ground reference
OUTPUT1	8	Switchable voltage supply to sensor IC

THERMAL CHARACTERISTICS may require derating at maximum conditions, see application information

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	4-layer PCB based on JEDEC standard	80	ºC/W
		1-layer PCB with copper limited to solder pads	140	ºC/W

*Additional thermal data available on the Allegro Web site.

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ELECTRICAL CHARACTERISTICS at T_J = -40 to +150°C (unless noted otherwise)

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply Input Voltage Range	V_{IN}		4.75	–	26.5	V
Supply Input Quiescent Current	I_{INQ}	Operating mode, $I_{OUTPUTx}$ = 0 mA	–	–	5.0	mA
		Sleep mode: ENABLE1 and ENABLE2 low $V_{OUTPUT1} = V_{OUTPUT2}$ = 0 V	–	–	15	µA
Power-Up Time[1]	t_{ON}		–	–	20	µs
Output Rise Time[2]	t_{rLH}	$I_{OUTPUTx}$ = 0 to –10 mA, 10% to 90%V_{SENSEx}	–	0.18	1.5	µs
Output Fall Time[2]	t_{fHL}	$I_{OUTPUTx}$ = 0 to –10 mA, 90% to 10%V_{SENSEx}	–	1.4	3.5	µs
Enable Delay Time[2]	$t_{ENdlyLH}$	$I_{OUTPUTx}$ = –5 mA, 50% ENABLEx to 50%V_{SENSEx}	–	150	500	ns
Disable Delay Time[2]	$t_{ENdlyHL}$	$I_{OUTPUTx}$ = –5 mA, 50% ENABLEx to 50%V_{SENSEx}	–	4.0	7.5	µs
OUTPUTx Source Resistance	$R_{DS(on)}$	$I_{OUTPUTx}$ = –20 mA	–	–	35	Ω
OUTPUTx Leakage Current	$I_{OUTPUTQ}$	$V_{OUTPUTx}$ = 0 V; disabled	–	–	–20	µA
SENSE*x* Output Current Offset[3]	$I_{SENSE(ofs)}$	$I_{SENSEx} = (I_{OUTPUTx} / 10) + I_{SENSE(ofs)}$, I_{OUTPUT} = –2 mA to –20 mA	–100	–	100	µA
	I_{SENSEQ}	V_{SENSEx} = 0 V; disabled	–	–	10	µA
SENSE*x* Voltage[4]	V_{SENSEx}	V_{IN} > 7 V	0	–	6	V
		V_{IN} < 7 V	0	–	V_{IN} – 1	V
ENABLE*x* Input Voltage Range	$V_{ENABLEH}$		2.0	–	–	V
	$V_{ENABLEL}$		–	–	0.4	V
ENABLE*x* Input Hysteresis	$V_{ENABLEhys}$	At least one output enabled	125	–	375	mV
ENABLE*x* Current	I_{ENABLE}	ENABLE*x* = 2.0 V	–	40	100	µA
		ENABLE*x* = 0.4 V	–	8.0	20	µA
OUTPUT Current Limit	$I_{OUTPUTM}$		–25.0	–35.0	–45.0	mA
OUTPUT Reverse Bias Current	$I_{OUTPUT(rvrs)}$	Reverse bias blocking: V_{IN} = 4.75 V, V_{OUTPUT} = 26.5 V	–	500	750	µA
Overvoltage Protection Threshold	V_{OVP}	Rising V_{IN}	27.0	–	33.0	V
Overvoltage Protection Hysteresis	V_{OVPhys}		–	2.0	–	V
Thermal Shutdown Threshold	T_{TSD}	Temperature Increasing	–	175	–	°C
Thermal Shutdown Hysteresis	T_{TSDhys}		–	15	–	°C

[1]Delay from end of Sleep mode to outputs enabled.

[2] R_{SENSEx} = 1.5 kΩ.

[3]For input and output current specifications, negative current is defined as coming out of (sourced from) the specified device pin.

[4]User to ensure that V_{SENSEx} remains within the specified range. If V_{SENSEx} exceeds the maximum value, the device is self-protected by an internal clamp, but not all parameters perform as specified.

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Characteristic Performance

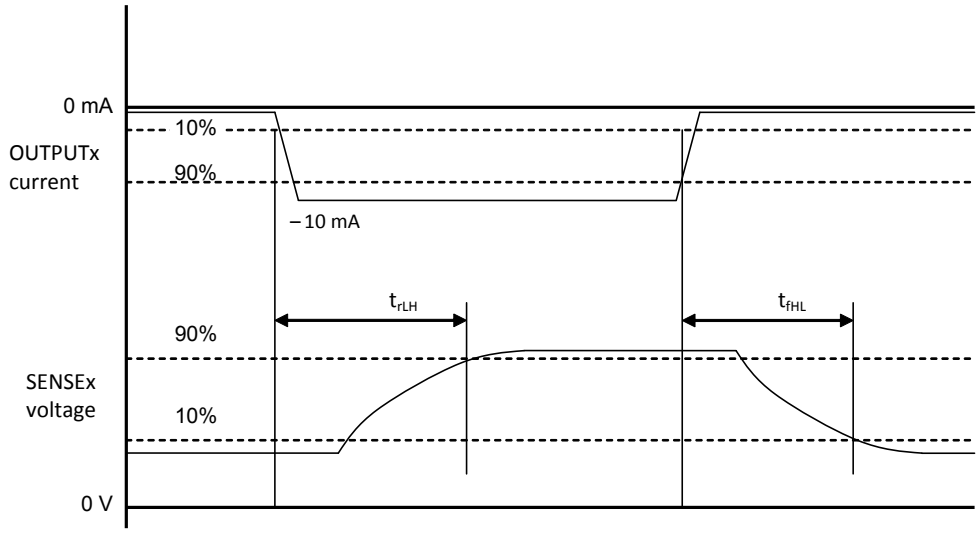

Figure 1. Signal Channel Timing, ENABLE1 = ENABLE1 = High, R_{SENSE} = 1.5 kΩ

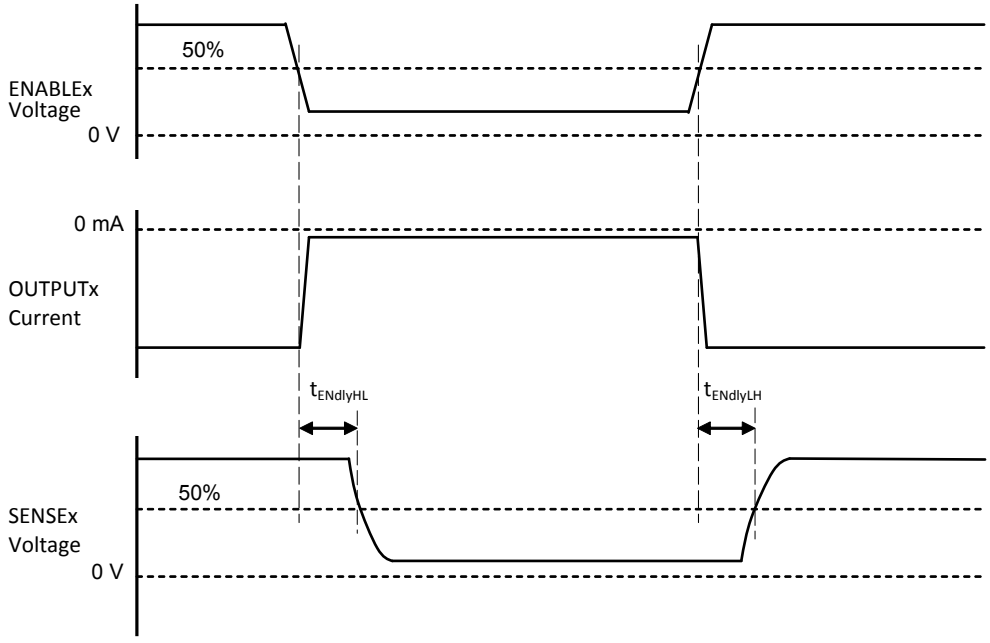

Figure 2. Enable Delays, one ENABLE input held high to prevent the IC going into Sleep mode

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Functional Description

SENSE Pin Outputs

The A6850 divides the OUTPUTx pin current by 10 and mirrors it onto the corresponding SENSEx pin. Putting sense resistors, RSENSE , from these pins to ground will create a voltage that can be read by an ADC (analog-to-digital converter). The value of R_{SENSE} should be chosen so that the voltage drop across the sense resistor (V_{RSENSE}) does not exceed the maximum voltage rating of the ADC. For further protection of the ADC, an external clamping circuit, such as a Zener diode, can be used to clamp any transient current spikes that may occur on the output that would be translated onto the SENSE pins.

The sense current is one tenth of the output current, plus an offset current. This offset current is consistent across the whole range of the output current. The sense current can be calculated by the following formula:

$$I_{SENSEx} = (I_{OUTPUTx} / 10) + I_{SENSE(ofs)} . \quad (1)$$

The sense resistor must also be chosen to meet the voltage limits on the sense pin (see Electrical Characteristics table).

Output Current Limit

The A6850 limits the output current to a maximum current of $I_{OUTPUTM}$. The output current will remain at the current limit until the output load is reduced or the A6850 goes into thermal shutdown.

The high output current limit allows the bypass capacitor, C_{BYP}, on the Hall sensor IC to charge up quickly. This allows a high slew rate on the VCC pin of the Hall sensor IC, ensuring that the sensor IC Power-On State will be correct. See the Applications Information section for schematic diagrams and power calculations.

Output Faults

The A6850 withstands short-to-ground or short-to-battery of the OUTPUTx pins. In the case of short-to-ground, current is held to the current limit ($I_{OUTPUTM}$).

If $V_{OUTPUTx} > (V_{IN} + 0.7\ V)$ during a short-to-battery event, the A6850 monitors $V_{OUTPUTx}$ and disables the outputs. Because the protection circuitry requires a finite amount of time to disable the outputs, a bypass capacitor of 1 µF is necessary on V_{IN}. Although OUTPUTx sinks current into the A6850 in this state, the reverse current is shunted to ground and does not appear on the VIN pin.

Overvoltage Protection

The A6850 has built-in overvoltage protection against a load dump on the supply bus. In the case of a load dump, or when V_{IN} is connected to the battery supply bus and V_{IN} rises above the overvoltage threshold, V_{OVP}, the A6850 will shut off the outputs.

Sleep Mode

Low-leakage or sleep modes are required in automotive applications to minimize battery drain when the vehicle is parked. The A6850 enters sleep mode when both ENABLE pins are low. In sleep mode, the internal regulators and all other internal circuitry are disabled.

When enabling an output, the part must first come out of sleep mode. Consequently, the wake-up time amounts to a propagation delay before the outputs turn on. Also, the ENABLE pins do not switch with hysteresis until the regulators stabilize.

After the internal regulators stabilize, internal circuitry is enabled and the outputs turn on, as shown in figure 3. As long as one ENABLE pin is held high, the A6850 operates with hysteresis.

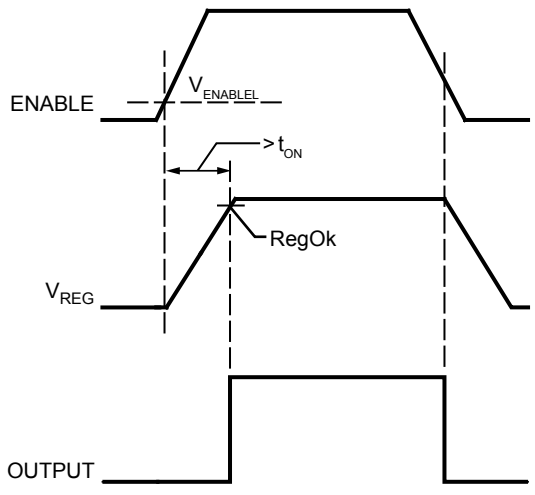

Figure 3. Activation Timing Diagram. Exiting Sleep mode via ENABLE signal to output waveform.

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Signal and Enable delays

When ENABLEx = 1, current signals applied to the OUTPUTx pins will appear scaled and delayed on the SENSEx pins. The transfer characteristic can be considered that of a low pass filter.

The response time definitions are given in figures 1 and 2, in the Characteristic Performance section.

The rise time response is dependent on the effective capacitance loading on the SENSEx pin.

The RC time constant, τ, can be estimated using:

$$\tau = R_{SENSEx} (90 + C_{SENSE}) \quad (2)$$

where R_{SENSEx} is in kΩ and C_{SENSE} is in pF; the result will be in ns.

The 10% to 90% rise time, t_{rLH}, may be estimated from:

$$t_{rLH} = 2.2 \times \tau \quad (3)$$

The small signal low pass filter bandwidth based on a single pole response may be estimated using:

$$BW = 350 / t_{rLH} \quad (4)$$

The result is in MHz when t_{rLH} is in ns.

If the values of t_{rLH} and t_{fHL} are significantly different then a better estimate may be given by:

$$BW = 700 / (t_{rLH} + t_{fHL}) \quad (5)$$

The result is in MHz when t_{rLH} and t_{fHL} are in ns.

Each signal channel may be enabled or disabled individually via their respective ENABLEx pins, as shown in table 1.

Table 1. Enable/Disable Signal Channel Truth Table

EN1	EN2	IOU1	IOU2	SEN1	SEN2
L*	L*	0	0	0	0
H	L	I_1	0	I_1 / 10	0
L	H	0	I_2	0	I_2 / 10
H	H	I_1	I_2	I_1 / 10	I_2 / 10

*Sleep mode

When a capacitor is added in parallel with the signal source connected to an OUTPUTx pin, additional allowance must be made for settling time caused by the inrush current needed to recharge a partially, or fully discharged, capacitor which has decayed during the disabled period.

During this time the current required may reach $I_{OUTPUTM}$, the current limit value for the OUTPUTx pins.

The effects will be most noticeable on a SENSEx pin and will usually cause a signal overshoot as shown as $t_{ENsettle}$ in figure 4.

Thermal Shutdown (TSD)

The A6850 protects itself from excessive heat damage by disabling both outputs when the junction temperature, T_J , rises above the TSD threshold (T_{TSD}). The outputs will remain off until the junction temperature falls below the T_{TSD} level minus the TSD hysteresis, T_{TSDhys}.

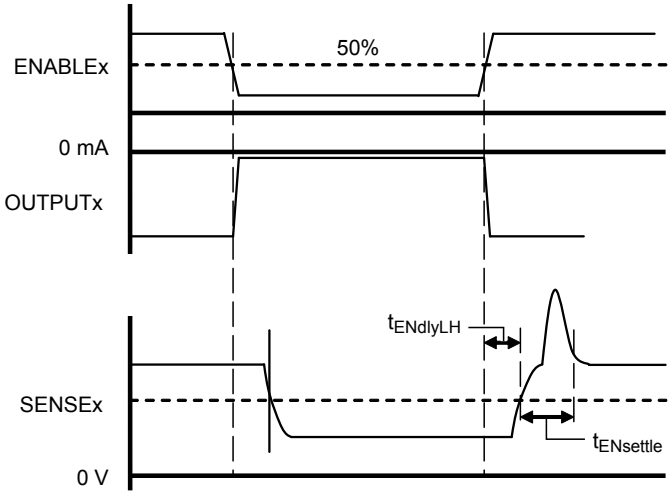

Figure 4. Overshoot resulting from additional capacitance.

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T_J can be estimated by calculating the power dissipation (P_D) of the A6850. To calculate P_D:

$$P_D = V_{IN} I_{INQ} - V_{OUTPUT1} I_{OUTPUT1} - V_{OUTPUT2} I_{OUTPUT2} - V_{SENSE1} I_{SENSE1} - V_{SENSE2} I_{SENSE2} . \quad (6)$$

$$P_D = V_{IN} I_{INQ} + (V_{IN} - V_{OUTPUT1}) I_{OUTPUT1} + (V_{IN} - V_{OUTPUT2}) I_{OUTPUT2} + (V_{IN} - V_{SENSE1}) I_{SENSE1} + (V_{IN} - V_{SENSE2}) I_{SENSE2} . \quad (7)$$

When $I_{OUTPUTx} \times R_{DS(on)}$ < approximately 700 mV, then:

$$(V_{IN} - V_{OUTPUTx}) = I_{OUTPUTx} \times R_{DS(on)} .$$

When $I_{OUTPUTx} \times R_{DS(on)}$ > approximately 700 mV, then:

$$I_{OUTPUTx} = I_{OUTPUT}(\text{max}) ,$$

and $V_{OUTPUTx}$ is set by the loading on the OUTPUTx pin.

The temperature rise of the A6850 can be calculated by multiplying P_D and the thermal resistance from junction to ambient, $R_{\theta JA}$. The formula for temperature rise, ΔT, is:

$$\Delta T = P_D \times R_{\theta JA} . \quad (8)$$

The $R_{\theta JA}$ for an 8-pin SOIC (Allegro L package) on a one-layer board with minimum copper area is 140 °C/W. (More thermal data is available on the Allegro MicroSystems website.)

The total junction temperature can be calculated by:

$$T_J = T_A + \Delta T , \quad (9)$$

where T_A is the ambient air temperature.

Example: Calculating the power dissipation and temperature rise, given:

$T_A = 25°C$,
$V_{IN} = 5$ V ,
$I_{INQ} = 5$ mA ,
$I_{OUTPUT1} = I_{OUTPUT2} = 15$ mA ,
$I_{SENSEx} = I_{OUTPUTx} /10 = 1.5$ mA ,
$R_{SENSE1} = R_{SENSE2} = 2$ kΩ , and
$I_{OUTPUTx} \times R_{DS(on)} = 15 \times 35 = 525$ mV $= V_{IN} - V_{OUTPUTx}$.

Then:

$P_D = 5$ V × 5 mA
+ 0.525 V×15 mA+[5 V – (1.5 mA×2 kΩ)]×1.5 mA
+ 0.525 V×15 mA+[5 V – (1.5 mA×2 kΩ)]×1.5 mA
= 46.75 mW .

Substituting in equation 8:

$$\Delta T = 46.75 \text{ mW} \times 140 \text{ °C/W} = 6.5°C .$$

Substituting in equation 9:

$$T_J = 25°C + 6.5°C = 31.5°C .$$

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Applications Information

Two-Wire Hall IC Interfacing

When voltage is applied to two-wire Hall effect ICs, current flows within one of two narrow ranges. Any current level not within these ranges indicates a fault condition.

The following table describes some of the possible output conditions that can be monitored through the SENSE pins. Figure 5 is a typical application using the A6850 with dual Hall effect ICs.

Signal and Fault Table

Condition	Output Pin Current (mA)	Sense Pin Current (mA)	Sense Pin Voltage, R_{sense}= 1.5 kΩ (V)
OUTPUT Pin Short-to-Ground	25 to 45	2.5 to 4.5	3.75 to 6.75
Logic High from Hall IC	12 to 17	1.2 to 1.7	1.8 to 2.55
Short-to-Battery	0.0	0.0	0
Logic Low from Hall IC*	2 to 6.9	0.2 to 0.69	0.3 to 1.04
Thermal Shutdown	0.0	0.0	0
OUTPUT Pin Open	0.0	0.0	0

*This current range includes all A114x and A118x devices.

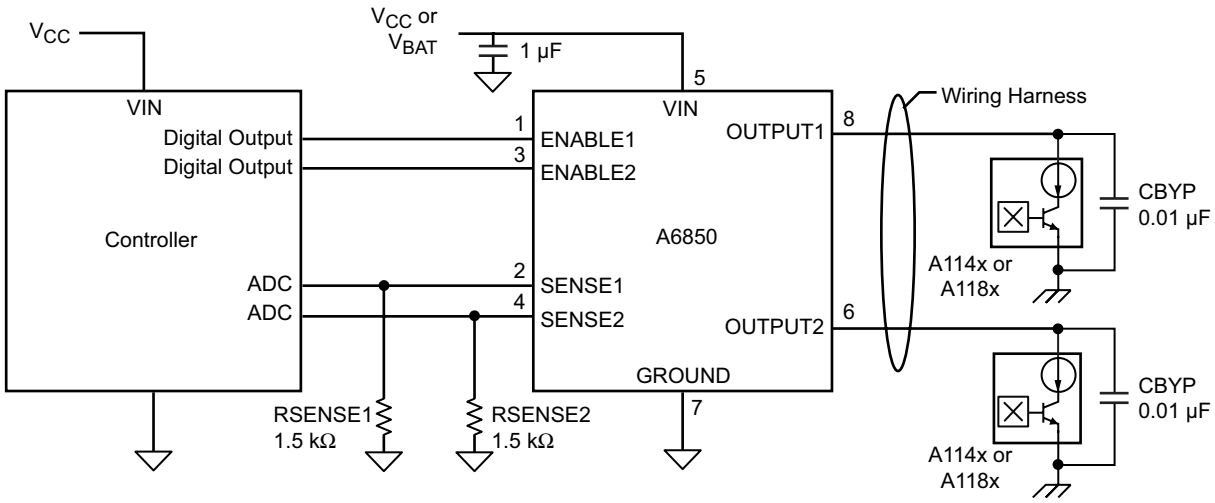

Figure 5. Typical Application with 2-Wire Hall Effect ICs

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Mechanical Switch Interfacing

The A6850 can be used as an interface between mechanical switches, set in a switch-to-ground configuration, and a low voltage microprocessor. A series resistor must be placed in the circuit to limit current when the mechanical switch is closed, in order to prevent excessive power dissipation in the A6850.

For example, to calculate the power dissipation in the A6850 driving two mechanical switches with 1 kΩ series resistors, with V_{IN} = 12 V, assume that the current limit for each of the outputs is set to the maximum value, $I_{OUTPUTM}$(max) = 45 mA.

When the mechanical switch is closed without a series resistor, the A6850 will be at the current limit. The full 12 V of the power supply will drop across the A6850 at 45mA The power dissipation for one mechanical switch closed would be:

$$P_{D1} = V_{Drop1} \times I_{OUTPUT1} \quad (6)$$
$$= 12\ V \times 45\ mA$$
$$= 540\ mW$$

A series resistor included in the circuit reduces power dissipation in the OUTPUTx section of the A6850.

The current is then limited to:

$$I_{OUTPUT1} = V_{IN} / (35 + R_{SERIES}) \quad (7)$$
$$= 12\ V / 1035\ \Omega$$
$$= 11.59\ mA$$

$$V_{Drop1} = 35 \times I_{OUTPUT1} \quad (8)$$
$$= 405.7\ mV$$

The power dissipation in the A6850 from this switch is much lower:

$$P_{D1} = V_{Drop1} \times I_{OUTPUT1} \quad (9)$$
$$= 0.4057\ V \times 11.3\ mA$$
$$= 4.58\ mW$$

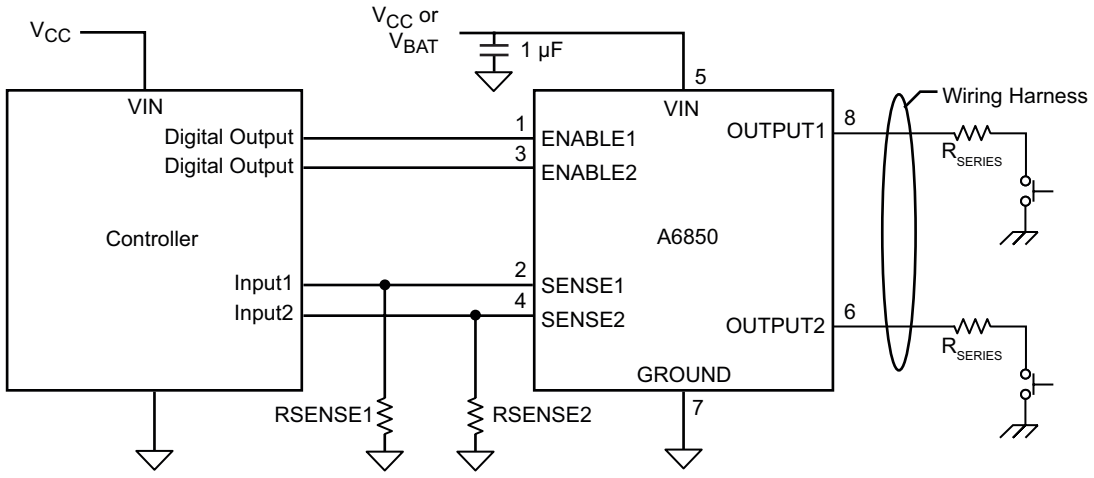

Figure 6. Typical Application with Mechanical Switches

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Ganging SENSE1 and SENSE2

In certain applications both outputs may be read with a single ADC channel. The OUTPUTx loads are enabled by alternatively activating ENABLEx. In fact, both ENABLE1 and ENABLE2 may be activated simultaneously, with the SENSE1 and SENSE2 currents added together. For valid measurements the load resistor need only be selected so that V_{SENSEx} remain within specification.

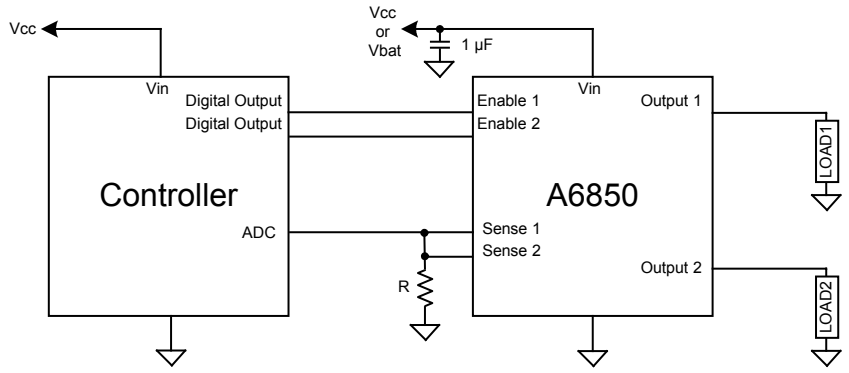

Figure 7. Outline of ganged configuration

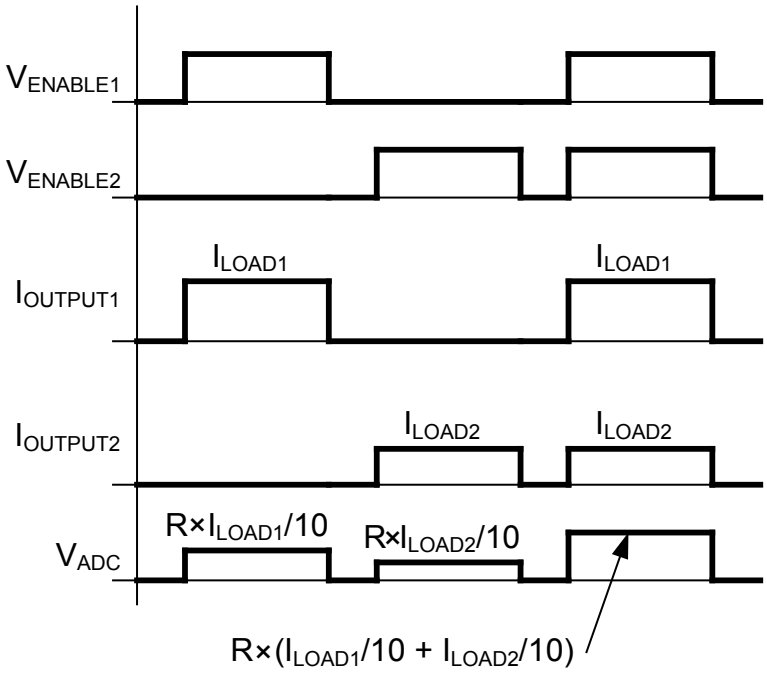

Figure 8. Functional response in ganged configuration

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Protection from EMI

Transients generated by electromagnetic interference (EMI) can disturb operation of the A6850 or add unwanted noise to the signals being processed.

The scheme shown in figure 9 illustrates possible supply decoupling and signal filtering options. The selection of protection and filtering component values will depend on the details of the final application.

The A6850 must be protected with a suitable bypass capacitor to prevent transients entering VIN. The capacitor should be as close to the VIN and GND pins as feasible.

A pi-filter placed between the OUTPUTx pins and the sensor IC has been shown to demonstrate excellent performance in normal automotive Bulk Cable Injection (BCI) testing. However, component selection and layout as well as cable specification and placement must be tailored to the individual application. EMC results should be validated.

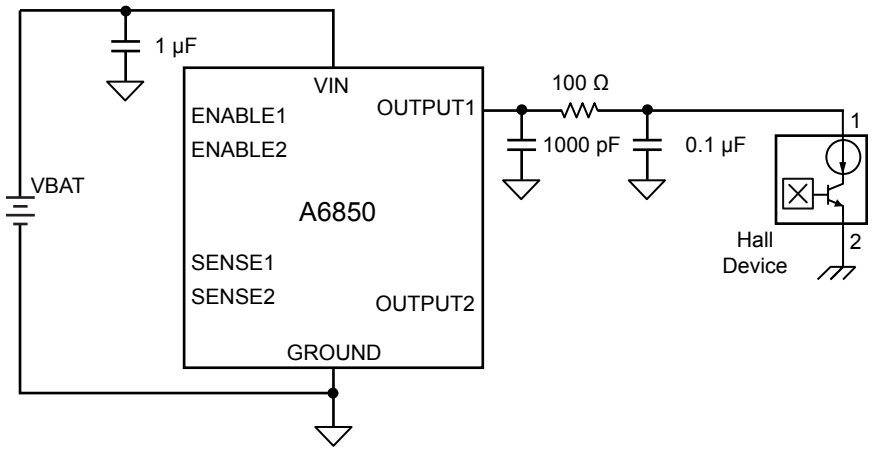

Figure 9. Decoupling and filtering suggestions

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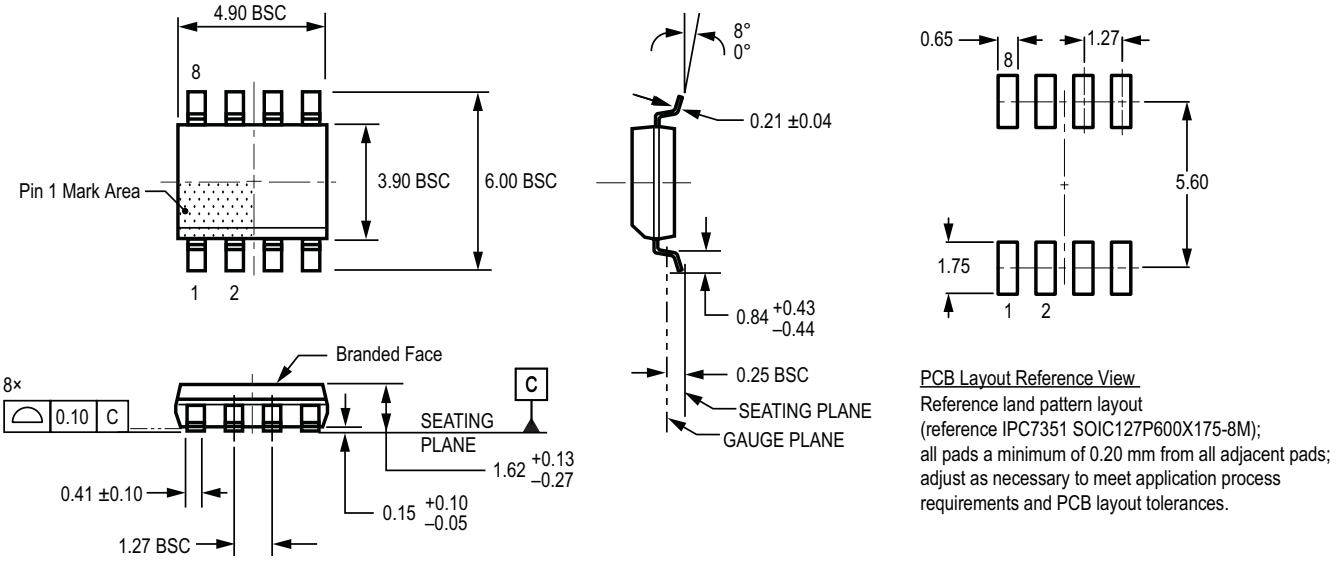
L Package, 8-Pin SOIC

For Reference Only; not for tooling use
(reference Allegro DWG-0000385, Rev. 2 or JEDEC MS-012AA)
Dimensions in millimeters – Not to scale
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



PCB Layout Reference View
Reference land pattern layout
(reference IPC7351 SOIC127P600X175-8M);
all pads a minimum of 0.20 mm from all adjacent pads;
adjust as necessary to meet application process
requirements and PCB layout tolerances.

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Revision Table

Number	Date	Description
6	May 29, 2020	Minor editorial updates
7	June 4, 2021	Updated Package Outline Drawing
8	October 1, 2022	Changed product status: Not for New Design
9	January 31, 2023	Changed product status: removed Not for New Design

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