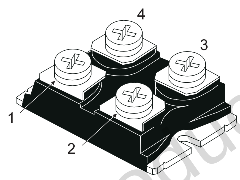
STE30NK90Z

N-channel 900V - 0.21Ω - 28A ISOTOP Zener-Protected SuperMESH™ MOSFET

General features

Type	V_{DSS}	$R_{DS(on)}$	I_D	Pw
STE30NK90Z	900V	<0.26Ω	28A	500W

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized



ISOTOP

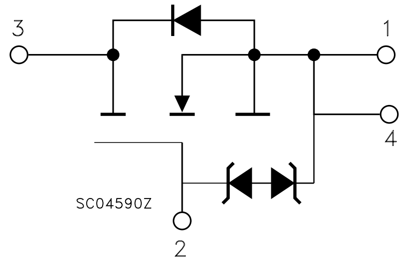
Description

The SuperFREDMesh™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

Applications

- Switching application

Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STE30NK90Z	E30NK90Z	ISOTOP	TUBE

Contents

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	900	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 kΩ)	900	V
V_{GS}	Gate- source voltage	± 30	V
I_D	Drain current (continuous) at T_C = 25°C	28	A
I_D	Drain current (continuous) at T_C = 100°C	18	A
I_{DM} (1)	Drain current (pulsed)	112	A
P_{tot}	Total dissipation at T_C = 25°C	500	W
	Derating Factor	4.3	W/°C
$V_{ESD(G-S)}$	Gate source ESD(HBM-C=100pF, R=1.5KW)	6.5	KV
dv/dt (2)	Peak diode recovery voltage slope	4.5	V/ns
V_{ISO}	Insulation withstand voltage (AC-RMS) from all four terminals to external heatsink	2500	V
T_{stg}	Storage temperature	-65 to 150	°C
T_j	Max. operating junction temperature		

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 28A$, di/dt ≤200A/µs, $V_{DD} \leq V_{(BR)DSS}$,

Table 2. Thermal data

Rthj-case	Thermal resistance junction-case max	0.23	°C/W
Rthj-amb	Thermal resistance junction-ambient max	40	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j Max)	13	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 35 V)	500	mJ

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	900			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating, T_C = 125 °C			10 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20V			±100	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 150 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10V, I_D = 14 A		0.21	0.26	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 15 V, I_D = 14 A		26		S
C_{iss} C_{oss} C_{rss}	Input capacitance output capacitance reverse transfer capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		12000 852 166		pF pF pF
$C_{oss\ eq.}$ (2)	Equivalent output capacitance	V_{GS} = 0V, V_{DS} = 0V to 720 V		377		pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time rise time turn-off delay time fall time	V_{DD} = 450 V, I_D = 13 A R_G = 4.7Ω V_{GS} = 10 V (see *Figure 14*)		67 59 250 72		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge gate-source charge gate-drain charge	V_{DD} = 720 V, I_D = 26 A, V_{GS} = 10V (see *Figure 15*)		350 51 190	490	nC nC nC

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %
2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}(1)	Source-drain current Source-drain current (pulsed)				28 112	A A
V_{SD}(2)	Forward on voltage	I_{SD} = 28 A, V_{GS} = 0			2	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 26 A, di/dt = 100 A/µs V_{DD} = 100 V, T_j = 25°C (see Figure 16)		1 18.9 36.6		µs µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 26 A, di/dt = 100 A/µs V_{DD} = 100 V, T_j = 150°C (see Figure 16)		1.33 25.2 37.8		µs µC A

1. Pulse width limited by safe operating area%
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5

Table 7. Gate-source zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-source breakdown voltage	Igs=± 1mA (Open Drain)	30			V

2.1 Protection features of gate-to-source zener diodes

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.2 Electrical characteristics (curves)

Figure 1. Safe operating area

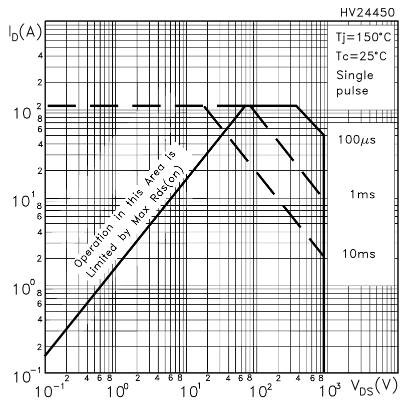


Figure 2. Thermal impedance

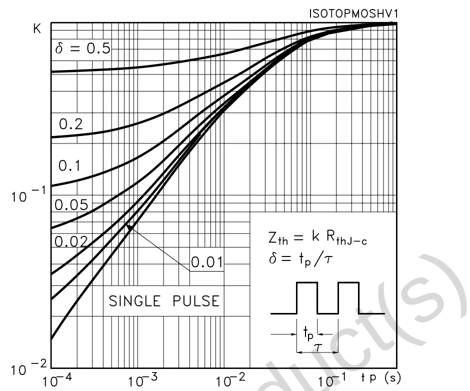


Figure 3. Output characterisics

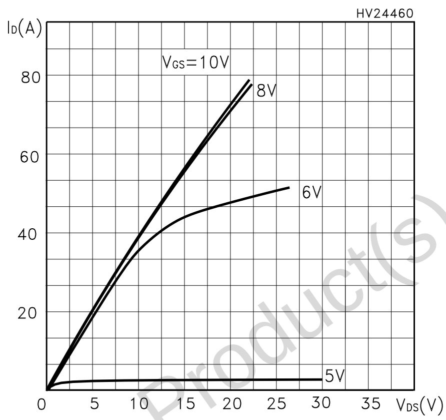


Figure 4. Transfer characteristics

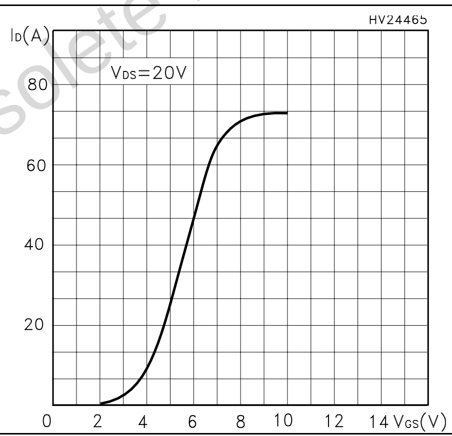


Figure 5. Transconductance

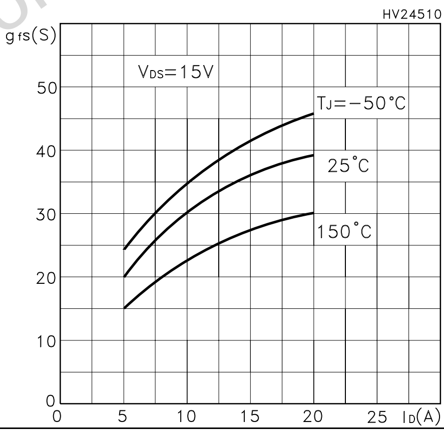


Figure 6. Static drain-source on resistance

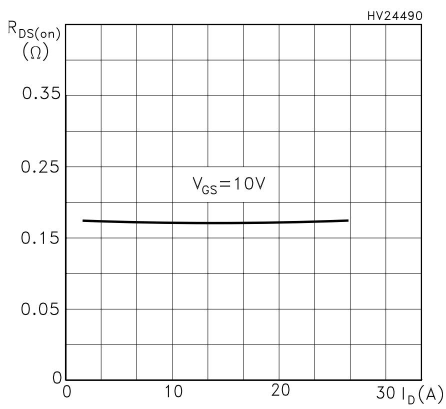


Figure 7. Gate charge vs gate-source voltage

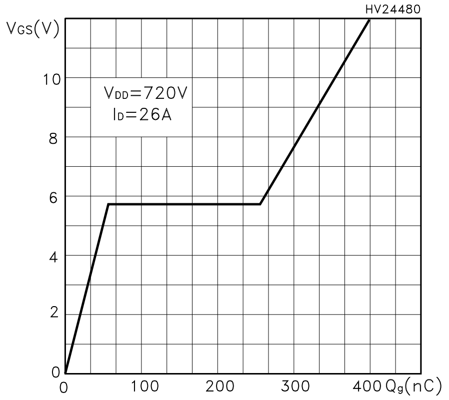


Figure 8. Capacitance variations

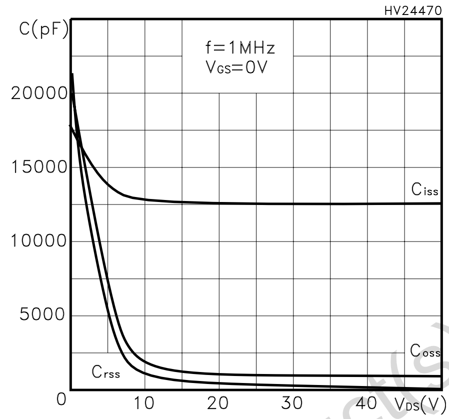


Figure 9. Normalized gate threshold voltage vs temperature

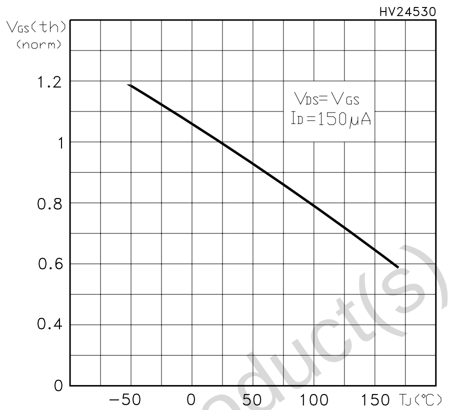


Figure 10. Normalized on resistance vs temperature

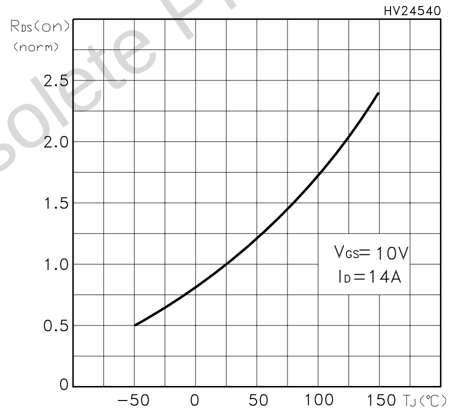


Figure 11. Source-drain diode forward characteristics

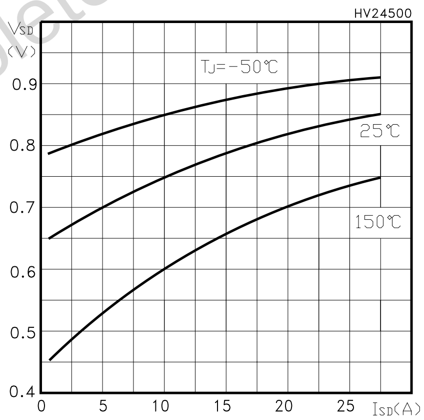


Figure 12. Normalized B_{VDSS} vs temperature

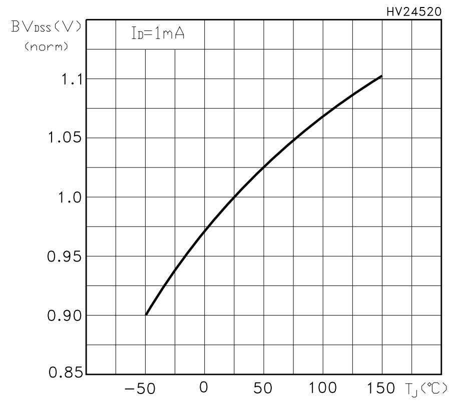
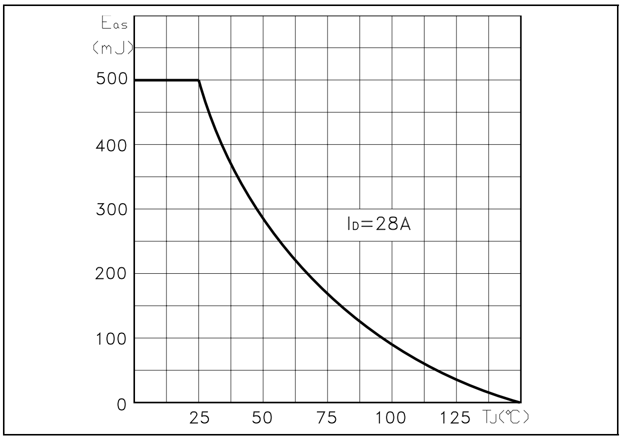


Figure 13. Avalanche energy vs starting Tj



3 Test circuit

Figure 14. Switching times test circuit for resistive load

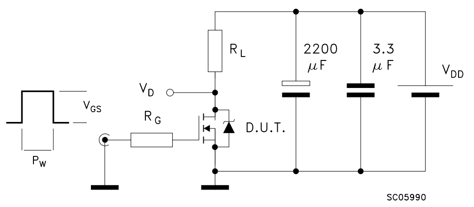


Figure 15. Gate charge test circuit

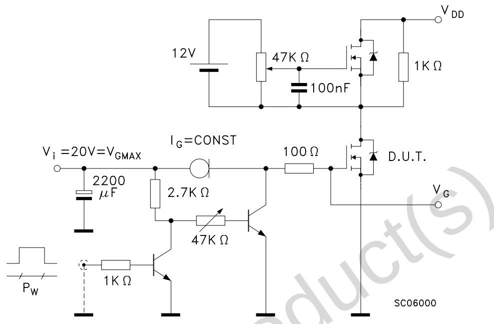


Figure 16. Test circuit for inductive load switching and diode recovery times

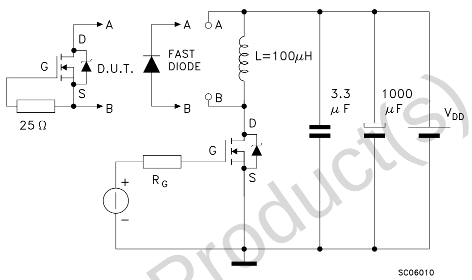


Figure 17. Unclamped Inductive load test circuit

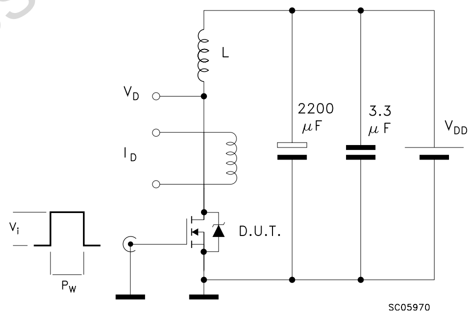


Figure 18. Unclamped inductive waveform

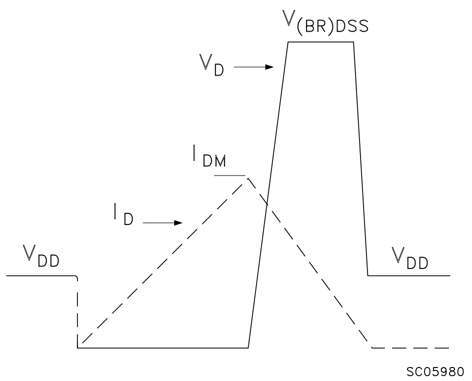
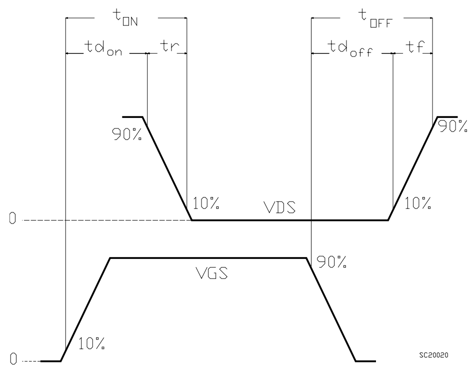


Figure 19. Switching time waveform

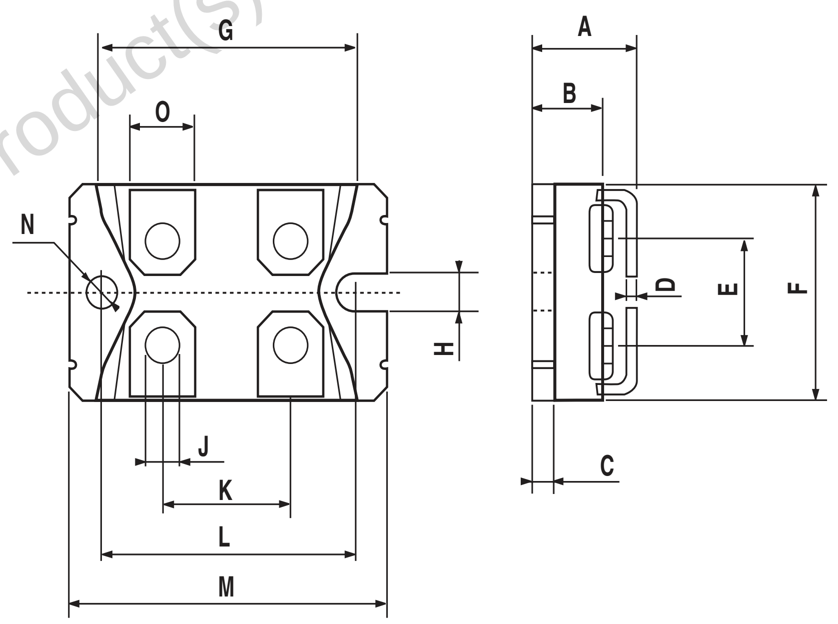


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

ISOTOP MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	11.8		12.2	0.466		0.480
B	8.9		9.1	0.350		0.358
C	1.95		2.05	0.076		0.080
D	0.75		0.85	0.029		0.033
E	12.6		12.8	0.496		0.503
F	25.15		25.5	0.990		1.003
G	31.5		31.7	1.240		1.248
H	4			0.157		
J	4.1		4.3	0.161		0.169
K	14.9		15.1	0.586		0.594
L	30.1		30.3	1.185		1.193
M	37.8		38.2	1.488		1.503
N	4			0.157		
O	7.8		8.2	0.307		0.322



5 Revision history

Table 8. Revision history

Date	Revision	Changes
24-May-2005	1	First Release
10-Jun-2005	2	Inserted new row in *Table 6.: Switching times*
28-Sep-2005	3	Complete version
14-Oct-2005	4	Modified *Figure 3*, *Figure 6*
12-Jul-2006	5	New template, no content change