



T-52-30-13

# 74FCT544A Octal Registered Transceiver

## General Description

The 74FCT544A octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow. The 74FCT544A inverts data in both directions.

FACT™ FCTA utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

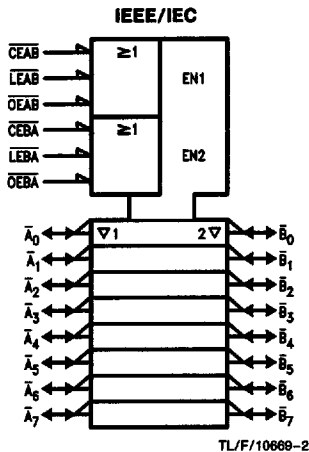
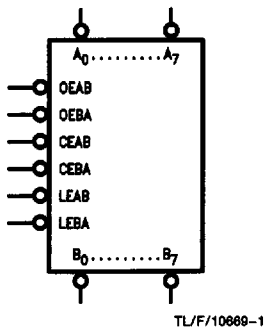
FACT FCTA features undershoot correction and split ground bus for superior performance.

## Features

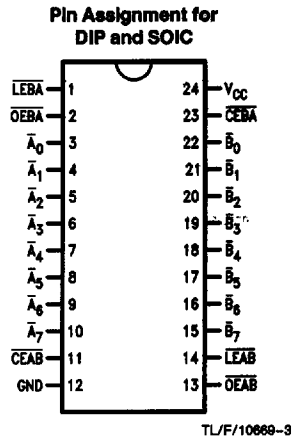
- NSC 74FCT544A is pin and functionally equivalent to IDT 74FCT544A
- Back to back registers for storage separate controls for data flow in each direction
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- $I_{OL} = 64$  mA
- CMOS power levels
- 4 kV minimum ESD immunity

**Ordering Code:** See Section 8

## Logic Symbols



## Connection Diagram



Pin Names	Description
OEAB	A-to-B Output Enable Input (Active LOW)
OEBA	B-to-A Output Enable Input (Active LOW)
CEAB	A-to-B Enable Input (Active LOW)
CEBA	B-to-A Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input (Active LOW)
LEBA	B-to-A Latch Enable Input (Active LOW)
$\bar{A}_0 - \bar{A}_7$	A-to-B Data Inputs or B-to-A TRI-STATE® Outputs
$\bar{B}_0 - \bar{B}_7$	B-to-A Data Inputs or A-to-B TRI-STATE Outputs

### Functional Description

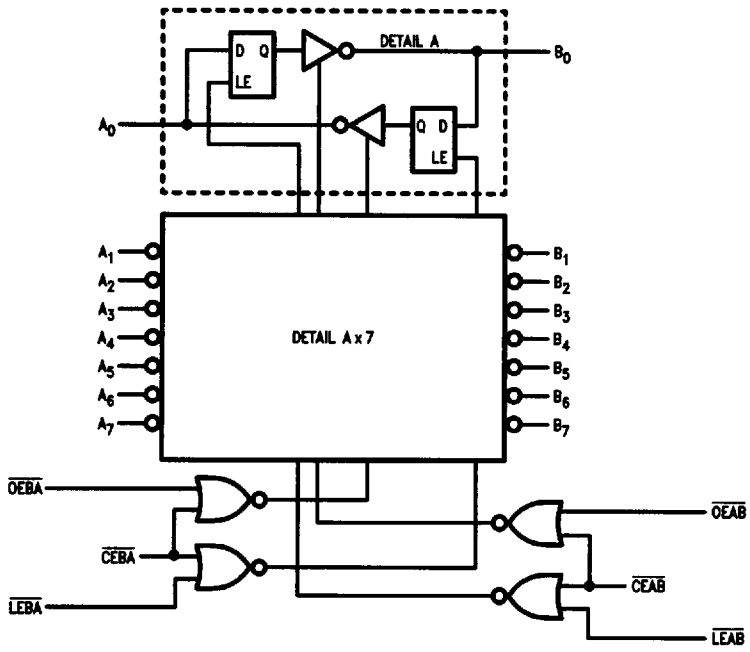
The 74CT544A contains two sets of eight D-type latches, with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ( $\overline{CEAB}$ ) input must be LOW in order to enter data from  $\overline{A_0}$ - $\overline{A_7}$  or take data from  $\overline{B_0}$ - $\overline{B_7}$ , as indicated in the Data I/O Control Table. With  $\overline{CEAB}$  LOW, a LOW signal on the A-to-B Latch Enable ( $\overline{LEAB}$ ) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the  $\overline{LEAB}$  signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With  $\overline{CEAB}$  and  $\overline{OEAB}$  both LOW, the TRI-STATE B output buffers are active and reflect the data present at the output of the A latches. Control of data flow from B to A is similar, but using the  $\overline{CEBA}$ ,  $\overline{LEBA}$  and  $\overline{OEBA}$  outputs.

Data I/O Control Table

Input			Latch Status	Output Buffers
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$		
H	X	X	Latched	High-Z
X	H	X	Latched	High-Z
L	L	X	Transparent	High-Z
X	X	H		High-Z Driving
L	X	L		High-Z Driving

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 A-to-B data flow shown; B-to-A flow control is the same, except using  $\overline{CEBA}$ ,  $\overline{LEBA}$  and  $\overline{OEBA}$ .

### Logic Diagram



TL/F/10669-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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### Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND ( $V_{TERM}$ )	
74FCTA	-0.5V to +7.0V
Temperature under Bias ( $T_{BIAS}$ )	
74FCTA	-55°C to +125°C
Storage Temperature ( $T_{STG}$ )	
74FCTA	-55°C to +125°C
DC Output Current ( $I_{OUT}$ )	120 mA

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Exposure to absolute maximum rating conditions for extended periods may affect reliability. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

### Recommended Operating Conditions

Supply Voltage ( $V_{CC}$ )	4.75V to 5.25V
74FCTA	
Input Voltage	0V to $V_{CC}$
Output Voltage	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	0°C to +70°C
74FCTA	
Junction Temperature ( $T_J$ )	
PDIP	140°C

Note: All commercial is not recommended for applications requiring greater than 2000 temperature cycles from -40°C to +125°C.

### DC Characteristics for 'FCTA Family Devices

Typical values are at  $V_{CC} = 5.0V$ , +25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC} = 5.0V \pm 5\%$ ,  $T_A = 0^\circ C$  to +70°C;  $V_{HC} = V_{CC} - 0.2V$ .

Symbol	Parameter	74FCTA			Units	Conditions	
		Min	Typ	Max			
$V_{IH}$	Minimum High Level Input Voltage	2.0			V		
$V_{IL}$	Maximum Low Level Input Voltage			0.8	V		
$I_{IH}$	Input High Current (Except I/O Pins)			5.0 5.0	$\mu A$	$V_{CC} = \text{Max}$	$V_I = V_{CC}$ $V_I = 2.7V$ (Note 2)
$I_{IL}$	Input Low Current (Except I/O Pins)			-5.0 -5.0	$\mu A$	$V_{CC} = \text{Max}$	$V_I = 0.5V$ (Note 2) $V_I = \text{GND}$
$I_{IH}$	Input High Currents (I/O Pins)			15 15	$\mu A$	$V_{CC} = \text{Max}$	$V_I = V_{CC}$ $V_I = 2.7V$ (Note 2)
$I_{IL}$	Input Low Currents (I/O Pins)			-15 -15	$\mu A$	$V_{CC} = \text{Max}$	$V_I = 0.5V$ (Note 2) $V_I = \text{GND}$
$V_{IK}$	Clamp Diode Voltage		-0.7	-1.2	V	$V_{CC} = \text{Min}; I_N = -18 \text{ mA}$	
$I_{OS}$	Short Circuit Current	-60	-120		mA	$V_{CC} = \text{Max}$ (Note 1); $V_O = \text{GND}$	
$V_{OH}$	Minimum High Level Output Voltage	2.8 $V_{HC}$ 2.4	3.0 $V_{CC}$ 4.3		V	$V_{CC} = 3V; V_{IN} = 0.2V$ or $V_{HC}; I_{OH} = -32 \mu A$	$I_{OH} = -300 \mu A$ $I_{OH} = -15 \text{ mA}$
$V_{OL}$	Maximum Low Level Output Voltage		GND GND 0.3	0.2 0.2 0.55	V	$V_{CC} = 3V; V_{IN} = 0.2V$ or $V_{HC}; I_{OL} = 300 \mu A$	$I_{OL} = 300 \mu A$ $I_{OL} = 64 \text{ mA}$
$I_{CC}$	Maximum Quiescent Supply Current		0.001	1.5	mA	$V_{CC} = \text{Max}$ $V_{IN} \geq V_{HC}, V_{IN} \leq 0.2V$ $f_i = 0$	
$\Delta I_{CC}$	Quiescent Supply Current; TTL Inputs HIGH		0.5	2.0	mA	$V_{CC} = \text{Max}$ $V_{IN} = 3.4V$ (Note 3)	

**DC Characteristics for 'FCTA Family Devices** (Continued)

Typical values are at  $V_{CC} = 5.0V$ ,  $+25^{\circ}C$  ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC} = 5.0V \pm 5\%$ ,  $T_A = 0^{\circ}C$  to  $+70^{\circ}C$ ;  $V_{HC} = V_{CC} - 0.2V$ .

Symbol	Parameter	74FCTA			Units	Conditions	
		Min	Typ	Max			
$I_{CCD}$	Dynamic Power Supply Current (Note 4)		0.25	0.3	mA/MHz	$V_{CC} = \text{Max}$ Outputs Open $\overline{CEAB} + \overline{OEAB} = \text{GND}$ $\overline{CEBA} = V_{CC}$ One Input Toggling 50% Duty Cycle $V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$	
$I_C$	Total Power Supply Current (Note 6)		1.5	4.0		mA	$V_{CC} = \text{Max}$ Outputs Open $f_{CP} = 10 \text{ MHz}$ 50% Duty Cycle $\overline{CEAB} + \overline{OEAB} = \text{GND}$ $\overline{CEBA} = V_{CC}$ $f_{CP} = \overline{LEAB} = 10 \text{ MHz}$ One Bit Toggling at $f_1 = 5 \text{ MHz}$ 50% Duty Cycle $V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			1.8	6.0	$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$		
			3.0	16.5	(Note 5) $V_{CC} = \text{Max}$ Outputs Open $f_{CP} = 10 \text{ MHz}$ 50% Duty Cycle $\overline{CEAB} + \overline{OEAB} = \text{GND}$ $\overline{CEBA} = V_{CC}$ $f_{CP} = \overline{LEAB} = 10 \text{ MHz}$ Eight Bits Toggling at $f_1 = 5 \text{ MHz}$ 50% Duty Cycle $V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$		
			5.0	21.75	$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$		

**Note 1:** Maximum test duration not to exceed one second, not more than one output shorted at one time.

**Note 2:** This parameter guaranteed but not tested.

**Note 3:** Per TTL driven input ( $V_{IN} = 3.4$ ); all other inputs at  $V_{CC}$  or GND.

**Note 4:** This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

**Note 5:** Values for these conditions are examples of the  $I_{CC}$  formula. These limits are guaranteed but not tested.

**Note 6:**  $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_1 N_1)$$

$I_{CC}$  = Quiescent Current

$\Delta I_{CC}$  = Power Supply Current for a TTL High Input ( $V_{IN} = 3.4V$ )

$D_H$  = Duty Cycle for TTL Inputs High

$N_T$  = Number of Inputs at  $D_H$

$I_{CCD}$  = Dynamic Current caused by an Input Transition Pair (HLH or LHL)

$f_{CP}$  = Clock Frequency for Register Devices (Zero for Non-Register Devices)

$f_1$  = Input Frequency

$N_1$  = Number of Inputs at  $f_1$

All currents are in milliamperes and all frequencies are in megahertz.

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**AC Electrical Characteristics:** See Section 2 for Waveforms

Symbol	Parameter	74FCTA		74FCTA		Units	Fig. No.
		$T_A = +25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		$T_A, V_{CC} = \text{Com}$ $R_L = 500\Omega$ $C_L = 50\text{pF}$			
		Typ	Min (Note)	Max			
$t_{PLH}$ $t_{PHL}$	Propagation Delay Transparent Mode $A_n$ to $B_n$ or $B_n$ to $A_n$	3.0	1.5	7.0		ns	2-8
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\overline{LEBA}$ to $A_n$ $\overline{LEAB}$ to $B_n$	3.5	1.5	8.0		ns	2-8
$t_{PZH}$ $t_{PZL}$	Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to $A_n$ or $B_n$ $\overline{CEAB}$ or $\overline{CEBA}$ to $A_n$ or $B_n$	4.5	1.5	9		ns	2-11
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time $\overline{CEBA}$ or $\overline{OEAB}$ to $A_n$ or $B_n$ $\overline{CEBA}$ or $\overline{OEAB}$ to $A_n$ or $B_n$	4.0	1.5	7.5		ns	2-11
$t_{SU}$	Setup Time High or Low $A_n$ or $B_n$ to $\overline{LEBA}$ or $\overline{LEAB}$	1.0	2			ns	2-10
$t_H$	Hold Time High or Low $A_n$ or $B_n$ to $\overline{LEBA}$ or $\overline{LEAB}$	1.0	2			ns	2-10

Note: Minimum propagation delays are guaranteed but not tested.

**Capacitance**  $T_A = +25^\circ\text{C}, f = 1.0\text{ MHz}$

Symbol	Parameter (Note)	Typ	Max	Units	Conditions
$C_{IN}$	Input Capacitance	6	10	pF	$V_{IN} = 0\text{V}$
$C_{OUT}$	Output Capacitance	8	12	pF	$V_{OUT} = 0\text{V}$

Note: This parameter is measured at characterization but not tested.