features

- Regulated 3.3-V Output Voltage From a 1.8-V to 3.6-V Input Voltage Range
- UltraLow Operating Current in Snooze Mode, Typical 2 μA
- Less Than 5-mV$_{(PP)}$ Output Voltage Ripple Achieved With Push-Pull Topology
- Integrated Low-Battery and Power-Good Detector
- Switching Frequency Can Be Synchronized to External Clock Signal
- Extends Battery Usage With up to 90% Efficiency and 35-μA Quiescent Current
- Easy-To-Design, Low Cost, Low EMI Power Supply Since No Inductors Are Used
- Compact Converter Solution in UltraSmall 10-Pin MSOP With Only Four External Capacitors Required
- Evaluation Module Available (TPS60210EVM-167)

applications

- Replaces DC/DC Converters With Inductors in Battery-Powered Applications Like:
  - Two Battery Cells to 3.3-V Conversion
  - MSP430 Ultralow-Power Microcontroller and Other Battery Powered Microprocessor Systems
  - Glucose Meters and Other Medical Instruments
  - MP3 Portable Audio Players
  - Backup-Battery Boost Converters
  - Cordless Phones, PDAs

description

The TPS6021x step-up, regulated charge pumps generate a 3.3-V ±4% output voltage from a 1.8-V to 3.6-V input voltage. These devices are typically powered by two alkaline, NiCd, or NiMH battery cells or by one primary lithium MnO2 (or similar) coin cell and operate down to a minimum supply voltage of 1.6 V. Continuous output current is a minimum of 100 mA for the TPS60210 and TPS60211, and 50 mA for the TPS60212 and TPS60213, all from a 2-V input.

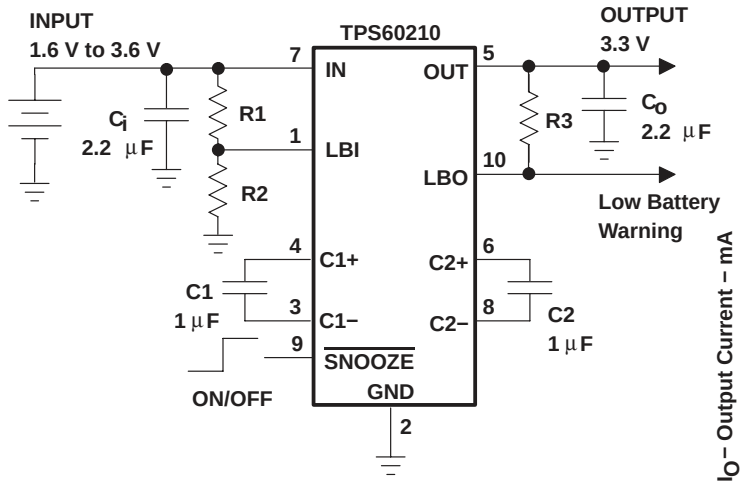
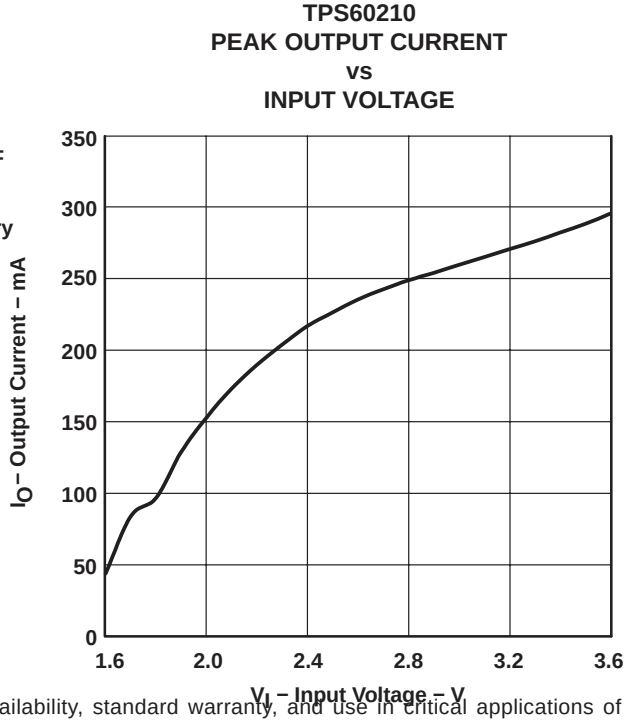


Figure 1. Typical Application Circuit With Low-Battery Warning



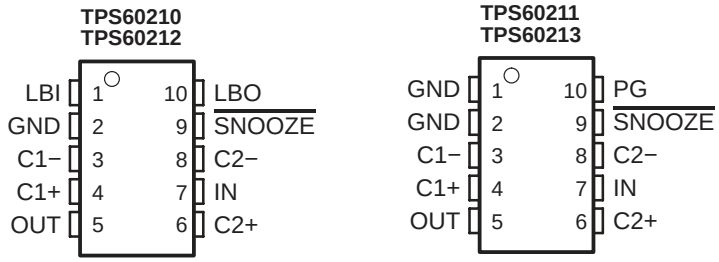
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

description (continued)

Three operating modes can be programmed using the $\overline{\text{SNOOZE}}$ pin. When $\overline{\text{SNOOZE}}$ is low, the device is put into snooze mode. In snooze mode, the device operates with a typical quiescent current of 2 μA while the output voltage is maintained at 3.3 V ±6%. This is lower than the self-discharge current of most batteries. Load current in snooze mode is limited to 2 mA. When $\overline{\text{SNOOZE}}$ is high, the device is put into normal operating mode. During normal operating mode, the device operates in the newly developed linskip mode where it switches seamlessly from the power saving pulse-skip mode at light loads to the low-noise constant-frequency linear-regulation mode once the output current exceeds the linskip current threshold of about 7 mA. In this mode, the device operates from the internal oscillator. The device is synchronized to an external clock signal if $\overline{\text{SNOOZE}}$ is clocked; thus switching harmonics can be controlled and minimized.

Only four external capacitors are needed to build a complete low-ripple dc/dc converter. The push-pull operating mode of two single-ended charge pumps assures the low output voltage ripple as charge is continuously transferred to the output. All the devices can start with full load current. The devices include a low-battery detector that issues a warning if the battery voltage drops below a user-defined threshold voltage or a power-good detector that goes active when the output voltage reaches about 90% of its nominal value. This dc/dc converter requires no inductors; therefore, EMI of the system is reduced to a minimum, making it easier to use in designs. It is available in the small 10-pin MSOP package (DGS).

DGS PACKAGES



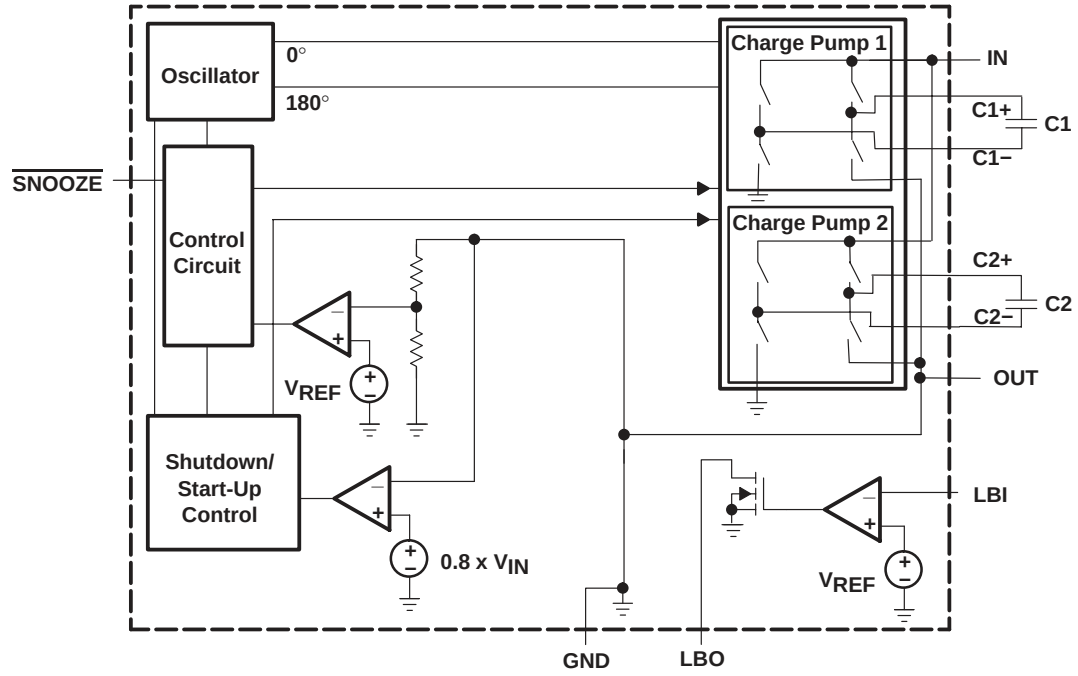
AVAILABLE OPTIONS

T_A	PART NUMBER†	MARKING DGS PACKAGE	OUTPUT CURRENT (mA)	OUTPUT VOLTAGE (V)	DEVICE FEATURES
−40°C to 85°C	TPS60210DGS	AFD	100	3.3	Low-battery detector
	TPS60211DGS	AFE	100	3.3	Power-good detector
	TPS60212DGS	AFF	50	3.3	Low-battery detector
	TPS60213DGS	AFG	50	3.3	Power-good detector

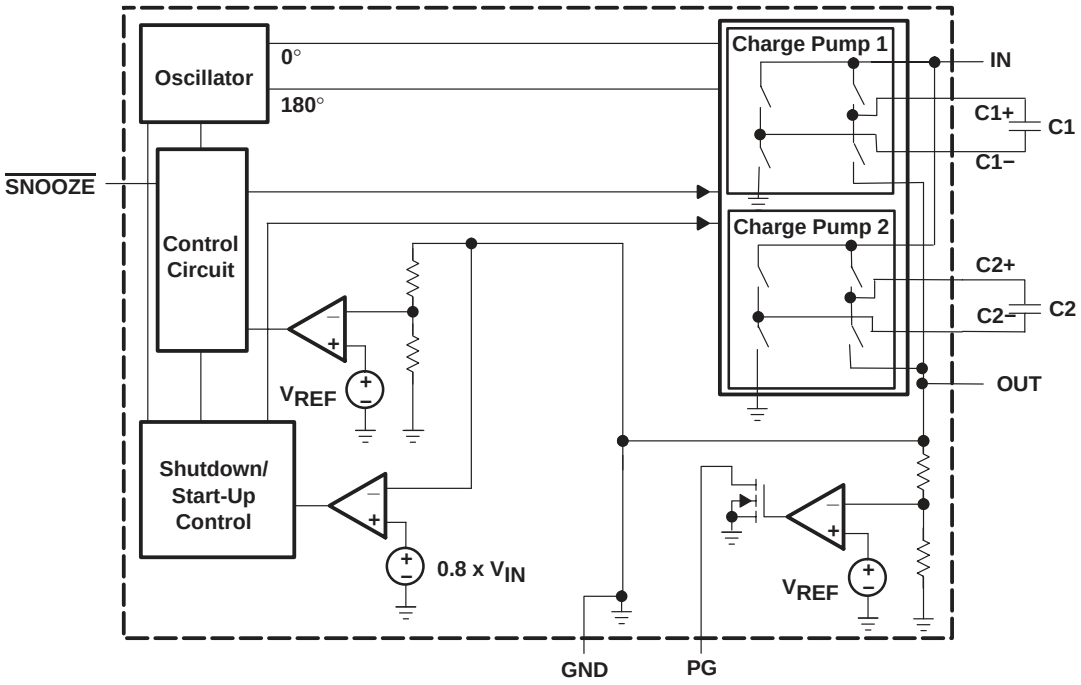
† The DGS package is available taped and reeled. Add R suffix to device type (e.g., TPS60210DGSR) to order quantities of 3000 devices per reel.

functional block diagrams

TPS60210 and TPS60212 with low-battery detector



TPS60211 and TPS60213 with power-good detector



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
C1+	4		Positive terminal of the flying capacitor C1
C1−	3		Negative terminal of the flying capacitor C1
C2+	6		Positive terminal of the flying capacitor C2
C2−	8		Negative terminal of the flying capacitor C2
GND	2		Ground
IN	7	I	Supply input. Bypass IN to GND with a capacitor of a minimum of 2.2 μF.
LBI/GND	1	I	Low-battery detector input for TPS60210 and TPS60212. A low-battery warning is generated at the LBO pin when the voltage on LBI drops below the threshold of 1.18 V. Connect LBI to GND or VBAT if the low-battery detector function is not used. For the devices TPS60211 and TPS60213, this pin is a ground (GND pin).
LBO/PG	10	O	Open-drain low-battery detector output for TPS60210 and TPS60212. This pin is pulled low if the voltage on LBI drops below the threshold of 1.18 V. A pullup resistor should be connected between LBO and OUT or any other logic supply rail that is lower than 3.6 V. Open-drain power-good detector output for TPS60211 and TPS60213. As soon as the voltage on OUT reaches about 90% of its nominal value, this pin goes active high. A pullup resistor should be connected between PG and OUT or any other logic supply rail that is lower than 3.6 V.
OUT	5	O	Regulated 3.3-V power output. Bypass OUT to GND with the output filter capacitor C_O.
$\overline{\text{SNOOZE}}$	9	I	Three operating modes can be programmed with the $\overline{\text{SNOOZE}}$ pin. − $\overline{\text{SNOOZE}}$ = Low programs the device in the snooze mode, enabling ultralow operating current while still maintaining the output voltage to within 3.3 V ±6%. − $\overline{\text{SNOOZE}}$ = High programs the device into normal operation mode where it runs from the internal oscillator. − If an external clock signal is applied to the $\overline{\text{SNOOZE}}$ pin, the charge pump operates synchronized to the frequency of the external clock signal.

detailed description

operating principle

The TPS6021x charge pumps provide a regulated 3.3-V output from a 1.8-V to 3.6-V input. They deliver a minimum 100-mA load current while maintaining the output at 3.3 V ±4%. Designed specifically for space critical battery-powered applications, the complete converter requires only four external capacitors. The device is using the push-pull topology to achieve the lowest output voltage ripple. The converter is also optimized for a very small board space. It makes use of small-sized capacitors, with the highest output current rating per output capacitance.

The TPS6021x circuits consist of an oscillator, a voltage reference, an internal resistive feedback circuit, an error amplifier, two charge-pump power stages with high-current MOSFET switches, a shutdown/start-up circuit, and a control circuit (see functional block diagrams).

push-pull operating mode

The two single-ended charge-pump power stages operate in the push-pull operating mode (i.e., they operate with a 180°C phase shift). Each single-ended charge pump transfers a charge into its flying capacitor (C1 or C2) in one-half of the period. During the other half of the period (transfer phase), the flying capacitor is placed in series with the input to transfer its charge to the load and output capacitor (C_O). While one single-ended charge pump is in the charge phase, the other one is in the transfer phase. This operation ensures that there is a continuous flow of charge to the load, hence the output capacitor no longer needs to buffer the load current for half of the switching cycle, avoiding the high, inherent output voltage ripple of conventional charge pumps.

In order to provide a regulated output voltage of 3.3 V, the TPS6021x devices operate either in constant-frequency linear-regulation control mode or in pulse-skip mode. The mode is automatically selected based on the output current. If the load current is low, the controller switches into the power-saving pulse-skip mode to boost efficiency at low output power.

detailed description (continued)

constant-frequency mode

When the output current is higher than the linskip current threshold, the charge pump runs continuously at the switching frequency f_{OSC}. The control circuit, fed from the error amplifier, controls the charge on C1 and C2 by regulating the $r_{DS(on)}$ of the integrated MOSFET switches. When the output voltage decreases, the $r_{DS(on)}$ decreases as well, resulting in a larger voltage across the flying capacitors C1 and C2. This regulation scheme minimizes output ripple.

Since the device switches continuously, the output ripple contains well-defined frequency components, and the circuit requires smaller external capacitors for a given output ripple. However, constant-frequency mode, due to higher operating current, is less efficient at light loads. For this reason, the device switches seamlessly into the pulse-skip mode when the output current drops below the linskip current threshold.

pulse-skip mode

The device enters the pulse-skip mode when the load current drops below the linskip current threshold of about 7 mA. In pulse-skip mode, the controller disables switching of the power stages when it detects an output voltage higher than 3.3 V. It skips switching cycles until the output voltage drops below 3.3 V. Then the controller reactivates the oscillator and switching of the power stages starts again. A 30-mV output voltage offset is introduced in this mode.

The pulse-skip regulation mode minimizes operating current because it does not switch continuously and deactivates all functions except the voltage reference and error amplifier when the output is higher than 3.3 V. Even in pulse-skip mode the $r_{DS(ON)}$ of the MOSFETs is controlled. This way the energy per switching cycle that is transferred by the charge pump from the input to the output is limited to the minimum that is necessary to sustain a regulated output voltage, with the benefit that the output ripple is kept to a minimum. When switching is disabled in pulse-skip mode, the load is isolated from the input.

start up, snooze mode, short circuit protection

During start-up (i.e., when voltage is applied to the supply pin IN) the input is connected to the output until the output voltage reaches 0.8 x V_I. When the start-up comparator detects this limit, the actual charge pump output stages are activated to boost the voltage higher than the input voltage. This precharging of the output current with a limited current ensures a short start-up time and avoids high inrush currents into an empty output capacitor.

Driving $\overline{\text{SNOOZE}}$ low, programs the device into the snooze mode. In this mode, the converter will still maintain the output voltage at 3.3 V ±6%. The operating current in snooze mode, is however, drastically reduced to a typical value of 2 µA, while the output current is limited to a maximum of 2 mA. If the load current increases above 2 mA, the controller recognizes a further drop of the output voltage and the device enters the start-up mode to bring the voltage up to its nominal value again. However, it does not switch into the normal operating mode. The device limits short circuit currents to typically 60 mA.

synchronization to an external clock signal

The operating frequency of the charge pump is limited to 400 kHz in order to avoid troublesome interference problems in the sensitive 455-kHz IF band. The device can either run from the integrated oscillator, or an external clock signal can be used to drive the charge pump. The maximum frequency of the external clock signal is 800 kHz. The switching frequency used internally to drive the charge pump power stages is half of the external clock frequency. The external clock signal is applied to the $\overline{\text{SNOOZE}}$-pin. The device will switch into the snooze mode if the signal on $\overline{\text{SNOOZE}}$ is held low for more than 10 µs.

When the load current drops below the linskip current threshold, the device enters the pulse-skip mode but stays synchronized to the external clock signal.

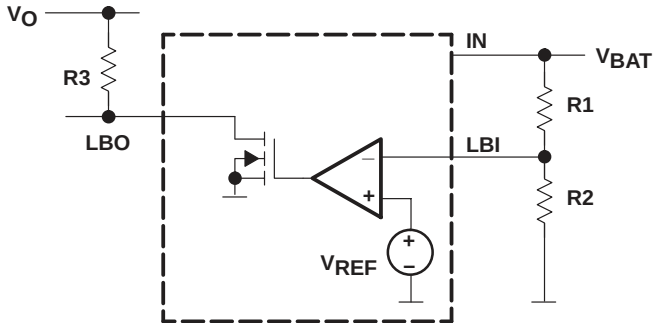
detailed description (continued)

low-battery detector (TPS60210 and TPS60212)

The low-battery comparator trips at 1.18 V ±5% when the voltage on pin LBI ramps down. The voltage $V_{(TRIP)}$ at which the low-battery warning is issued can be adjusted with a resistive divider as shown in Figure 2. The sum of resistors R1 and R2 is recommended to be in the 100-kΩ to 1-MΩ range.

LBO is an open drain output. An external pullup resistor to OUT, or any other voltage rail in the appropriate range, in the 100-kΩ to 1-MΩ range is recommended. During start-up, the LBO output signal is invalid for the first 500 μs. LBO is high impedance when the device is programmed into snooze mode.

If the low battery function is not used, connect LBI to ground and leave LBO unconnected. When the device is programmed into snooze mode ($\overline{SNOOZE}$ = LOW), the low-battery detector is disabled.



$$V_{(TRIP)} = 1.18\ V \left(1 + \frac{R1}{R2}\right)$$

Figure 2. Programming of the Low-Battery Comparator Trip Voltage

A 100-nF ceramic capacitor should be connected in parallel to R2 if large line transients are expected. These voltage drops may inadvertently trigger the low-battery comparator and produce a wrong low-battery warning signal at the LBO pin.

Formulas to calculate the resistive divider for low-battery detection, with V_{LBI} = 1.13 V to 1.23 V and the sum of resistors R1 and R2 equal 1 MΩ:

$$R2 = 1\ M\Omega \times \frac{V_{LBI}}{V_{Bat}} \quad (1)$$

$$R1 = 1\ M\Omega - R2 \quad (2)$$

Formulas to calculate the minimum and maximum battery voltage:

$$V_{Bat(min)} = V_{LBI(min)} \times \frac{R1_{(min)} + R2_{(max)}}{R2_{(max)}} \quad (3)$$

$$V_{Bat(max)} = V_{LBI(max)} \times \frac{R1_{(max)} + R2_{(min)}}{R2_{(min)}} \quad (4)$$

detailed description (continued)

Table 1. Recommended Values for the Resistive Divider From the E96 Series (±1%)

V_{IN}/V	R1/kΩ	R2/kΩ	$V_{TRIP(MIN)}$/V	$V_{TRIP(MAX)}$/V
1.6	267	750	1.524	1.677
1.7	301	681	1.620	1.785
1.8	340	649	1.710	1.887
1.9	374	619	1.799	1.988
2.0	402	576	1.903	2.106

power-good detector (TPS60211 and TPS60213)

The power-good output is an open-drain output that pulls low when the output is out of regulation. When the output rises above 91% of its nominal voltage, the power-good output is released. When the device is programmed into snooze mode ($\overline{\text{SNOOZE}}$ = LOW), the power-good detector is disabled and PG is high impedance. In normal operation, an external pullup resistor must be connected between PG and OUT, or any other voltage rail in the appropriate range. The pullup resistor should be in the 100-kΩ to 1-MΩ range. If the PG output is not used, it should remain unconnected.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range: IN, OUT, SNOOZE, LBI, LBO, PG to GND . . . . . −0.3 V to 3.6 V
C1+, C2+ to GND . . . . . −0.3 V to (V_O + 0.3 V)
C1−, C2− to GND . . . . . −0.3 V to (V_I + 0.3 V)
Continuous total power dissipation . . . . . See Dissipation Rating Table
Continuous output current: TPS60210, TPS60211 . . . . . 150 mA
TPS60212, TPS60213 . . . . . 75 mA
Storage temperature range, T_{stg} . . . . . −55°C to 150°C
Maximum junction temperature, T_J . . . . . 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE 1 FREE-AIR TEMPERATURE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DGS	424 mW	3.4 mW/°C	178 mW	136 mW

The thermal resistance junction to ambient of the DGS package is R_{TH-JA} = 294°C/W.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Input voltage range, V_I	1.6		3.6	V
Input capacitor, C_i		2.2		µF
Flying capacitors, C1, C2		1		µF
Output capacitor, C_O		2.2		µF
Operating junction temperature, T_J	−40		125	°C

electrical characteristics at C_i= 2.2 μF, C1 = C2 = 1 μF, C_o = 2.2 μF, T_A = −40°C to 85°C, V_I = 2.4 V, $\overline{SNOOZE}$ = V_I (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{O(MAX)}$	Maximum continuous output current	TPS60210 and TPS60211, V_I = 2 V	100			mA
		TPS60212 and TPS60213, V_I = 2 V	50			mA
V_O	Output voltage	1.6 V < V_I < 1.8 V, 0 < I_O < 0.25 × $I_{O(MAX)}$	3			V
		1.8 V < V_I < 2 V, 0 < I_O < 0.5 × $I_{O(MAX)}$	3.17	3.3	3.43	V
		2 V < V_I < 3.3 V, 0 < I_O < $I_{O(MAX)}$	3.17	3.3	3.43	V
		3.3 V < V_I < 3.6 V, 0 < I_O < $I_{O(MAX)}$	3.17	3.3	3.47	V
	Output voltage in snooze mode	$\overline{SNOOZE}$ = GND, 1.8 V < V_I < 3.6 V, I_O < 2 mA	3.1	3.3	3.47	V
V_{PP}	Output voltage ripple	I_O = $I_{O(MAX)}$		5		mV_{PP}
$I_{(Q)}$	Quiescent current (no-load input current)	I_O = 0 mA, V_I = 1.8 V to 3.6 V		35	70	μA
	Quiescent current in snooze mode	$\overline{SNOOZE}$ = GND, I_O = 0 mA		2	5	μA
$f_{(OSC)}$	Internal switching frequency		200	300	400	kHz
$f_{(SYNC)}$	External clock signal frequency		400	600	800	kHz
	External clock signal duty cycle		30%		70%	
V_{IL}	$\overline{SNOOZE}$ input low voltage	V_I = 1.6 V to 3.6 V			0.3 × V_I	V
V_{IH}	$\overline{SNOOZE}$ input high voltage	V_I = 1.6 V to 3.6 V	0.7 × V_I			V
I_{lkg}	$\overline{SNOOZE}$ input leakage current	$\overline{SNOOZE}$ = GND or V_I		0.01	0.1	μA
	LinSkip current threshold	V_I = 2 V to 3 V		7		mA
	Output load regulation	V_I = 2.4 V, 1 mA < I_O < $I_{O(MAX)}$, T_C = 25°C		0.015		%/mA
		V_I = 2.4 V, 10 mA < I_O < $I_{O(MAX)}$, T_C = 25°C		0.008		
	Output line regulation	2 V < V_I < 3.3 V, I_O = 0.5 x $I_{O(MAX)}$, T_A = 25°C		0.28		%V
$I_{(SC)}$	Short circuit current	V_I = 2.4 V, V_O = 0 V		60		mA

electrical characteristics for low-battery comparator of devices TPS60210 and TPS60212 at T_A = −40°C to 85°C, V_I = 2.4 V and $\overline{SNOOZE}$ = V_I (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(LBI)}$	LBI trip voltage	V_I = 1.6 V to 2.2 V, T_c = 0°C to 70°C	1.13	1.18	1.23	V
	LBI trip voltage hysteresis	For rising voltage at LBI		10		mV
$I_{I(LBI)}$	LBI input current	$V_{(LBI)}$ = 1.3 V		20	100	nA
$V_{O(LBO)}$	LBO output voltage low	$V_{(LBI)}$ = 0 V, $I_{(LBO)}$ = 1 mA			0.4	V
$I_{lkg(LBO)}$	LBO leakage current	$V_{(LBI)}$ = 1.3 V, $V_{(LBO)}$ = 3.3 V		0.01	0.1	μA

NOTE: During start-up of the converter the LBO output signal is invalid for the first 500 μs.

electrical characteristics for power-good comparator of devices TPS60211 and TPS60213 at T_A = −40°C to 85°C, V_I = 2.4 V and $\overline{SNOOZE}$ = V_I (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(PG)}$	Power-good trip voltage	T_c = 0°C to 70°C	0.87 × V_O	0.91 × V_O	0.95 × V_O	V
$V_{hys(PG)}$	Power-good trip voltage hysteresis	V_O decreasing, T_c = 0°C to 70°C		1%		
$V_{O(PG)}$	Power-good output voltage low	V_O = 0 V, $I_{(PG)}$ = 1 mA			0.4	V
$I_{lkg(PG)}$	Power-good leakage current	V_O = 3.3 V, $V_{(PG)}$ = 3.3 V		0.01	0.1	μA

NOTE: During start-up of the converter the PG output signal is invalid for the first 500 μs.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURES
η	Efficiency	vs Output current (TPS60210 and TPS60212)	3, 4
		vs Input voltage	5
I_O	Output current	vs Input voltage	6
V_O	Output voltage	vs Output current (TPS60210 and TPS60212)	7, 8
		vs Input voltage (TPS60210 and TPS60212)	9, 10
I_Q	Quiescent supply current	vs Input voltage	11
		vs Output current in snooze mode	12
V_O	Output voltage	vs Time (Exit from snooze mode)	13
V_O	Output voltage ripple	vs Time	14, 15, 16
		vs Time in snooze mode	17, 18
	Load transient response		19
	Line transient response		20

NOTE: All typical characteristics were measured using the typical application circuit of Figure 21 (unless otherwise noted).

TPS60210
EFFICIENCY
vs
OUTPUT CURRENT

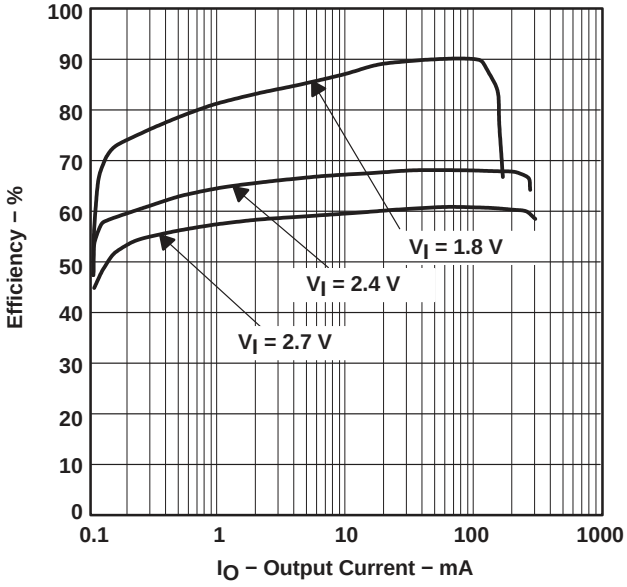


Figure 3

TPS60212
EFFICIENCY
vs
OUTPUT CURRENT

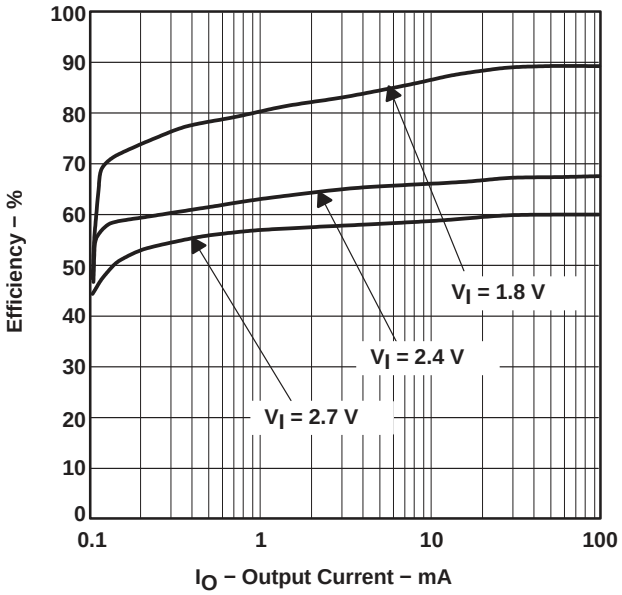


Figure 4

TYPICAL CHARACTERISTICS

TPS60210
EFFICIENCY
vs
INPUT VOLTAGE

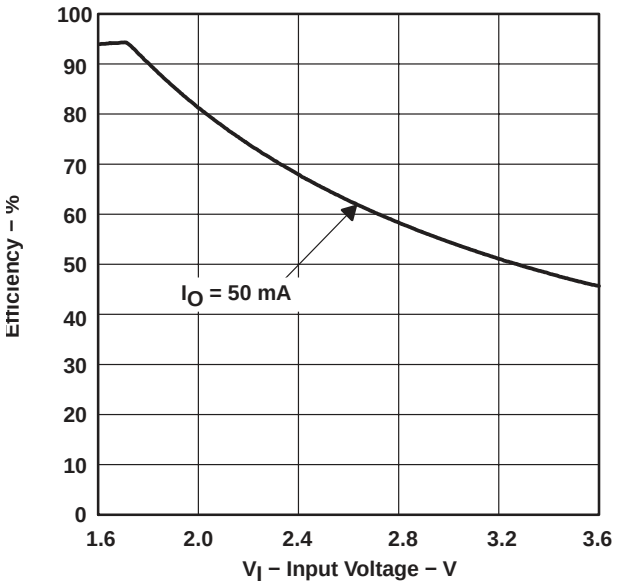


Figure 5

TPS60210
PEAK OUTPUT CURRENT
vs
INPUT VOLTAGE

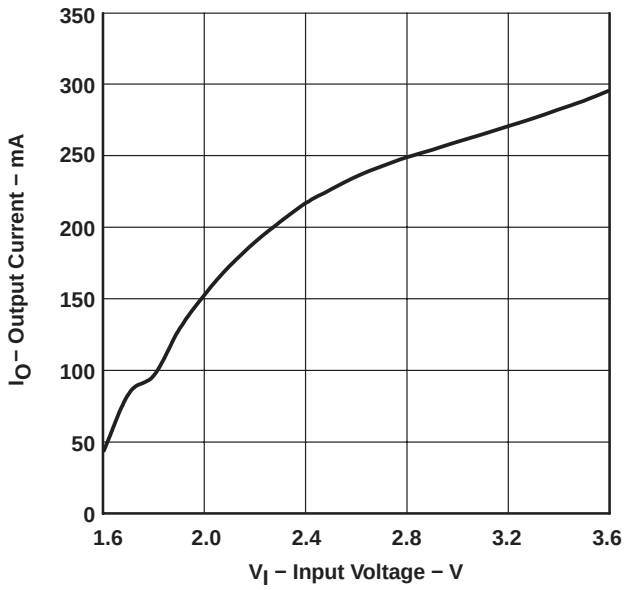


Figure 6

TPS60210
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

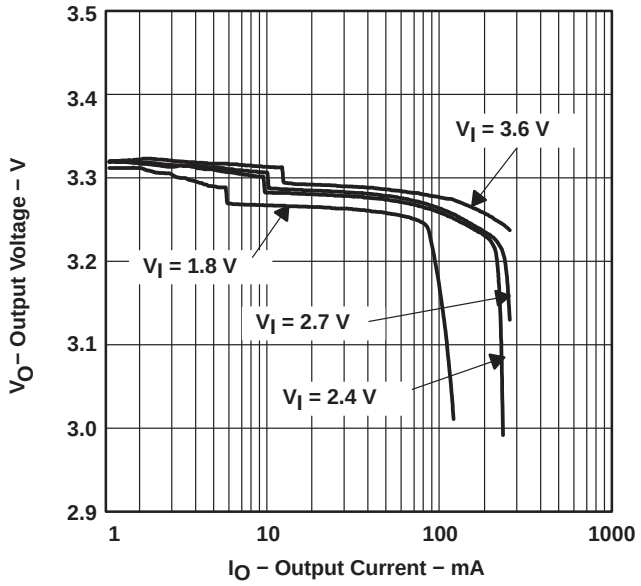


Figure 7

TPS60212
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

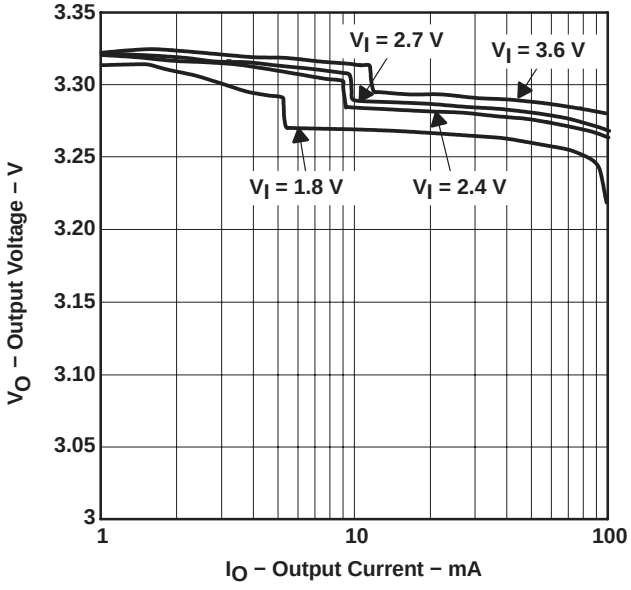


Figure 8

TYPICAL CHARACTERISTICS

TPS60210
OUTPUT VOLTAGE
vs
INPUT VOLTAGE

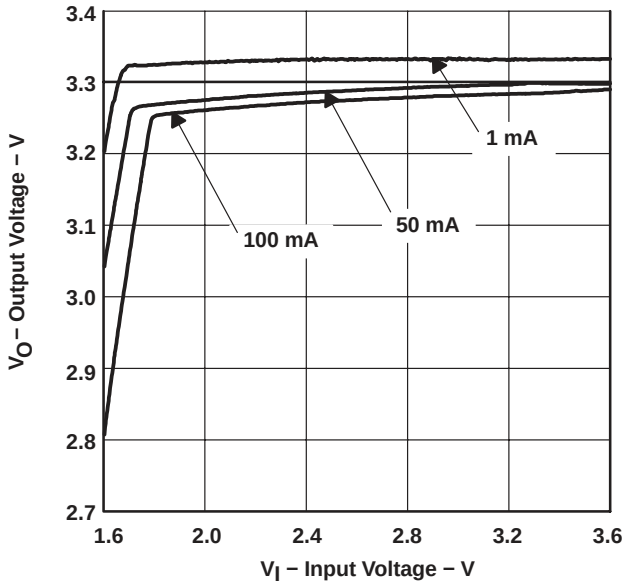


Figure 9

TPS60212
OUTPUT VOLTAGE
vs
INPUT VOLTAGE

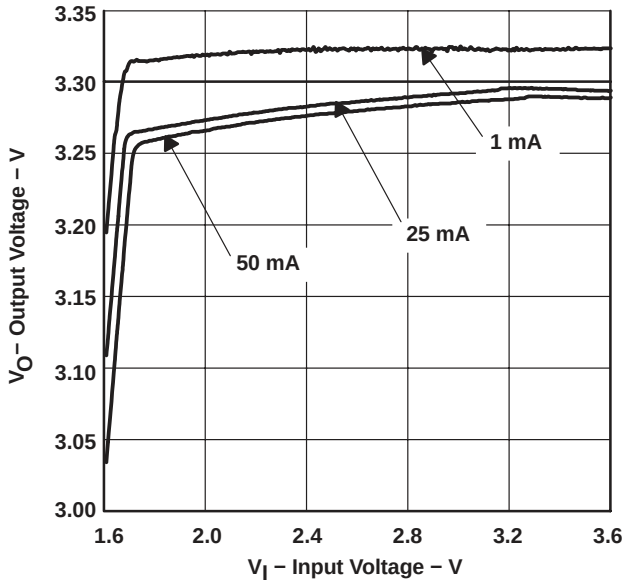


Figure 10

QUIESCENT SUPPLY CURRENT
vs
INPUT VOLTAGE

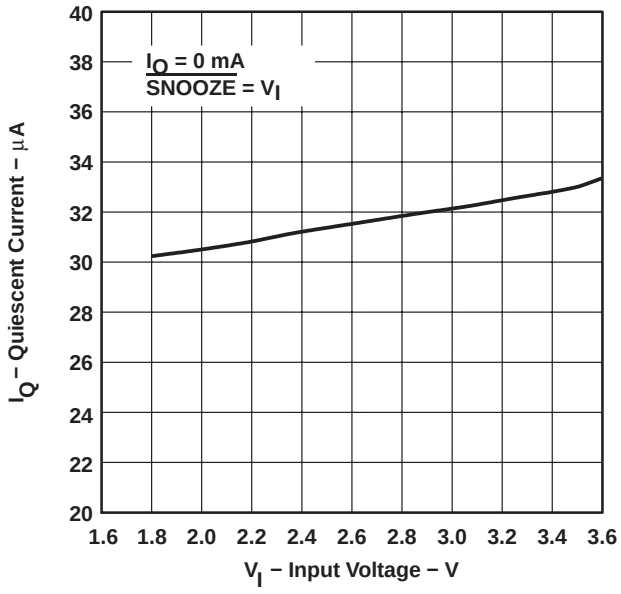


Figure 11

QUIESCENT SUPPLY CURRENT
vs
OUTPUT CURRENT IN SNOOZE MODE

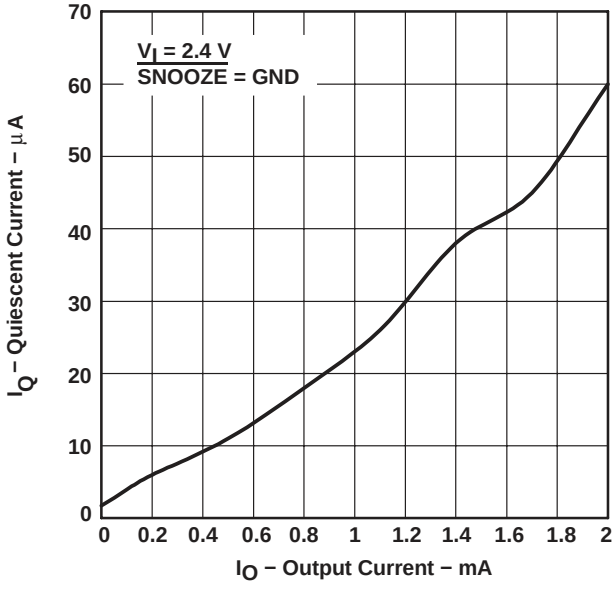


Figure 12

TYPICAL CHARACTERISTICS

TPS60210
OUTPUT VOLTAGE
vs
TIME

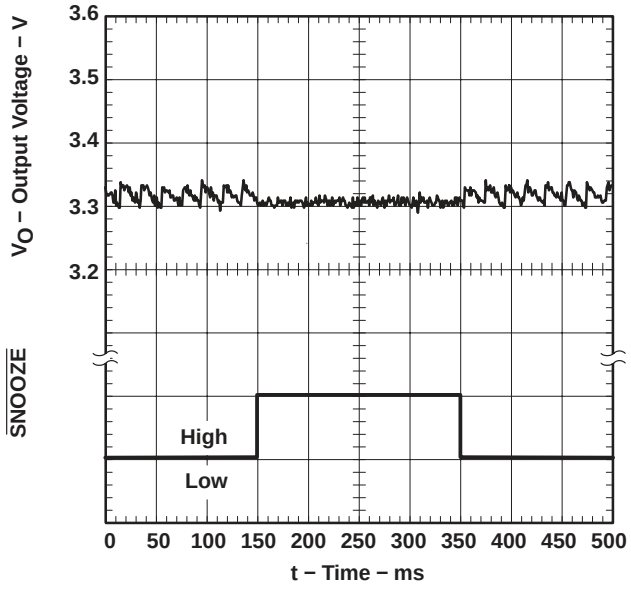


Figure 13

TPS60210
OUTPUT VOLTAGE RIPPLE
vs
TIME

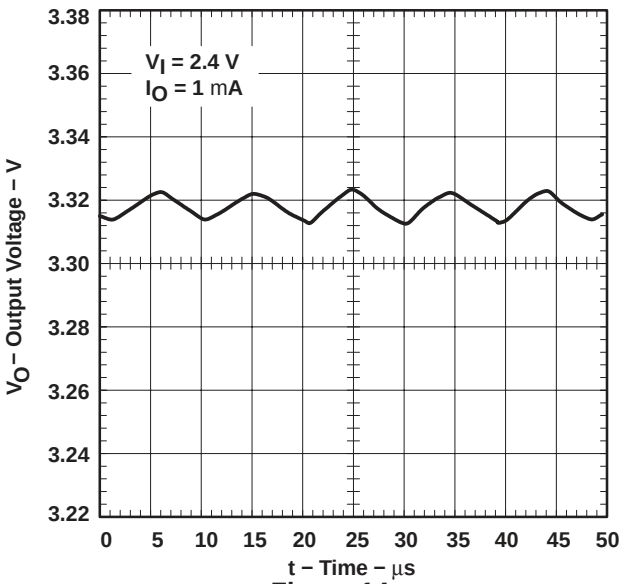


Figure 14

TPS60210
OUTPUT VOLTAGE RIPPLE
vs
TIME

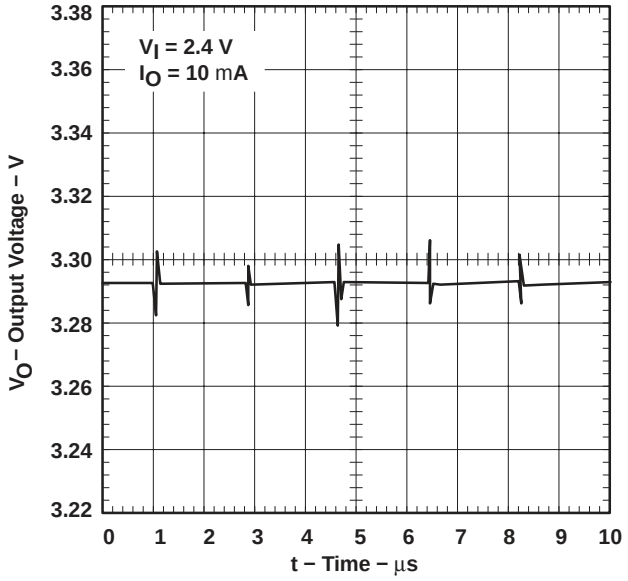


Figure 15

TPS60210
OUTPUT VOLTAGE RIPPLE
vs
TIME

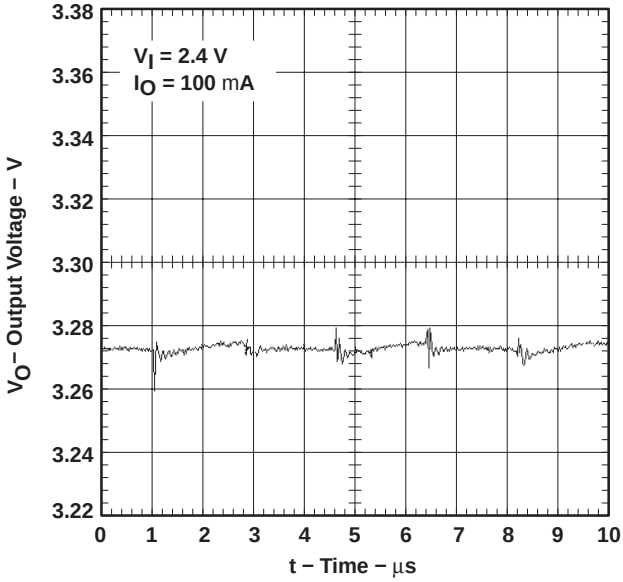


Figure 16

TYPICAL CHARACTERISTICS

TPS60210
OUTPUT VOLTAGE RIPPLE IN SNOOZE MODE
vs
TIME

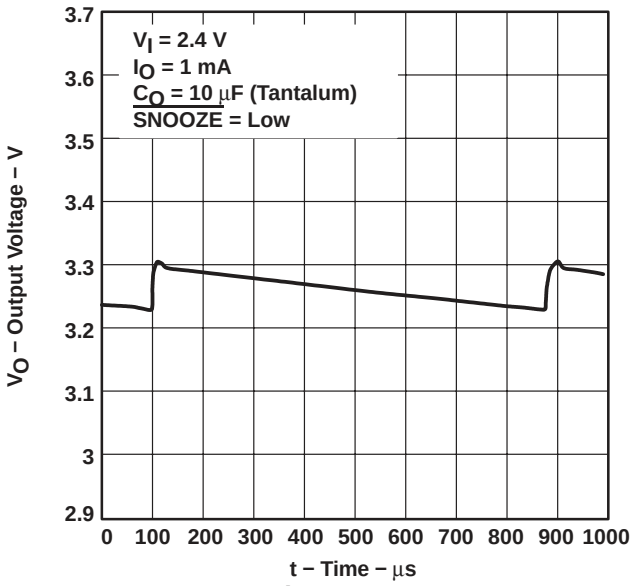


Figure 17

TPS60210
OUTPUT VOLTAGE RIPPLE IN SNOOZE MODE
vs
TIME

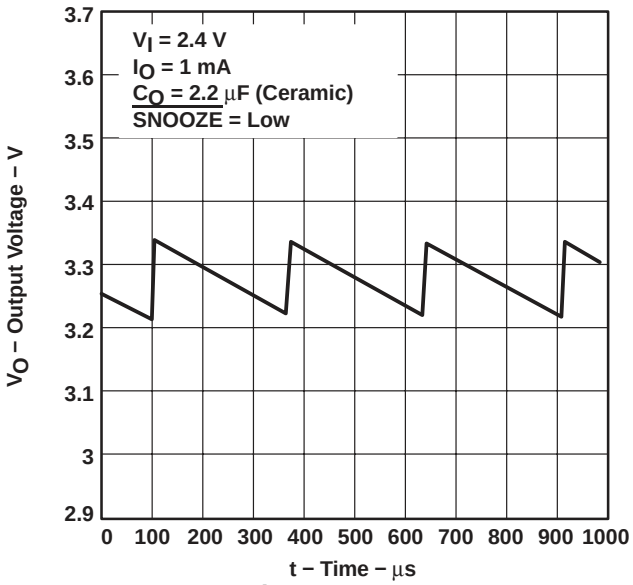


Figure 18

TPS60210
LOAD TRANSIENT RESPONSE

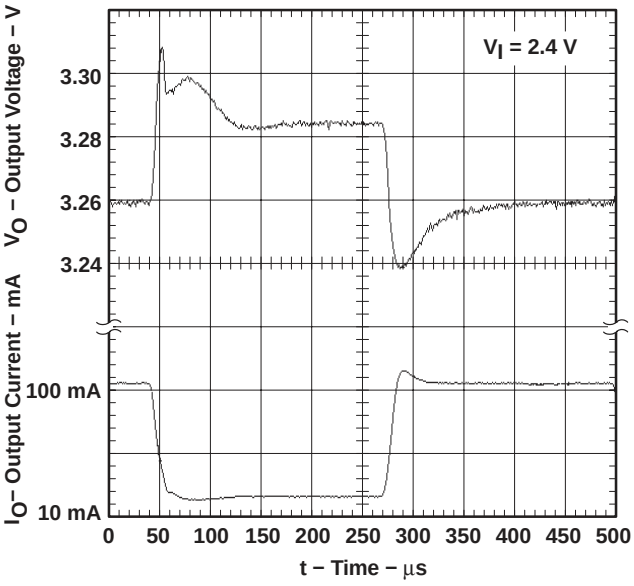


Figure 19

TPS60210
LINE TRANSIENT RESPONSE

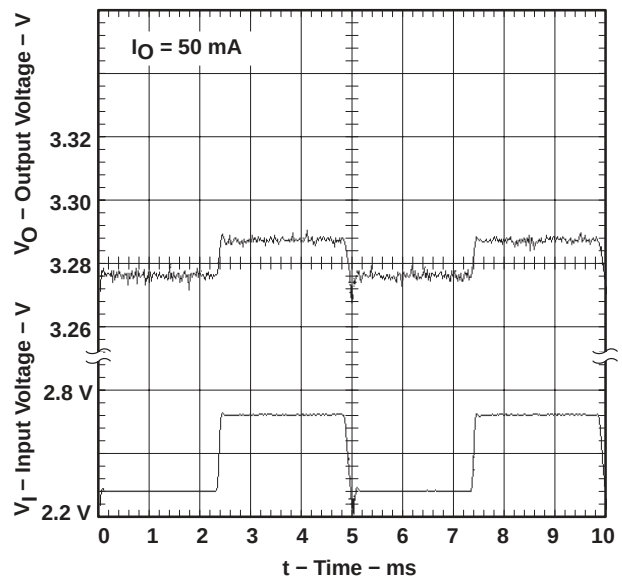


Figure 20

APPLICATION INFORMATION

capacitor selection

The TPS6021x devices require only four external capacitors to achieve a very low output voltage ripple. The capacitor values are closely linked to the required output current. Low ESR (< 0.1-Ω) capacitors should be used at the input and output of the charge pump. In general, the transfer capacitors (C1 and C2) will be the smallest. A 1-µF value is recommended if full load current performance is needed. With smaller capacitor values, the maximum possible load current is reduced and the linskip threshold is lowered.

The input capacitor improves system efficiency by reducing the input impedance. It also stabilizes the input current of the power source. The input capacitor should be chosen according to the power supply used, the distance from the power source to the converter IC. C_I is recommended to be about two to four times as large as the flying capacitors C1 and C2.

The minimum required capacitance is 2.2 µF. Larger values will improve the load transient performance and will reduce the maximum output ripple voltage. The larger the output capacitor, the better the output voltage accuracy, and the more output current can be drawn from the converter when programmed into snooze mode.

Only ceramic capacitors are recommended for input, output and flying capacitors. Depending on the material used to manufacture them, ceramic capacitors might lose their capacitance over temperature and voltage. Ceramic capacitors of type X7R or X5R material will keep their capacitance over temperature and voltage, whereas Z5U- or Y5V-type capacitors will decrease in capacitance. Table 1 lists recommended capacitor values.

APPLICATION INFORMATION

Table 2. Recommended Capacitor Values (Ceramic X5R and X7R)

LOAD CURRENT, I_{LOAD} (mA)	FLYING CAPACITORS, C1/C2 (μF)	INPUT CAPACITOR, C_{IN} (μF)	OUTPUT CAPACITOR, C_{OUT} (μF)	OUTPUT VOLTAGE RIPPLE IN LINEAR MODE, V_{P-P} (mV)	OUTPUT VOLTAGE RIPPLE IN SKIP MODE, V_{P-P} (mV)
0−100	1	2.2	2.2	3	20
0−100	1	4.7	4.7	3	10
0−100	1	2.2	10	3	7
0−100	2.2	4.7	4.7	3	10
0−50	0.47	2.2	2.2	3	20
0−25	0.22	2.2	2.2	5	15
0−10	0.1	2.2	2.2	5	15

Table 3. Recommended Capacitor Types

MANUFACTURER	PART NUMBER	SIZE	CAPACITANCE	TYPE
Taiyo Yuden	UMK212BJ104MG	0805	0.1 μF	Ceramic
	EMK212BJ224MG	0805	0.22 μF	Ceramic
	EMK212BJ474MG	0805	0.47 μF	Ceramic
	LMK212BJ105KG	0805	1 μF	Ceramic
	LMK212BJ225MG	0805	2.2 μF	Ceramic
	EMK316BJ225KL	1206	2.2 μF	Ceramic
	LMK316BJ475KL	1206	4.7 μF	Ceramic
	JMK316BJ106ML	1206	10 μF	Ceramic
AVX	0805ZC105KAT2A	0805	1 μF	Ceramic
	1206ZC225KAT2A	1206	2.2 μF	Ceramic

Table 4. Recommended Capacitor Manufacturers

MANUFACTURER	CAPACITOR TYPE	INTERNET SITE
Taiyo Yuden	X7R/X5R ceramic	http://www.t−yuden.com/
AVX	X7R/X5R ceramic	http://www.avxcorp.com/

APPLICATION INFORMATION

typical operating circuit TPS60210

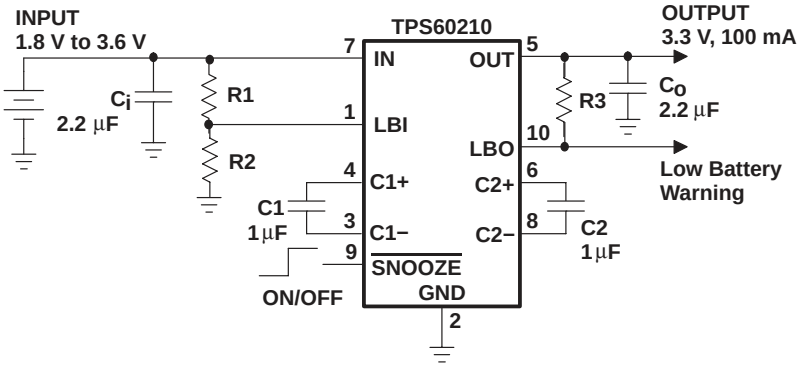


Figure 21. Typical Operating Circuit TPS60210 With Low-Battery Comparator

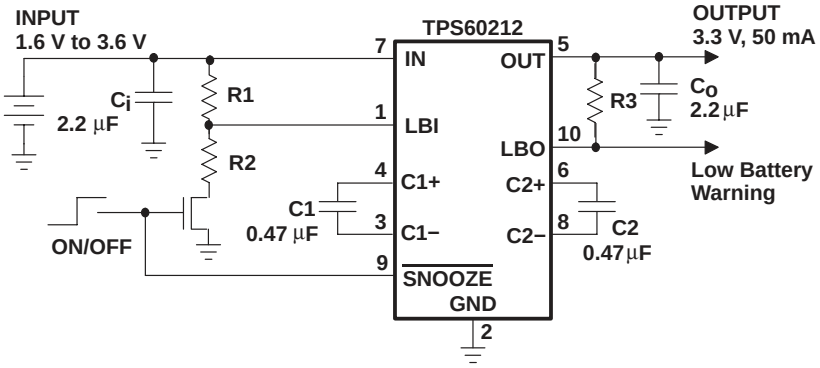


Figure 22. Typical Operating Circuit TPS60212 With Low-Battery Comparator

The current losses through the resistive divider used to set the low-battery threshold can be avoided if an additional MOSFET (like BSS138) is used in series to the resistors. This switch is controlled using the $\overline{\text{SNOOZE}}$ signal. When the $\overline{\text{SNOOZE}}$-signal is taken high, the device is programmed into normal operating mode, the switch will turn on and the resistive divider draws current to set the LBI threshold voltage. When $\overline{\text{SNOOZE}}$ is taken low, the device is programmed into snooze mode during which the low-battery comparator is disabled. In addition, the resistive divider R1/R2 is disconnected from GND and therefore draws no current from the battery. A typical schematic for this circuit is shown in Figure 22.

APPLICATION INFORMATION

typical operating circuit TPS60211

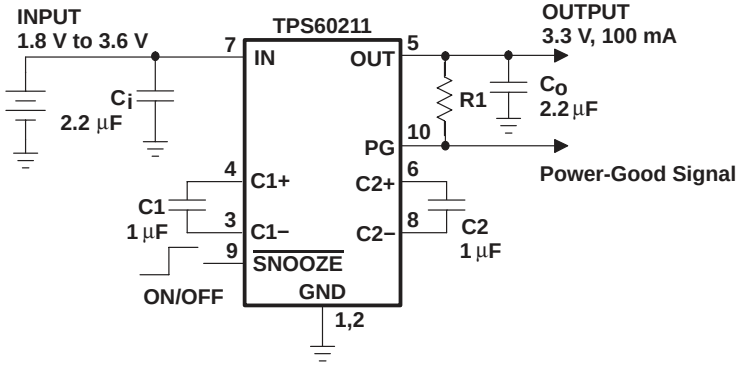


Figure 23. Typical Operating Circuit TPS60211 With Power-Good Comparator

power dissipation

The power dissipated in the TPS6021x devices depends mainly on input voltage (V_I) and output current (I_O) and is approximated by:

$$P_{(DISS)} = I_O \times \left(2 \times V_I - V_O\right) \text{ for } I_{(Q)} << I_O \quad (5)$$

By observing equation 5, it can be seen that the power dissipation is worse with a higher input voltage and a higher output current. For an input voltage of 3.6 V and an output current of 100 mA, the calculated power dissipation ($P_{(DISS)}$) is 390 mW. This is also the point where the charge pump operates with its lowest efficiency.

With the recommended maximum junction temperature of 125°C and an assumed maximum ambient operating temperature of 85°C, the maximum allowed thermal resistance junction to ambient of the system can be calculated.

$$R_{\Theta JA(max)} = \frac{T_{J(MAX)} - T_A}{P_{DISS(max)}} = \frac{125°C - 85°C}{390\ mW} = 102°C/W \quad (6)$$

P_{DISS} must be less than that allowed by the package rating. The thermal resistance junction to ambient of the used 10-pin MSOP is 294°C/W for an unsoldered package. The thermal resistance junction to ambient with the IC soldered to a printed circuit using a board layout as described in the application information section, the $R_{\Theta JA}$ is typically 200°C/W, which is higher than the maximum value calculated previously. However, in a battery powered application, both the V_I and the ambient temperature (T_A) will typically be lower than the worst case ratings used in equation 6, and P_{DISS} should not be a problem in most applications.

layout and board space

Careful board layout is necessary due to the high transient currents and switching frequency of the converter. All capacitors should be placed in close proximity to the device. A PCB layout proposal for a one-layer board is given in Figure 24.

An evaluation module for the TPS60210 is available and can be ordered under product code TPS60210EVM−167. The EVM uses the layout shown in Figure 26. The EVM has the form factor of a 14-pin dual in-line package and can be mounted accordingly on a socket. All components, including the pins, are shown in Figure 24. The actual size of the EVM is 17,9 mm x 10,2 mm = 182,6 mm^2.

APPLICATION INFORMATION

layout and board space (continued)

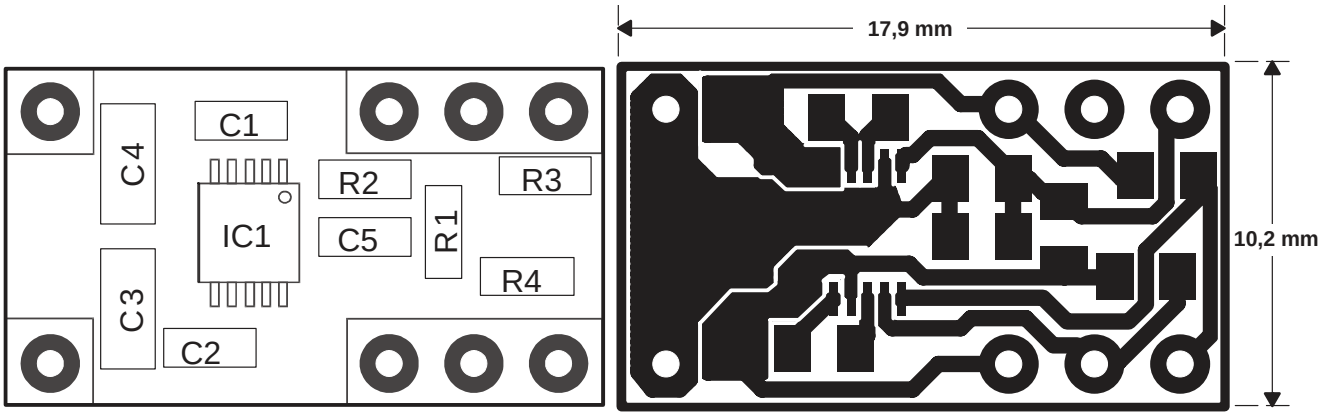


Figure 24. Recommended Component Placement and Board Layout

Table 5. Component Identification

IC1	TPS60210
C1, C2	Flying capacitors
C3	Input capacitor
C4	Output capacitor
C5	Stabilization capacitor for LBI
R1, R2	Resistive divider for LBI
R3	Pullup resistor for LBO
R4	Pullup resistor for EN

Capacitor C5 should be included if large line transients are expected. This capacitor suppresses toggling of the LBO due to these line changes.

APPLICATION INFORMATION

device family products

Other charge pump dc-dc converters from Texas Instruments are:

Table 6. Product Identification

PART NUMBER	LITERATURE NUMBER	DESCRIPTION
TPS60100	SLVS213	2-cell to regulated 3.3-V, 200-mA low-noise charge pump
TPS60101	SLVS214	2-cell to regulated 3.3-V, 100-mA low-noise charge pump
TPS60110	SLVS215	3-cell to regulated 5.0-V, 300-mA low-noise charge pump
TPS60111	SLVS216	3-cell to regulated 5.0-V, 150-mA low-noise charge pump
TPS60120	SLVS257	2-cell to regulated 3.3-V, 200-mA high-efficiency charge pump with low-battery comparator
TPS60121	SLVS257	2-cell to regulated 3.3-V, 200-mA high-efficiency charge pump with power-good comparator
TPS60122	SLVS257	2-cell to regulated 3.3-V, 100-mA high-efficiency charge pump with low-battery comparator
TPS60123	SLVS257	2-cell to regulated 3.3-V, 100-mA high-efficiency charge pump with power-good comparator
TPS60130	SLVS258	3-cell to regulated 5.0-V, 300-mA high-efficiency charge pump with low-battery comparator
TPS60131	SLVS258	3-cell to regulated 5.0-V, 300-mA high-efficiency charge pump with power-good comparator
TPS60132	SLVS258	3-cell to regulated 5.0-V, 150-mA high-efficiency charge pump with low-battery comparator
TPS60133	SLVS258	3-cell to regulated 5.0-V, 150-mA high-efficiency charge pump with power-good comparator
TPS60140	SLVS273	2-cell to regulated 5.0-V, 100-mA charge pump voltage tripler with low-battery comparator
TPS60141	SLVS273	2-cell to regulated 5.0-V, 100-mA charge pump voltage tripler with power-good comparator
TPS60200	SLVS274	2-cell to regulated 3.3-V, 100-mA low-ripple charge pump with low-battery comparator
TPS60201	SLVS274	2-cell to regulated 3.3-V, 100-mA low-ripple charge pump with power-good comparator
TPS60202	SLVS274	2-cell to regulated 3.3-V, 50-mA low-ripple charge pump with low-battery comparator
TPS60203	SLVS274	2-cell to regulated 3.3-V, 50-mA low-ripple charge pump with power-good comparator

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS60210DGS	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AFD	Samples
TPS60210DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AFD	Samples
TPS60211DGS	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AFE	Samples
TPS60212DGS	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AFF	Samples
TPS60212DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AFF	Samples
TPS60213DGS	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AFG	Samples
TPS60213DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AFG	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

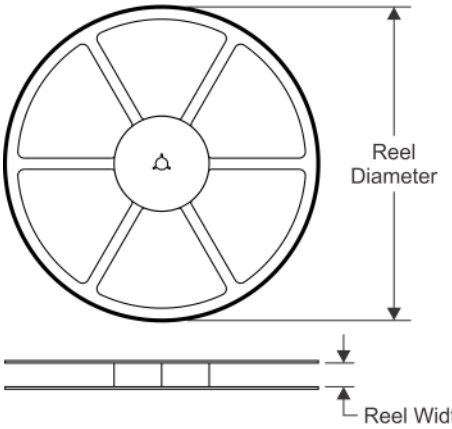
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

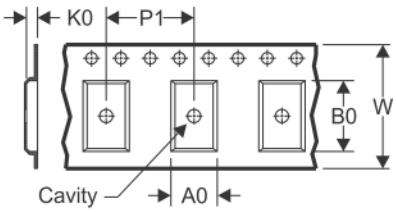
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

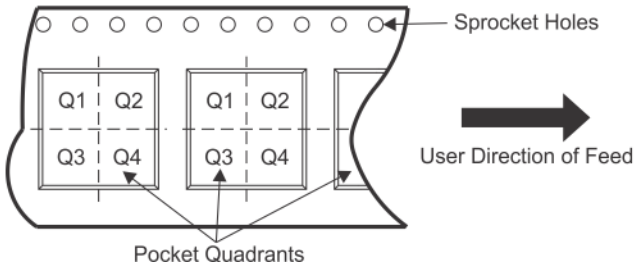


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

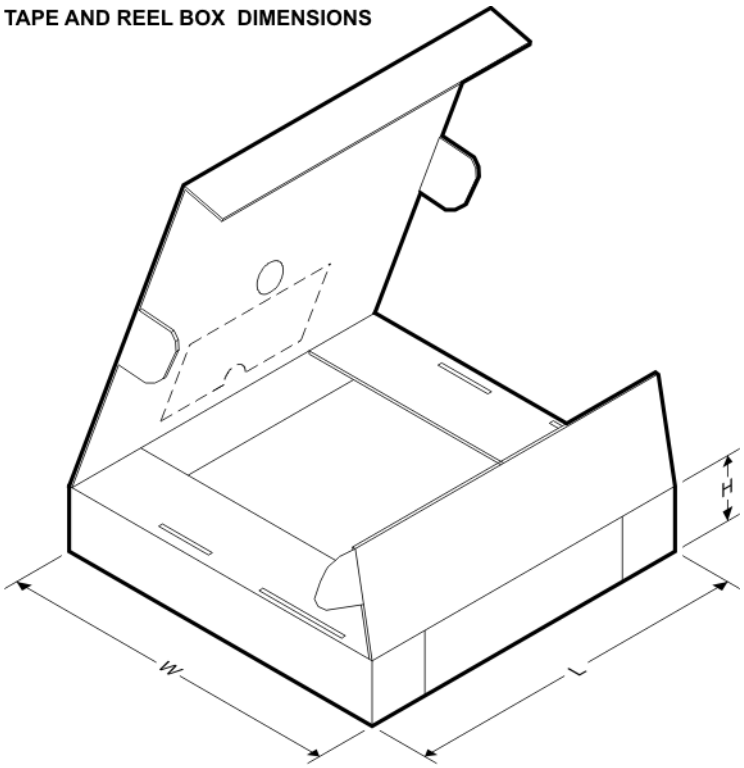
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS60210DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS60212DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS60213DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

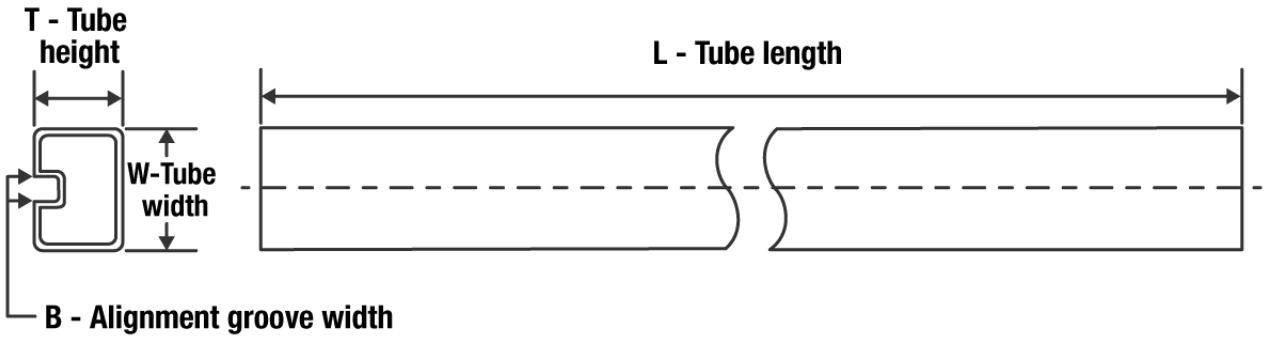
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS60210DGSR	VSSOP	DGS	10	2500	350.0	350.0	43.0
TPS60212DGSR	VSSOP	DGS	10	2500	350.0	350.0	43.0
TPS60213DGSR	VSSOP	DGS	10	2500	350.0	350.0	43.0

TUBE



*All dimensions are nominal

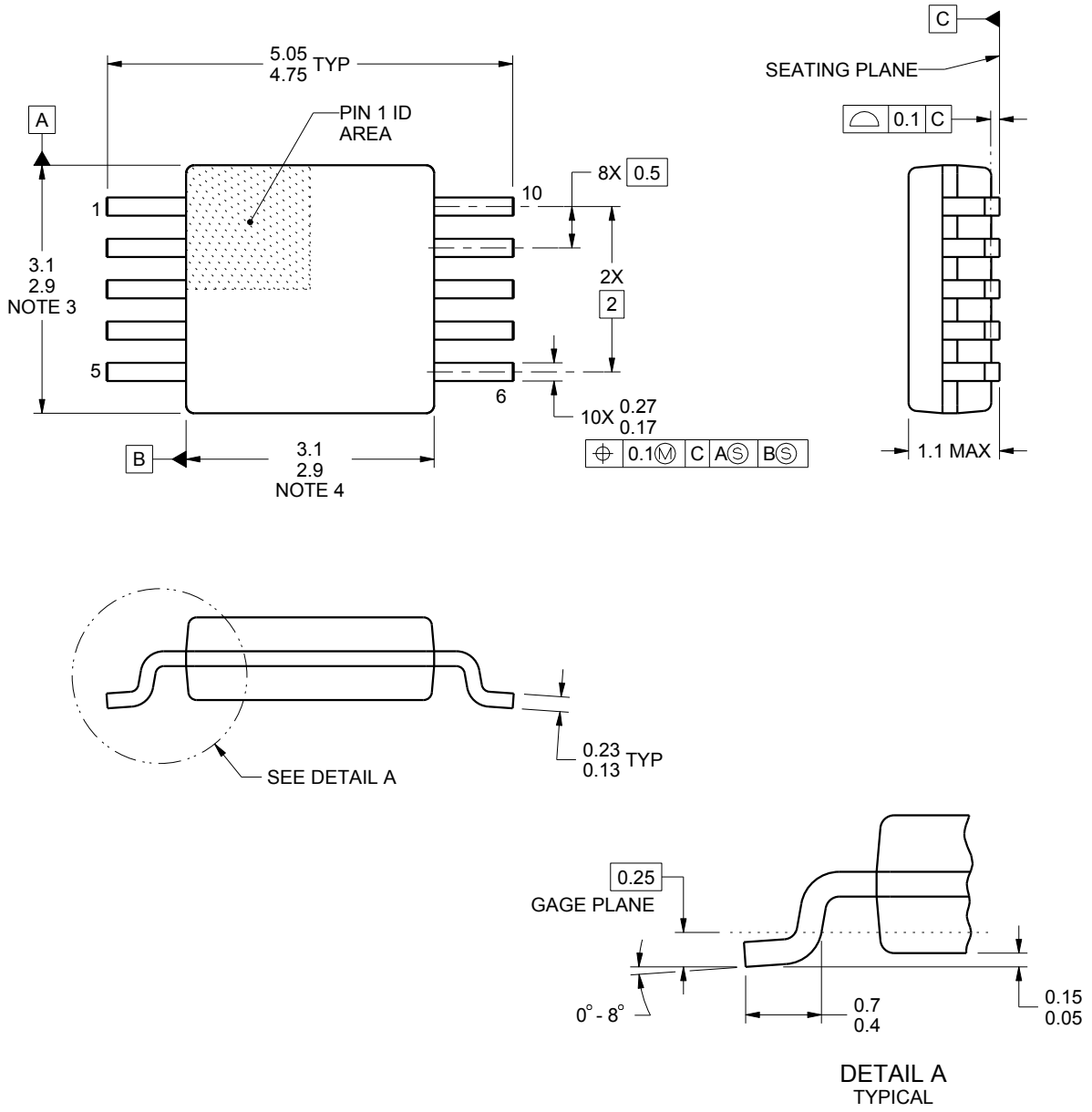
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS60210DGS	DGS	VSSOP	10	80	331.47	6.55	3000	2.88
TPS60211DGS	DGS	VSSOP	10	80	331.47	6.55	3000	2.88
TPS60212DGS	DGS	VSSOP	10	80	331.47	6.55	3000	2.88
TPS60213DGS	DGS	VSSOP	10	80	331.47	6.55	3000	2.88

PACKAGE OUTLINE

DGS0010A

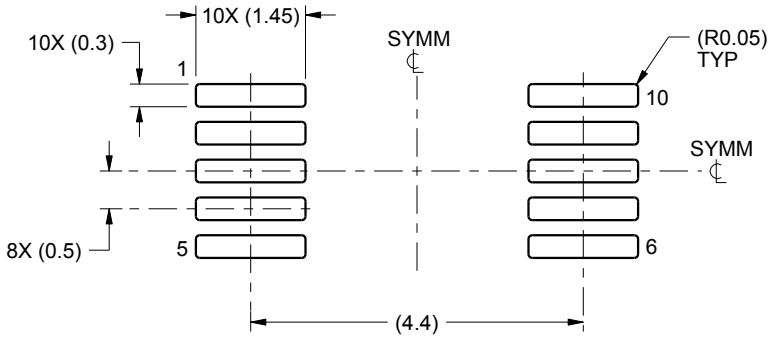
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

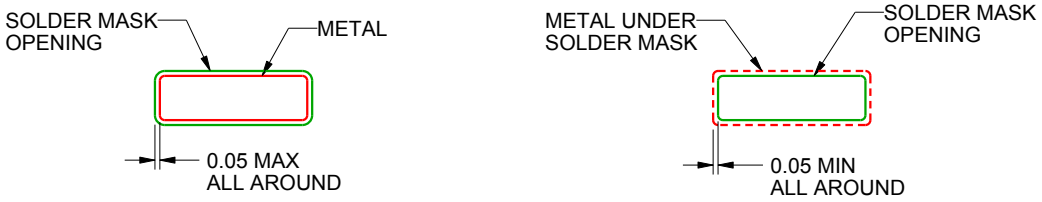


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

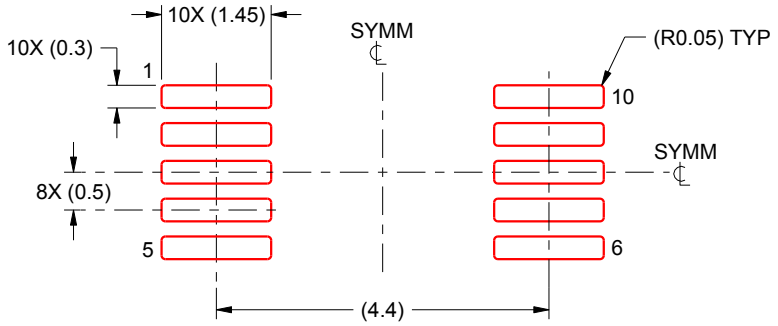


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265