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March 2006

FAIRCHILD
### SEMICONDUCTOR®

FDS9934C

Complementary

These dual N- and P-Channel enhancement mode power field effect transistors are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state ressitance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

Features

- **Q1:** 6.5 A, 20 V. $R_{DS(ON)} = 30\ m\Omega$ @ $V_{GS} = 4.5$ V
  $R_{DS(ON)} = 43\ m\Omega$ @ $V_{GS} = 2.5$ V.

- **Q2:** −5 A, −20 V, $R_{DS(ON)} = 55\ m\Omega$ @ $V_{GS} = -4.5$ V
  $R_{DS(ON)} = 90\ m\Omega$ @ $V_{GS} = -2.5$ V

SO-8

Pin 1
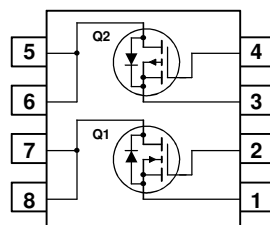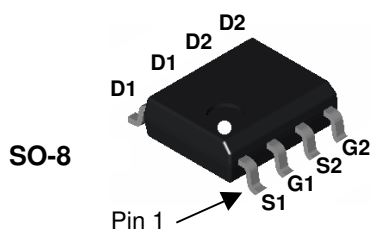
Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings		Units
			Q1	Q2	
V_{DSS}	Drain-Source Voltage		20	−20	V
V_{GSS}	Gate-Source Voltage		±10	±12	V
I_D	Drain Current – Continuous	(Note 1a)	6.5	−5	A
	– Pulsed		20	−30	
P_D	Power Dissipation for Dual Operation		2		W
	Power Dissipation for Single Operation	(Note 1a)	1.6		
		(Note 1b)	1		
		(Note 1c)	0.9		
T_J, T_{STG}	Operating and Storage Junction Temperature Range		−55 to +150		°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS9934C	FDS9934C	13''	12mm	2500 units

Electrical Characteristics

$T_A = 25°C$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Off Characteristics							
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0$ V, $I_D = 250$ µA $V_{GS} = 0$ V, $I_D = -250$ µA	Q1 Q2	20 −20			V
$\dfrac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250$ µA, Referenced to 25°C $I_D = -250$ µA, Referenced to 25°C	Q1 Q2		14 −14		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 16$V, $V_{GS} = 0$ V $V_{DS} = -16$V, $V_{GS} = 0$ V	Q1 Q2			1 −1	µA
I_{GSS}	Gate-Body Leakage	$V_{GS} = \pm 8$ V, $V_{DS} = 0$ V $V_{GS} = \pm 12$ V, $V_{DS} = 0$ V	Q1 Q2			±100 ±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250$ µA $V_{DS} = V_{GS}$, $I_D = 250$ µA	Q1 Q2	0.6 −0.6	1 −0.9	1.5 −1.2	V
$\dfrac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250$ uA, Referenced to 25°C $I_D = 250$ uA, Referenced to 25°C	Q1 Q2		−3 3		mV/°C
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 4.5$ V, $I_D = 6.5$ A $V_{GS} = 2.5$ V, $I_D = 5.4$ A $V_{GS} = 4.5$ V, $I_D = 6.5$A, $T_J = 125$°C	Q1		25 35 35	30 43 50	mΩ
		$V_{GS} = -4.5$ V, $I_D = -3.2$ A $V_{GS} = -2.5$ V, $I_D = -1.0$ A $V_{GS} = -4.5$ V,$I_D = -3.2$ A, $T_J = 125$°C	Q2		43 64 55	55 90 76	mΩ
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 4.5$V, $V_{DS} = 5$ V $V_{GS} = -4.5$ V, $V_{DS} = -5$ V	Q1 Q2	15 −16			A
g_{FS}	Forward Transcoductance	$V_{DS} = -5$ V, $I_D = 6.5$ A $V_{DS} = 5$ V, $I_D = -5.5$ A	Q1 Q2		22 14		S S
Dynamic Characteristics							
C_{iss}	Input Capacitance	Q1 $V_{DS} = 10$V, $V_{GS} = 0$ V,	Q1 Q2		650 955		pF
C_{oss}	Output Capacitance	$f = 1.0$ MHz Q2	Q1 Q2		150 215		pF
C_{rss}	Reverse Transfer Capacitance	$V_{DS} = -10$ V, $V_{GS} = 0$ V, $f = 1.0$ MHz	Q1 Q2		85 115		pF
R_G	Gate Resistance	$V_{GS} = 15$ mV, $f = 1.0$ MHz	Q1 Q2		1.4 4.9		Ω

Electrical Characteristics (continued) $T_A = 25°C$ unless otherwise noted

| Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Switching Characteristics (Note 2)							
$t_{d(on)}$	Turn-On Delay Time	Q1 $V_{DD} = 10$ V, $I_D = 1$ A,	Q1		8	16	ns
			Q2		16	29	
t_r	Turn-On Rise Time	$V_{GS} = 4.5V$, $R_{GEN} = 6\Omega$	Q1		9	17	ns
			Q2		9	18	
$t_{d(off)}$	Turn-Off Delay Time	Q2 $V_{DD} = -6V$, $I_D = -1A$,	Q1		15	26	ns
			Q2		25	41	
t_f	Turn-Off Fall Time	$V_{GS} = -4.5V$, $R_{GEN} = 6\Omega$	Q1		4	9	ns
			Q2		9	19	
Q_g	Total Gate Charge	Q1 $V_{DS} = 10$ V, $I_D = 3$ A, $V_{GS} = 4.5V$	Q1		6.2	9	nC
			Q2		8.7	12	
Q_{gs}	Gate-Source Charge		Q1		1.2		nC
			Q2		2.1		
Q_{gd}	Gate-Drain Charge	Q2 $V_{DS} = -6$ V, $I_D = -3.2$ A, $V_{GS} = -4.5$ V	Q1		1.7		nC
			Q2		2.1		
Drain–Source Diode Characteristics and Maximum Ratings							
I_S	Maximum Continuous Drain-Source Diode Forward Current		Q1			1.3	A
			Q2			−1.3	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0$ V, $I_S = 1.3$ A (Note 2)	Q1		0.73	1.2	V
		$V_{GS} = 0$ V, $I_S = -2.0$ A (Note 2)	Q2		−0.8	−1.2	
t_{rr}	Diode Reverse Recovery Time	Q1 $I_F = 6.5$ A, $d_{iF}/d_t = 100$ A/μs	Q1		15		nS
			Q2		20		
Q_{rr}	Diode Reverse Recovery Charge	Q2 $I_F = -3.2$ A, $d_{iF}/d_t = 100$ A/μs	Q1		5		nC
			Q2		7		

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.
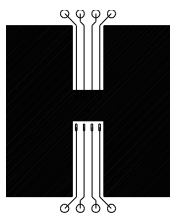
a) 78°C/W when mounted on a 0.5 in^2 pad of 2 oz copper
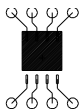
b) 125°C/W when mounted on a .02 in^2 pad of 2 oz copper
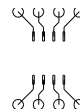
c) 135°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%

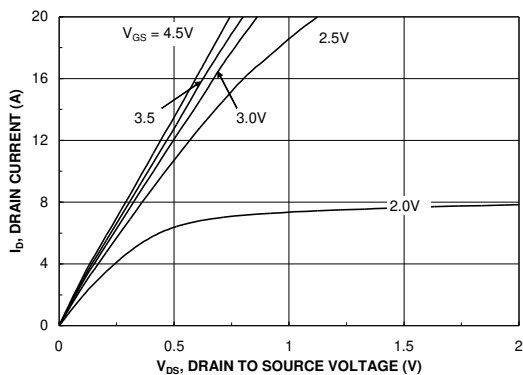# Typical Characteristics: Q1 (N-Channel)

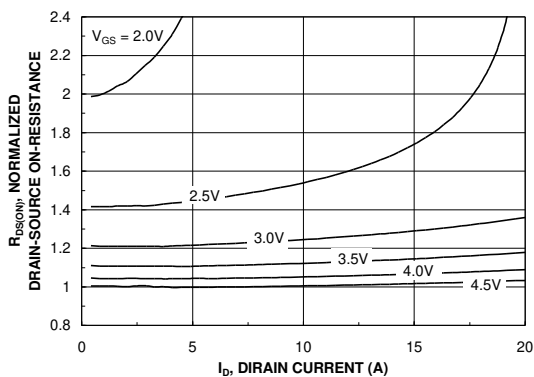**Figure 1. On-Region Characteristics.**

**Figure 2. On-Resistance Variation with
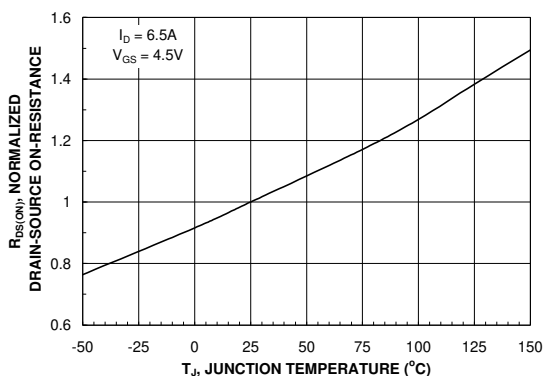Drain Current and Gate Voltage.**

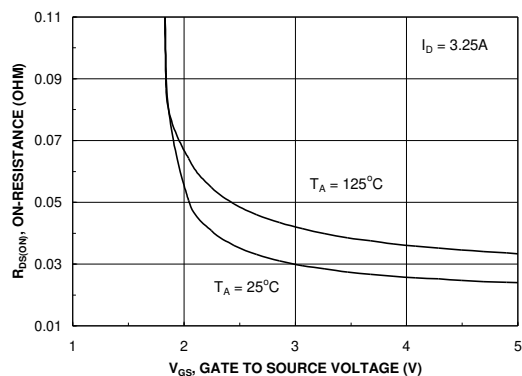**Figure 3. On-Resistance Variation with
Temperature.**

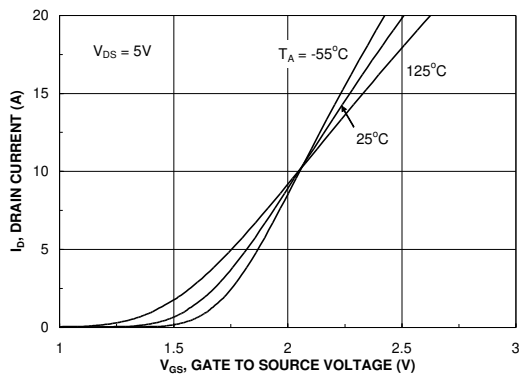**Figure 4. On-Resistance Variation with
Gate-to-Source Voltage.**
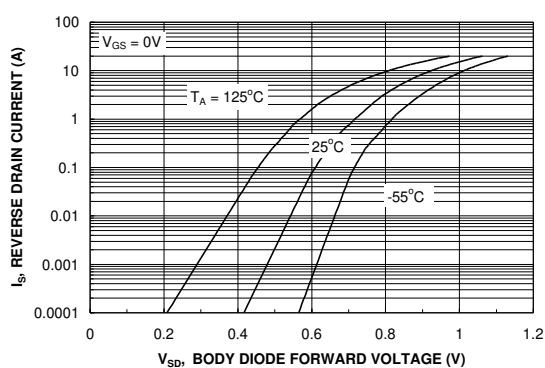
Figure 5. Transfer Characteristics.

**Figure 6. Body Diode Forward Voltage Variation
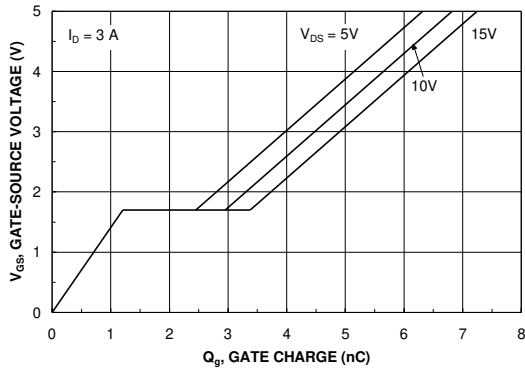with Source Current and Temperature.**
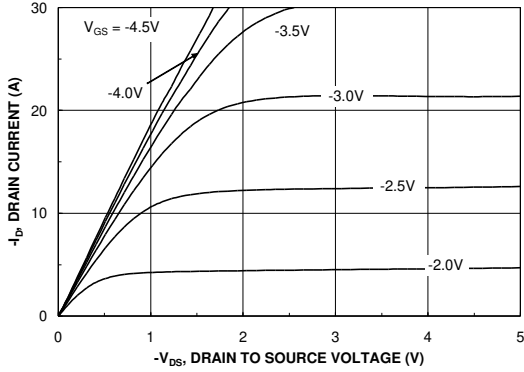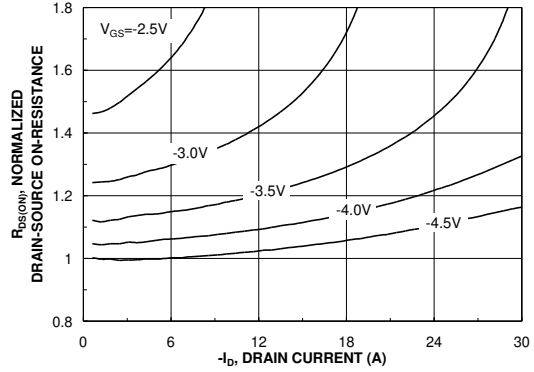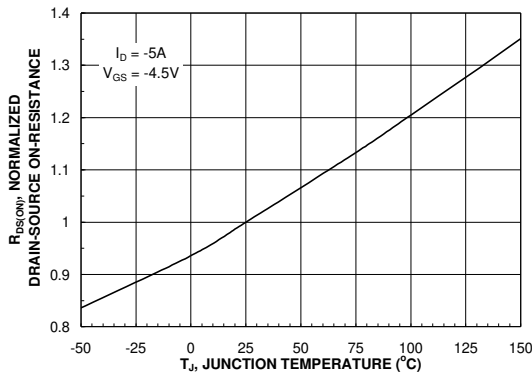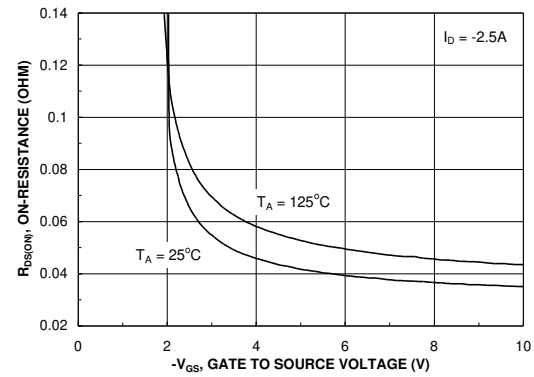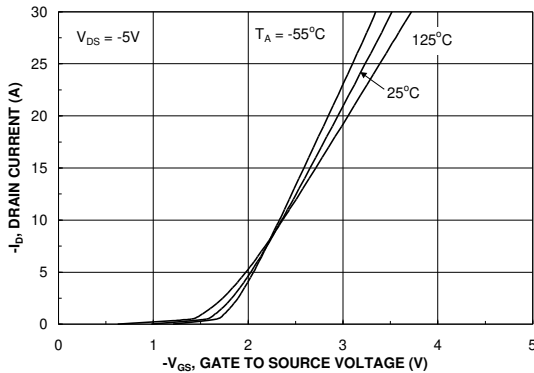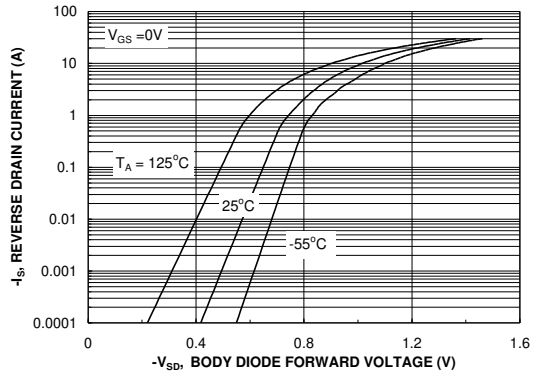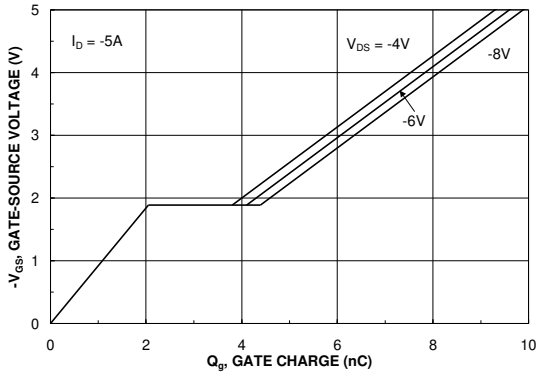
Typical Characteristics: Q1 (N-Channel)
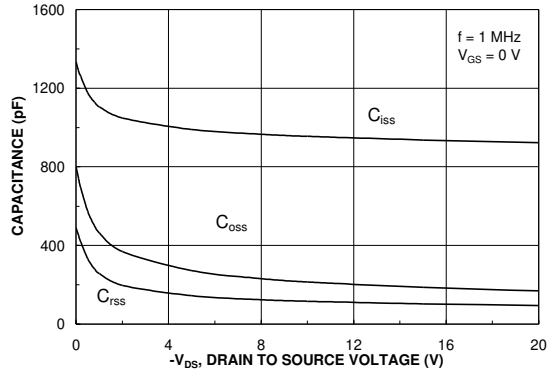

Figure 7. Gate Charge Characteristics.
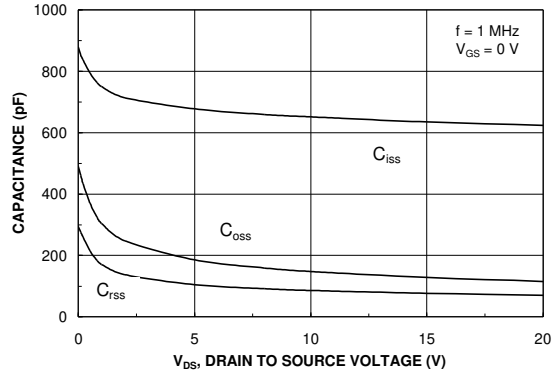
Figure 8. Capacitance Characteristics.
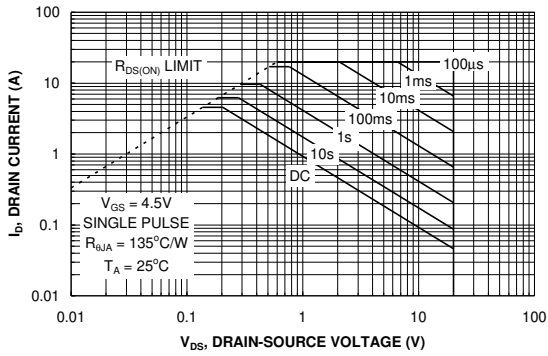
Figure 9. Maximum Safe Operating Area.
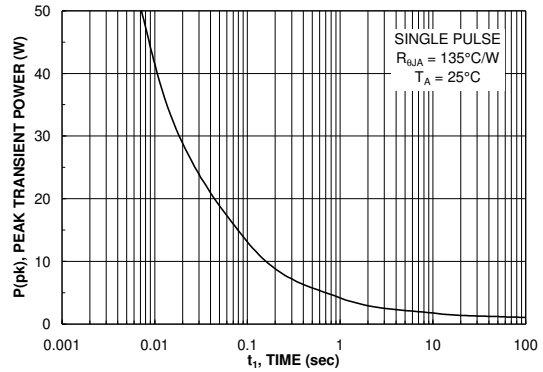
Figure 10. Single Pulse Maximum Power Dissipation.

Typical Characteristics: Q2 (P-Channel)

Figure 11. On-Region Characteristics.

Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

Figure 13. On-Resistance Variation with Temperature.

Figure 14. On-Resistance Variation with Gate-to-Source Voltage.

Figure 15. Transfer Characteristics.

Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: Q2 (P-Channel)

Figure 17. Gate Charge Characteristics.
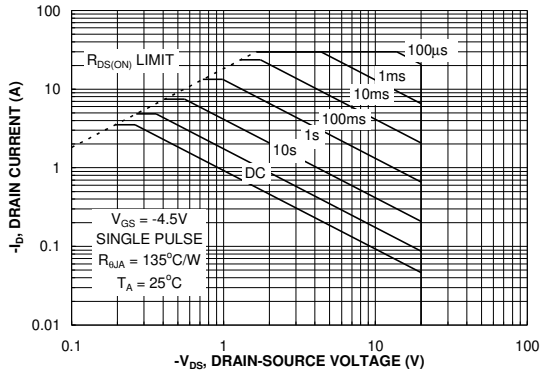

Figure 18. Capacitance Characteristics.
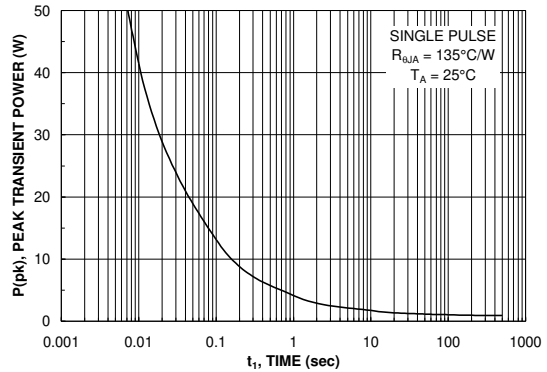

Figure 19. Maximum Safe Operating Area.

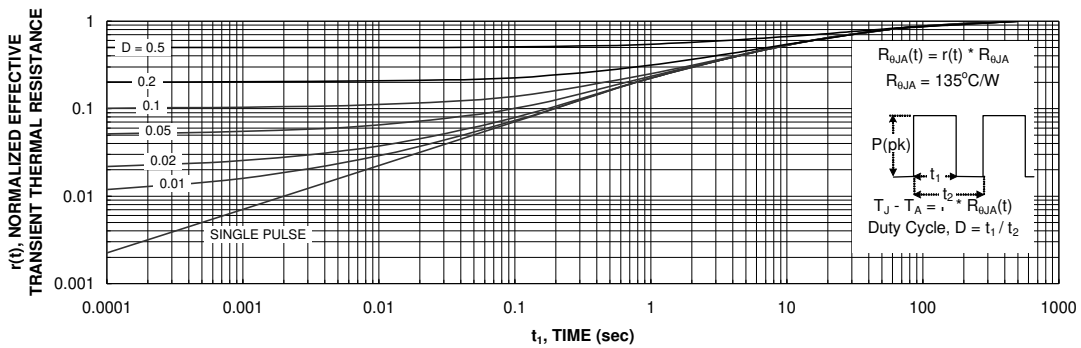**Figure 20. Single Pulse Maximum Power Dissipation.**

Figure 21. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

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