

1. General description

Planar passivated SCR with sensitive gate in a SOT223 surface mountable plastic package. This SCR is designed to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

2. Features and benefits

- On-state RMS current, 1.25 A
- Repetitive peak off-state voltage, 1000 V
- High surge current capability
- Direct triggering from low power drivers and logic ICs
- Planar passivated for voltage ruggedness and reliability
- Surface mountable package

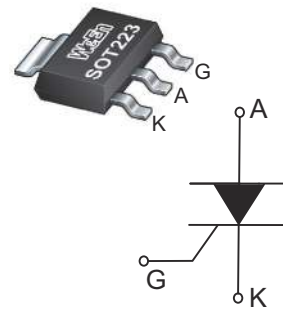
3. Applications

- GFCI (Ground Fault Circuit Interrupter)
- AFCI (Arc Fault Circuit Interrupter)
- RCD (Residual Current Device)
- RCBO (Residual Current circuit Breaker with Overload protection)
- AFDD (Arc Fault Detection Device)

4. Quick reference data

Table 1. Quick reference data

Symbol	Values	Unit
V_{DRM}, V_{RRM}	1000	V
$I_{T(RMS)}$	1.25	A
I_{GT}	≤90	μA
T_j	125	°C



5. Characteristics

Table 2. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Values	Unit
V_{DRM}	repetitive peak off-state voltage		1000	V
V_{RRM}	repetitive peak reverse voltage		1000	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_c \leq 105\text{ }^\circ\text{C}$	0.8	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_c \leq 105\text{ }^\circ\text{C}$	1.25	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$; $t_p = 10\text{ ms}$	23	A
		half sine wave; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$; $t_p = 8.3\text{ ms}$	25	A
I^2t	I^2t for fusing	$t_p = 10\text{ ms}$; sine-wave pulse	2.645	A^2s
di_T/dt	rate of rise of on-state current	$I_G = 0.1\text{ mA}$	100	$\text{A}/\mu\text{s}$
I_{GM}	peak gate current		1.2	A
P_{GM}	peak gate power		2	W
$P_{G(AV)}$	average gate power	over any 20 ms period	0.2	W
T_{stg}	storage temperature		-40 to 150	$^\circ\text{C}$
T_j	junction temperature		-40 to 125	$^\circ\text{C}$

Table 3. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $R_L = 100\text{ }\Omega$; $T_j = 25\text{ }^\circ\text{C}$	10	-	90	μA
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}$; $R_L = 100\text{ }\Omega$; $T_j = 25\text{ }^\circ\text{C}$	-	0.6	0.8	V
		$V_D = 800\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 125\text{ }^\circ\text{C}$	0.25	0.4	-	V
V_{RG}	gate reverse voltage	$I_{RG} = 2\text{ mA}$	10	-	-	V
I_L	latching current	$I_T = 0.1\text{ A}$; $R_{GK} = 1\text{ k}\Omega$; $T_j = 25\text{ }^\circ\text{C}$	-	-	5	mA
I_H	holding current	$V_D = 12\text{ V}$; $R_{GK} = 1\text{ k}\Omega$; $T_j = 25\text{ }^\circ\text{C}$	-	-	3	mA
V_T	on-state voltage	$I_T = 2.5\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$	-	-	1.45	V
I_{DRM}	off-state current	$V_D = V_{DRM} / V_{RRM}$; $R_{GK} = 1\text{ k}\Omega$				$T_j = 25\text{ }^\circ\text{C}$
I_{RRM}	reverse current					$T_j = 125\text{ }^\circ\text{C}$
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 670\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; $R_{GK} = 1\text{ k}\Omega$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform	50	-	-	$\text{V}/\mu\text{s}$

Table 4. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-c)}$	thermal resistance from junction to case		SOT223	-	-	20	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	SOT223	-	120	-	K/W

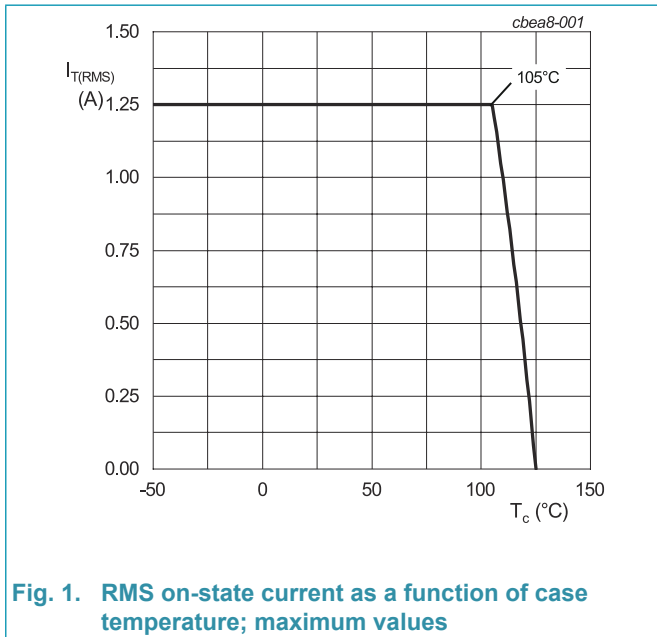
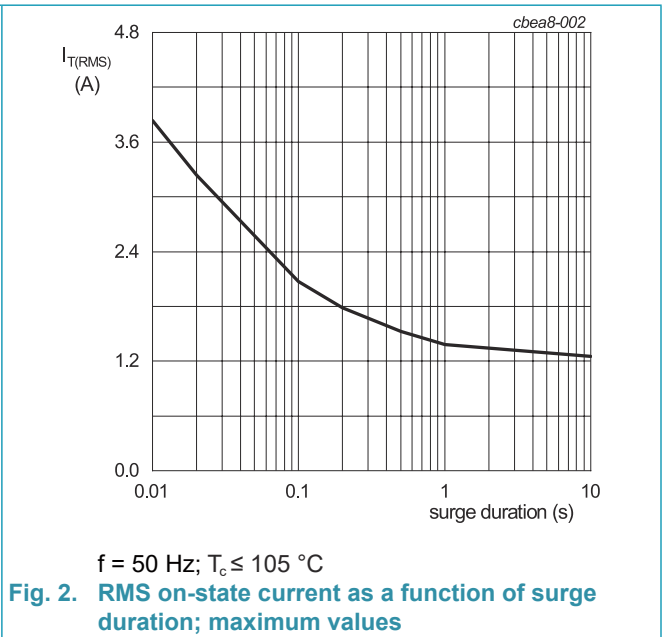
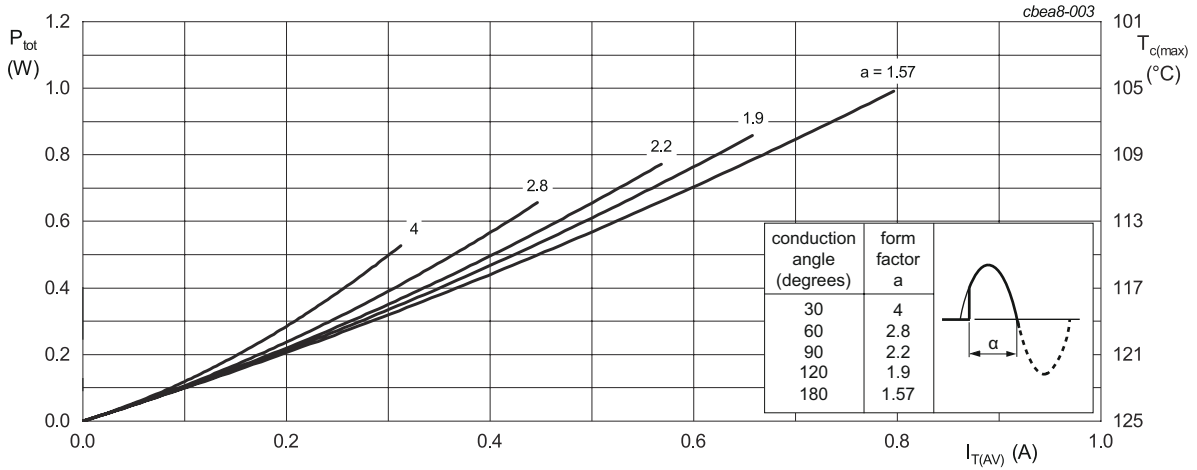


Fig. 1. RMS on-state current as a function of case temperature; maximum values



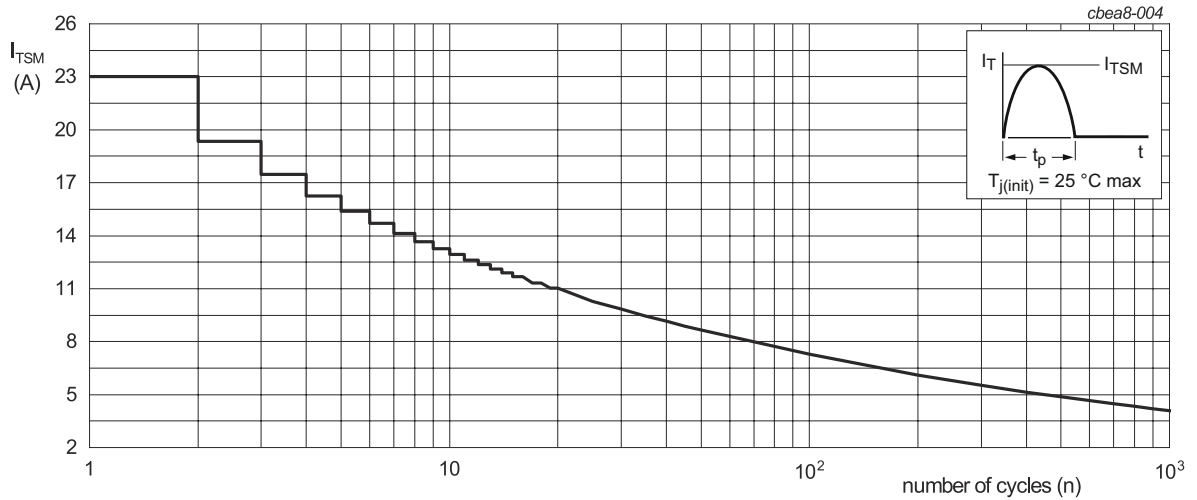
f = 50 Hz; $T_c \leq 105$ °C

Fig. 2. RMS on-state current as a function of surge duration; maximum values



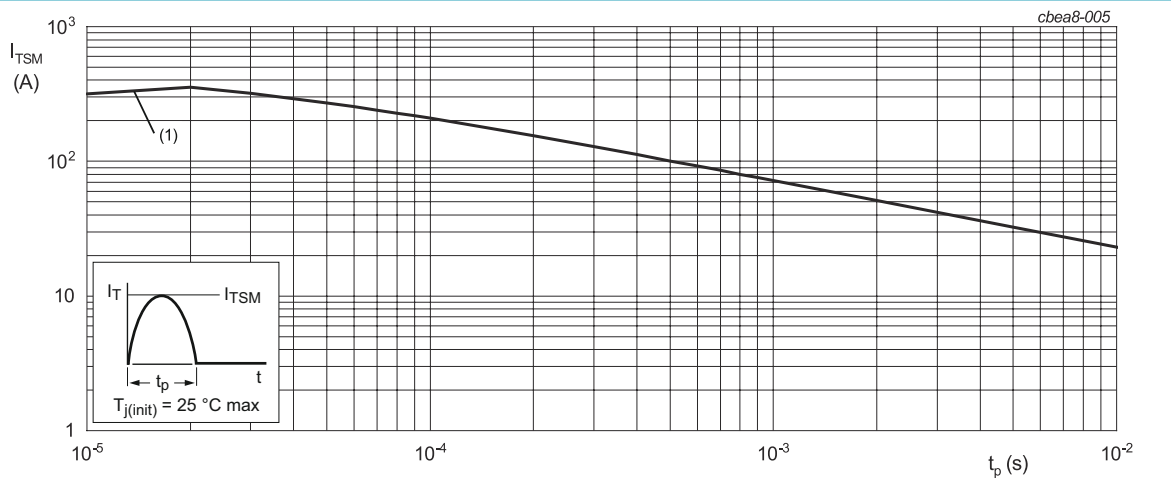
α = conduction angle
 a = form factor = $I_{T(RMS)} / I_{T(AV)}$

Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values



$f = 50 \text{ Hz}$

Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



$t_p \leq 10 \text{ ms}$
 (1) di_T/dt limit

Fig. 5. Non-repetitive peak on-state current as a function of pulse duration; maximum values

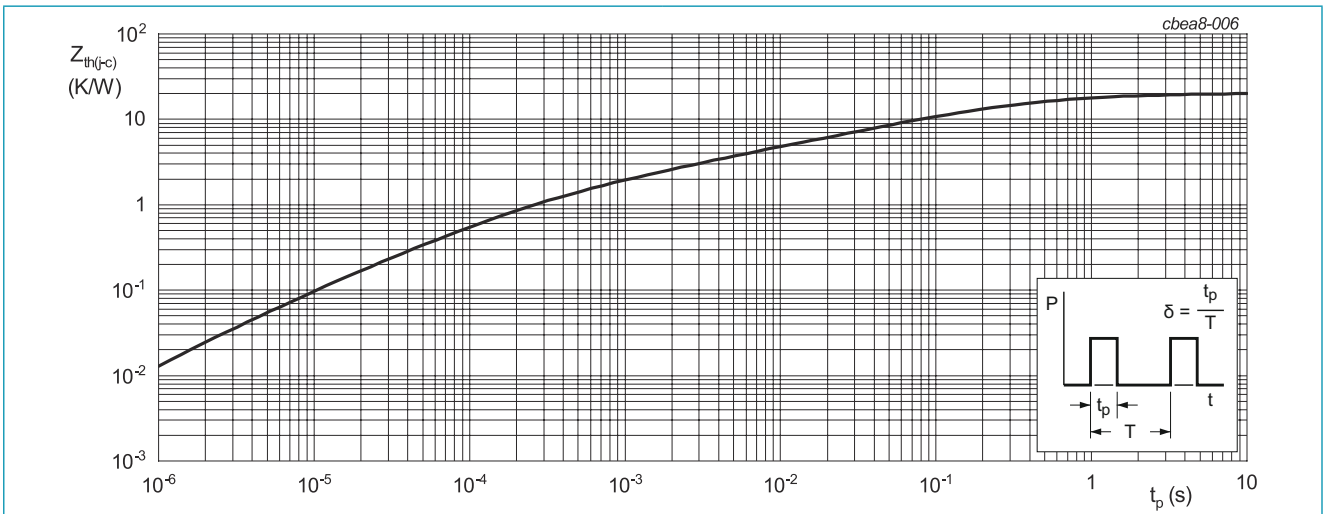


Fig. 6. Transient thermal impedance from junction to case as a function of pulse duration

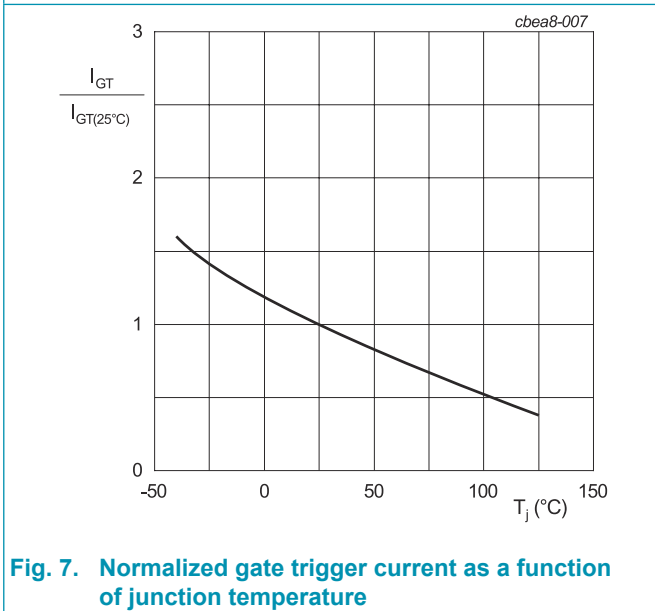


Fig. 7. Normalized gate trigger current as a function of junction temperature

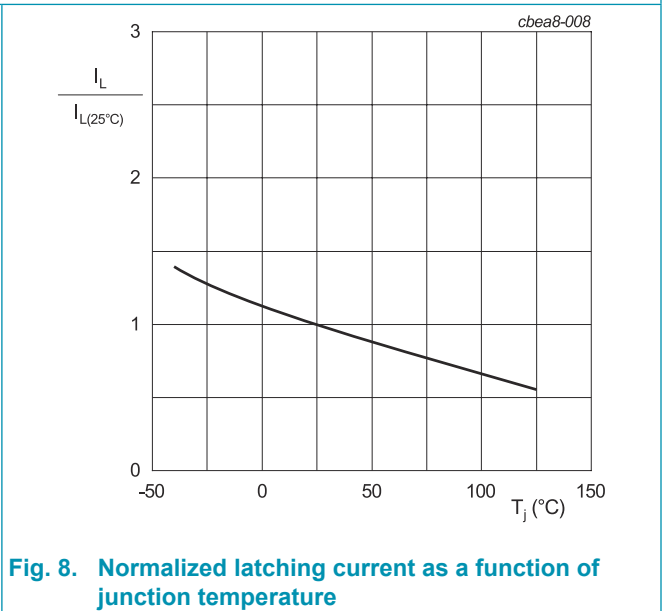


Fig. 8. Normalized latching current as a function of junction temperature

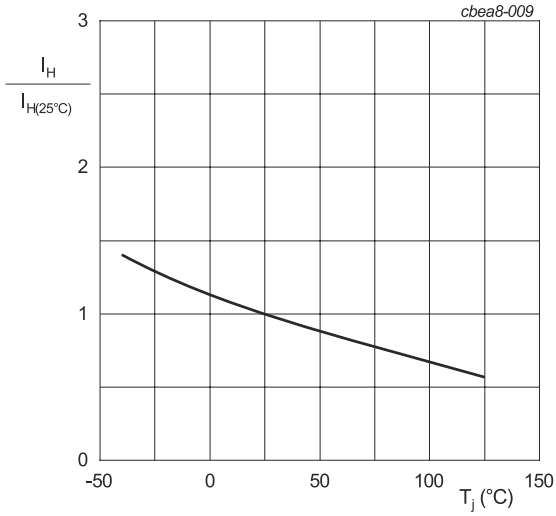
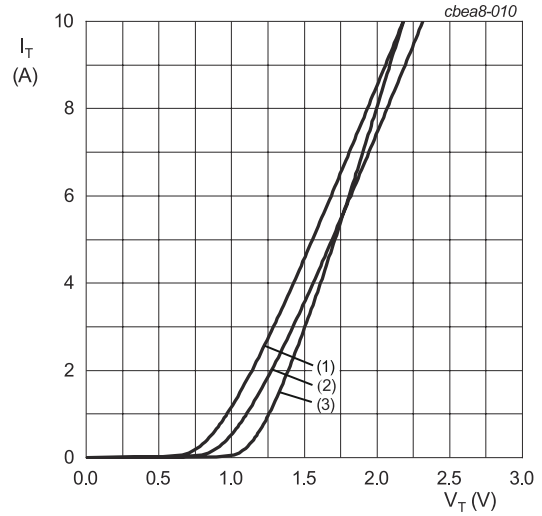


Fig. 9. Normalized holding current as a function of junction temperature



$V_o = 0.957 \text{ V}; R_s = 0.1464 \Omega$
 (1) $T_j = 150 \text{ }^\circ\text{C}$; typical values
 (2) $T_j = 150 \text{ }^\circ\text{C}$; maximum values
 (3) $T_j = 25 \text{ }^\circ\text{C}$; maximum values

Fig. 10. On-state current as a function of on-state voltage

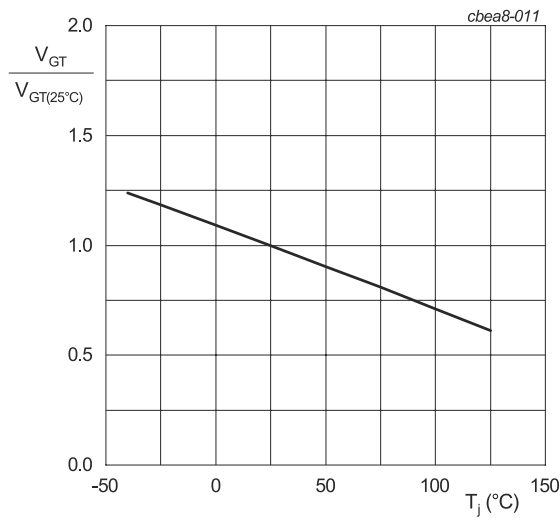


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

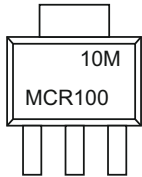
6. Ordering information

Table 5. Ordering information

Type number	Package Name	Orderable part number	Packing method	Small packing quantity	Package version	Package issue date
MCR100W-10M	SOT223		Reel	1000	SOT223	16-Mar-2006

7. Marking

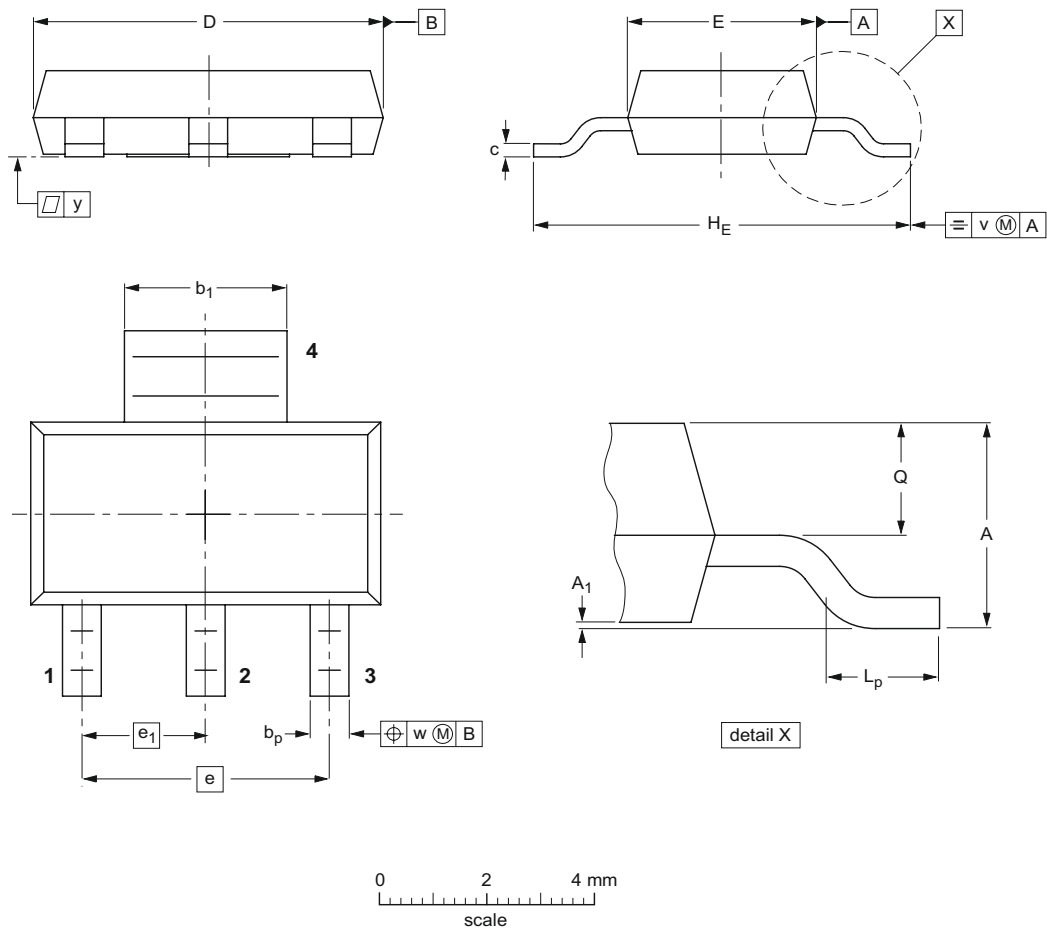
Table 6. Marking codes

Type number	Marking codes
MCR100W-10M	 A schematic diagram of a 3-pin SOT223 package. The package is rectangular with a small tab at the top. It has three pins extending downwards. The marking codes '10M' and 'MCR100' are shown on the top surface of the package.

8. Package outline

Plastic surface-mounted package with increased heatsink; 4 leads

SOT223



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b _p	b ₁	c	D	E	e	e ₁	H _E	L _p	Q	v	w	y
mm	1.8 1.5	0.10 0.01	0.80 0.60	3.1 2.9	0.32 0.22	6.7 6.3	3.7 3.3	4.6	2.3	7.3 6.7	1.1 0.7	0.95 0.85	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT223			SC-73			04-11-10 06-03-16

9. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Date of release: 27 August 2021
