

# CGD65B200S2 DATASHEET

650 V / 200 m $\Omega$  GaN HEMT with  
ICeGaN™ Gate and Current Sense

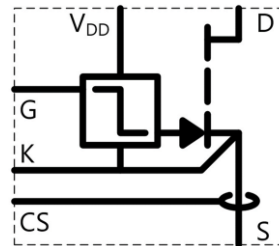
DECEMBER 2022



# 650 V / 200 mΩ GaN HEMT with ICeGaN™ Gate and Current Sense

## Key features

- 650 V - 8.5 A e-mode GaN power switch
- ICeGaN™ gate technology for high gate threshold and broad gate voltage window compatible with gate-drivers and controllers for Si MOSFETs
- Gate drive voltage 9 V to 20 V
- Current sense function
- $R_{DS(on)} = 200 \text{ m}\Omega$
- Suitable for very high switching frequency
- Kelvin Contact
- Small 5x6 mm<sup>2</sup> PCB footprint
- Bottom side cooled DFN package



## Description

The CGD65B200S2 is an enhancement mode GaN-on-silicon power transistor, exploiting the unique material properties of GaN to deliver high current, high breakdown voltage and high switching frequency for a wide range of electronics applications. The CGD65B200S2 features CGD's ICeGaN™ gate technology enabling compatibility with virtually all gate drivers and controller chips available. The integrated current sense function eliminates a separate current sense resistor and the associated efficiency losses. Because no external sense resistor is needed, the device can be directly soldered to the large copper area of the ground plane, improving the thermal performance and simplifying the thermal design. It comes in a DFN 5x6 SMD package to support high frequency operation while ensuring the highest thermal performance.

## Application & Topologies

PSUs, Industrial SMPS and inverters

- Mobile chargers, fast-chargers
- AC adapters
- Notebook adapters, PC power
- Gaming PSUs
- LED lighting
- Class-D Audio
- TV and wireless power
- PV micro-inverters
- SMPS and converters in single-switch and half-bridge topologies with hard- or soft-switching
- DC/DC converters
- Quasi-resonant flyback and Active Clamp flyback
- Totem pole and single-switch PFC
- LLC and high frequency converters
- Class-E inverters

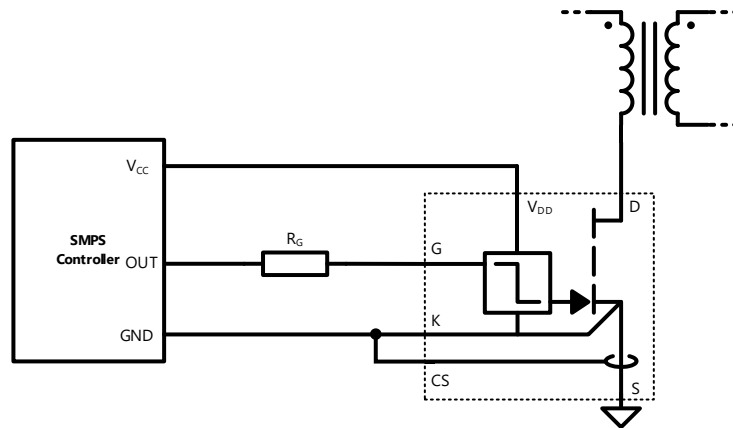
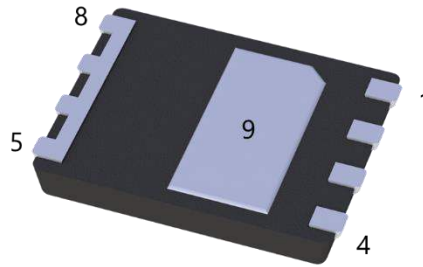


Figure 1. Exemplary Application Circuit



PIN	NAME	DESCRIPTION
1	Kelvin Source	Kelvin source connection (internally tied to power HEMT source), reference potential for gate voltage.
2	Gate	Gate signal input. Recommended gate-drive voltage: $V_{drive}$ ( $V_{GS}$ in on-state) = 9 V to $V_{DD}$ .
3	Current Sense	Current sense output, relative to source, non-isolated.
4	$V_{DD}$	ICeGaN™ gate supply voltage (recommended at 12 V), relative to source.
5-8	Drain	Power HEMT drain
9	Source	Power HEMT source, thermal pad

Figure 2. Pin Configuration and Functions

## Absolute Maximum Ratings

$T_{\text{case}} = 25\text{ °C}$  if not listed.

PARAMETER		VALUE	UNIT
Operating Junction Temperature	$T_J$	-55 to +150	°C
Storage Temperature Range	$T_S$	-55 to +150	°C
Drain-to-Source Voltage	$V_{DS}$	650	V
Drain-to-Source Voltage - transient <sup>1</sup>	$V_{DS(\text{transient})}$	750	V
Gate-to-Source Voltage	$V_{GS}$	-1 to +20 and $V_{GS} \leq V_{DD}$	V
Gate-to-Source Voltage - transient <sup>2</sup>	$V_{GS(\text{transient})}$	-1.5 to +21.5 and $V_{GS} \leq V_{DD} + 1.5$	V
Current Sense Voltage	$V_{CS}$	-1.5 to 1.5	V
ICeGaN™ Gate Supply Voltage	$V_{DD}$	0 to +20	V
Continuous Drain Current ( $T_{\text{case}} = 25\text{ °C}$ )	$I_D$	8.5	A

The recommended range of operation for  $V_{\text{drive}}$  ( $V_{GS}$  in on-state) and  $V_{DD}$  is 9 V to 20 V, enabling simple integration with a large variety of control chips and gate drivers.

Recommended maximum operating case temperature:  $T_{\text{case}} = 125\text{ °C}$ .

<sup>1</sup> Non-repetitive pulsed conditions, < 1 ms.

<sup>2</sup> Non-repetitive pulsed conditions.

## Electrical Characteristics

Values at  $T_J = 25\text{ }^\circ\text{C}$ ,  $V_{DD} = 12\text{ V}$  if not listed. To turn the device on the recommended gate voltage range is  $V_{GS} = 9\text{ V}$  to  $V_{DD}$ . To turn the device off set  $V_{GS} = 0\text{ V}$ . An integrated Miller Clamp eliminates the need for negative gate voltages.

### STATIC CHARACTERISTICS

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
Drain-to-Source Blocking Voltage	$BV_{DS}$	$V_{GS} = 0\text{ V}$ , $I_{DSS} = 5.5\text{ }\mu\text{A}$	650			V
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 12\text{ V}$ , $I_D = 0.6\text{ A}$		200	280	m $\Omega$
Drain-to-Source On Resistance	$R_{DS(on)}$	$T_J = 150\text{ }^\circ\text{C}$ $V_{GS} = 12\text{ V}$ , $I_D = 0.6\text{ A}$		530		m $\Omega$
Source-to-Drain Voltage	$V_{SD(on)}$	$V_{GS} = 0\text{ V}$ , $I_D = 0.6\text{ A}$		2.0	3.7	V
Gate-to-Source Threshold	$V_{GS(th)}$	$V_{DS} = 0.1\text{ V}$ , $I_D = 2.75\text{ mA}$	2.2	2.9	4.2	V
Gate-to-Source Threshold	$V_{GS(th)}$	$T_J = 150\text{ }^\circ\text{C}$ $V_{DS} = 0.1\text{ V}$ , $I_D = 2.75\text{ mA}$		2.6		V
Gate-to-Source Current	$I_{GS}$	$V_{GS} = 12\text{ V}$ , $V_{DS} = 0\text{ V}$		2.8	3.7	mA
Gate-to-Source Current	$I_{GS}$	$T_J = 150\text{ }^\circ\text{C}$ $V_{GS} = 12\text{ V}$ , $V_{DS} = 0\text{ V}$		2.5		mA
$V_{DD}$ current	$I_{VDD}$	$V_{GS} = 12\text{ V}$ , $V_{DS} = 0\text{ V}$		1.8	2.8	mA
$V_{DD}$ current	$I_{VDD}$	$T_J = 150\text{ }^\circ\text{C}$ $V_{GS} = 12\text{ V}$ , $V_{DS} = 0\text{ V}$		1.1		mA
Drain-to-Source Leakage Current	$I_{DSS}$	$V_{GS} = 0\text{ V}$ , $V_{DS} = 650\text{ V}$		0.1	5.5	$\mu\text{A}$
Drain-to-Source Leakage Current	$I_{DSS}$	$T_J = 150\text{ }^\circ\text{C}$ $V_{GS} = 0\text{ V}$ , $V_{DS} = 650\text{ V}$		6		$\mu\text{A}$

### DYNAMIC CHARACTERISTICS

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
Output Capacitance	$C_{OSS}$	$V_{DS} = 400\text{ V}$ , $V_{GS} = 0\text{ V}$ $f = 100\text{ kHz}$		14		pF
Output Charge	$Q_{OSS}$	$V_{DS} = 400\text{ V}$ , $V_{GS} = 0\text{ V}$		14		nC
Total Gate Charge <sup>3</sup>	$Q_G$	$V_{DS} = 400\text{ V}$ , $V_{GS} = 0\text{...}12\text{ V}$ $I_D = 2.75\text{ A}$ , $I_G = 15\text{ mA}$		1.4		nC
Reverse Recovery Charge	$Q_{RR}$	$I_S = 8\text{ A}$ , $V_{DS} = 400\text{ V}$		0		nC
Turn-on delay time	$t_{d(on)}$	See Figure 17 and Figure 18		5		ns
Turn-off delay time	$t_{d(off)}$	See Figure 17 and Figure 18		13		ns
Rise time	$t_r$	See Figure 17 and Figure 18		4		ns
Fall time	$t_f$	See Figure 17 and Figure 18		4		ns

<sup>3</sup> Turn-on gate charge value is listed. Turn-off gate charge value is lower, because ICeGaN™ gate discharges the gate internally.

### CURRENT SENSING

Please refer to the application note CG-AN2206: Current Sensing with ICeGaN™. Please contact CGD for advice on the use of the current sense function.

### ESD RATING

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
ESD withstand rating	HBM	Human Body Model (per JEDEC JS-001-2017)	2000			V

### Thermal Characteristics

Typical values unless otherwise specified.

PARAMETER		CONDITIONS	VALUE	UNIT
Thermal resistance, junction to case	$R_{th(jc)}$		2.5	°C/W
Maximum reflow soldering temperature	$T_{reflow}$	MSL 1	260	°C

**Figures**

Figures at  $T_J = 25\text{ }^\circ\text{C}$ ,  $V_{DD} = 12\text{ V}$  if not specified.

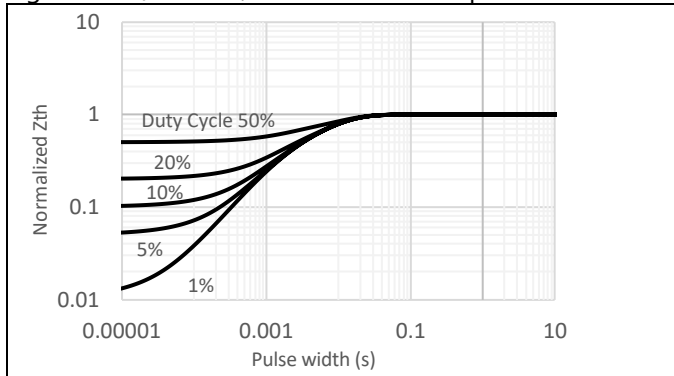


Figure 3. Normalized thermal transient impedance ( $Z_{th,Jc}$ ) as a function of pulse width.

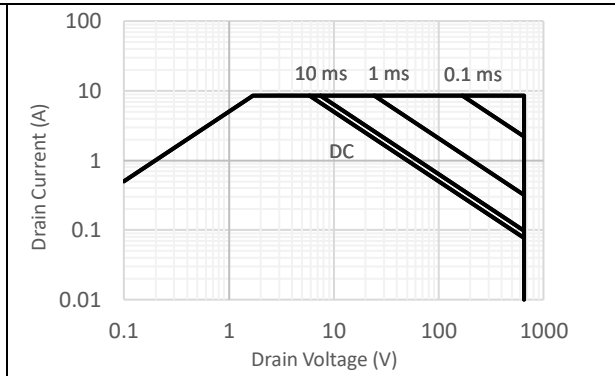


Figure 4. Safe Operating Area (SOA) based on thermal impedance  $Z_{th,Jc}$  at  $T_{CASE} = 25\text{ }^\circ\text{C}$ .

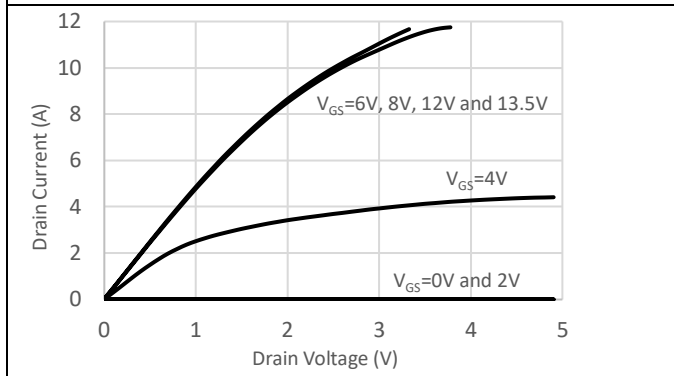


Figure 5. Forward output characteristics at  $T_J = 25\text{ }^\circ\text{C}$ .

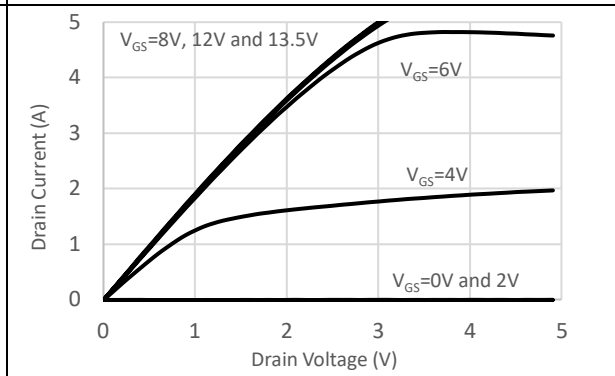


Figure 6. Forward output characteristic at  $T_J = 150\text{ }^\circ\text{C}$ .

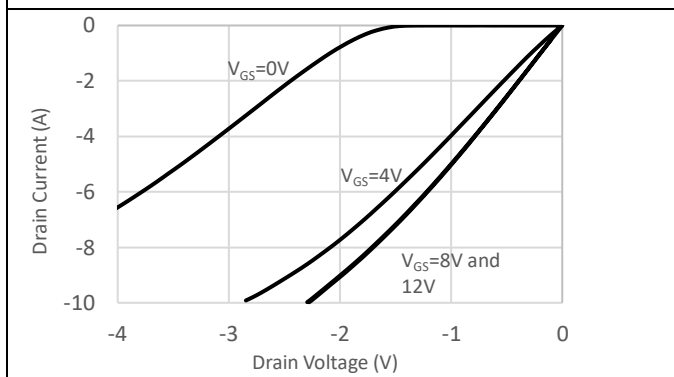


Figure 7. Reverse output characteristics at  $T_J = 25\text{ }^\circ\text{C}$ .

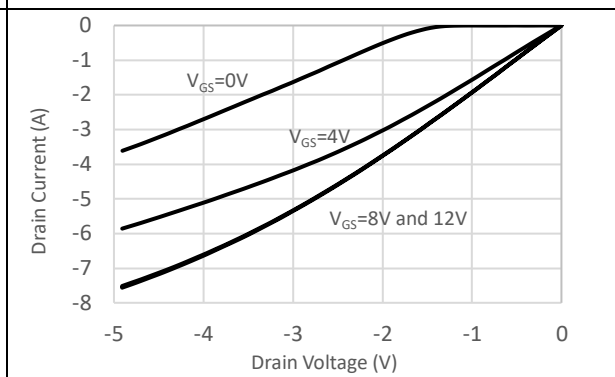


Figure 8. Reverse output characteristics at  $T_J = 150\text{ }^\circ\text{C}$ .

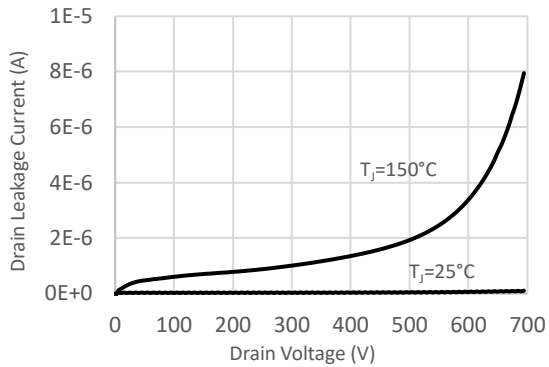


Figure 9. Drain leakage current characteristics at  $T_j = 25\text{ °C}$  and  $T_j = 150\text{ °C}$ .

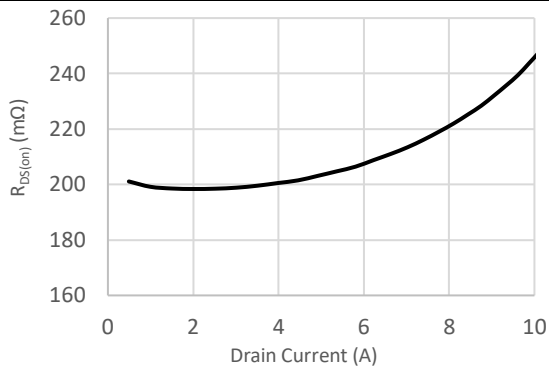


Figure 10. On-state resistance as a function of drain current at  $T_j = 25\text{ °C}$ .

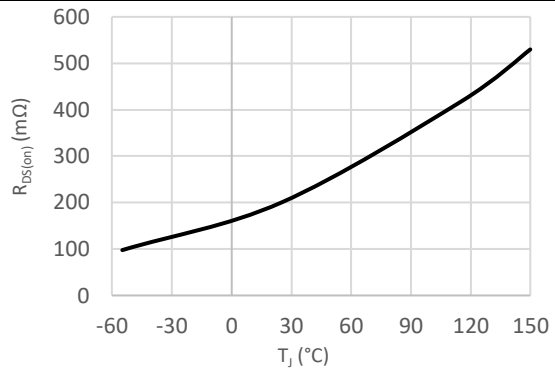


Figure 11. On-state resistance as a function of junction temperature at  $V_{GS} = 12\text{ V}$ .

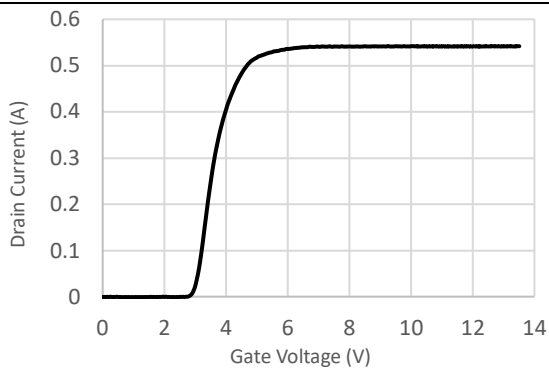


Figure 12. Transfer characteristics at  $V_{DS} = 0.1\text{ V}$ ,  $T_j = 25\text{ °C}$ .

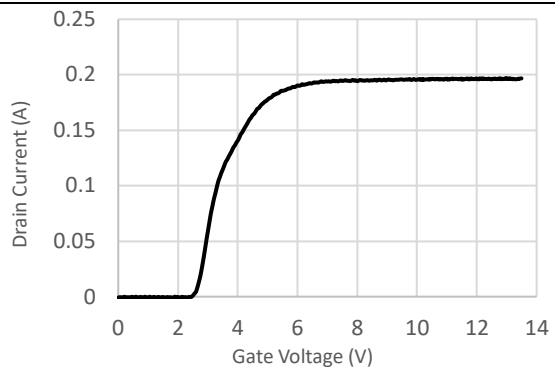


Figure 13. Transfer characteristics at  $V_{DS} = 0.1\text{ V}$ ,  $T_j = 150\text{ °C}$ .



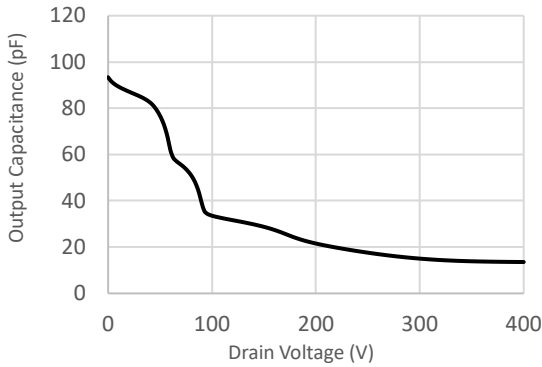


Figure 14. Typical output capacitance  $C_{OSS}$  vs.  $V_{DS}$  at 100 kHz,  $T_J = 25\text{ }^\circ\text{C}$ .

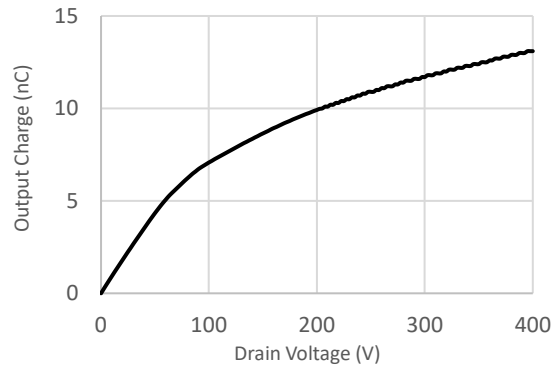


Figure 15. Typical output charge  $Q_{OSS}$  vs.  $V_{DS}$  at 100 kHz,  $T_J = 25\text{ }^\circ\text{C}$ .

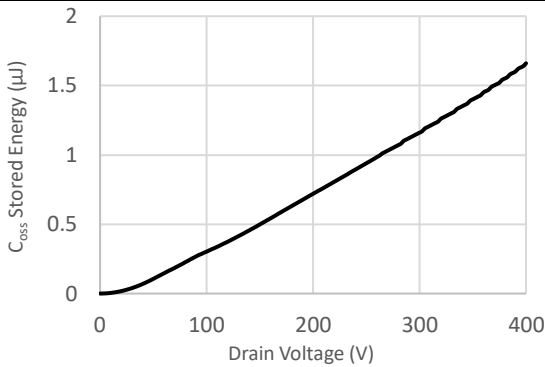


Figure 16. Typical  $C_{OSS}$  stored energy  $E_{OSS}$  vs.  $V_{DS}$  at  $T_J = 25\text{ }^\circ\text{C}$ .

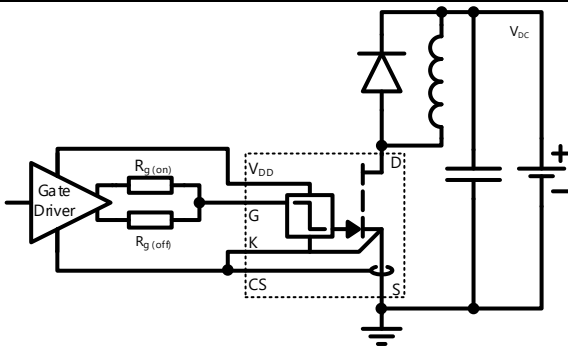


Figure 17. Inductive switching circuit.  $I_D = 6\text{ A}$ ,  $R_{g(on)} = 15\text{ }\Omega$ ,  $R_{g(off)} = 2\text{ }\Omega$ ,  $V_{DD} = 12\text{ V}$ ,  $V_{DC} = 400\text{ V}$ ,  $L = 125\text{ }\mu\text{H}$ , diode = IDH04G65C5.

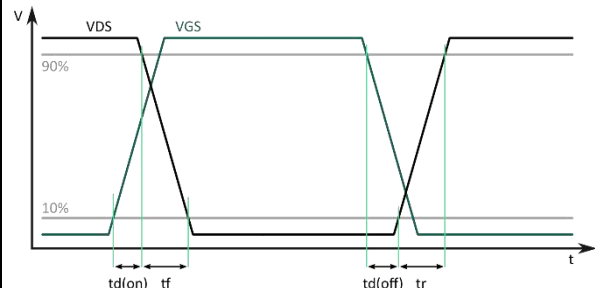
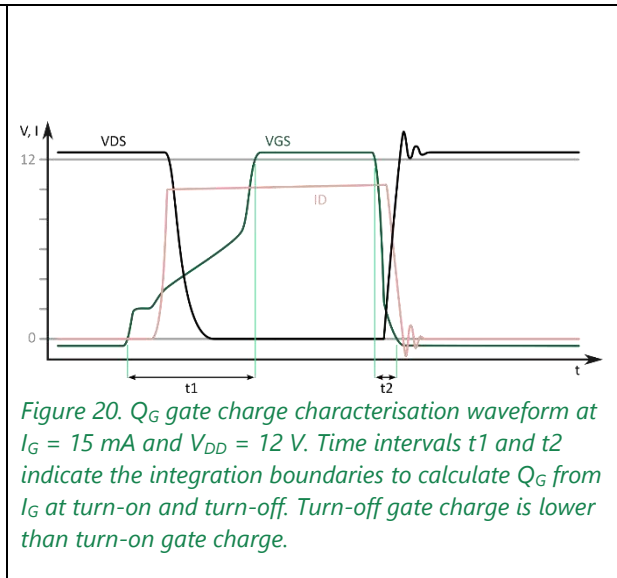
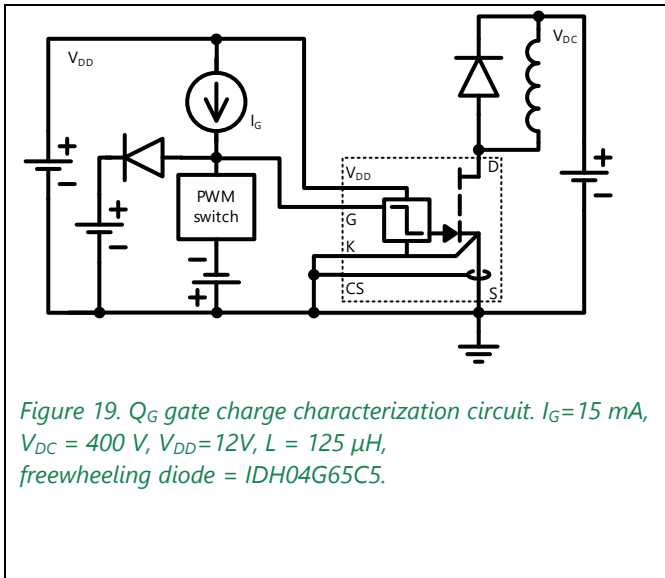


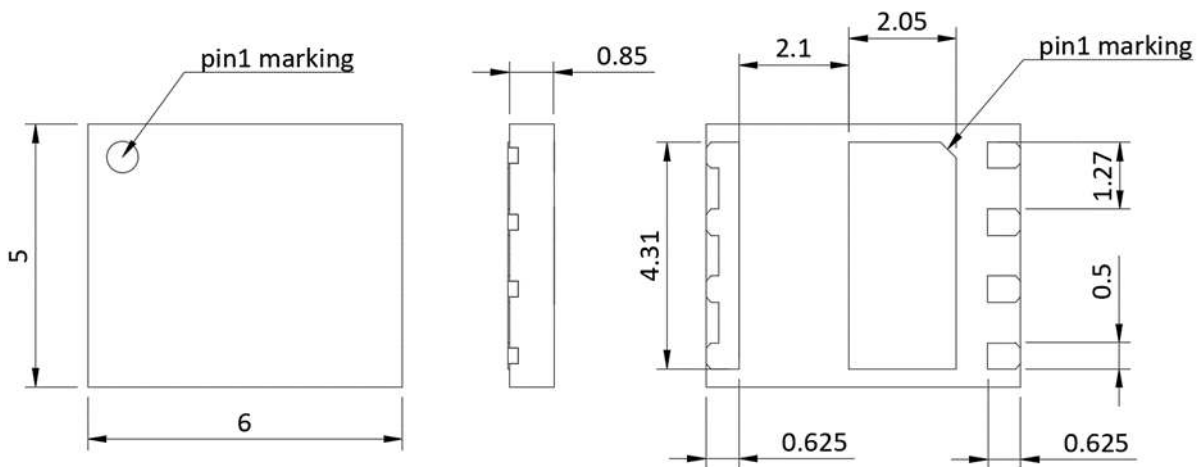
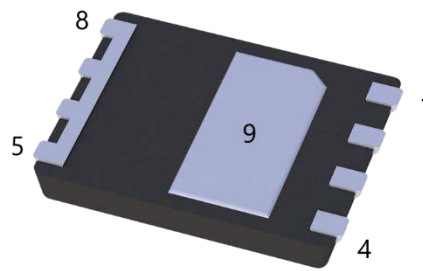
Figure 18. Switching waveform timing definitions.



## Packaging

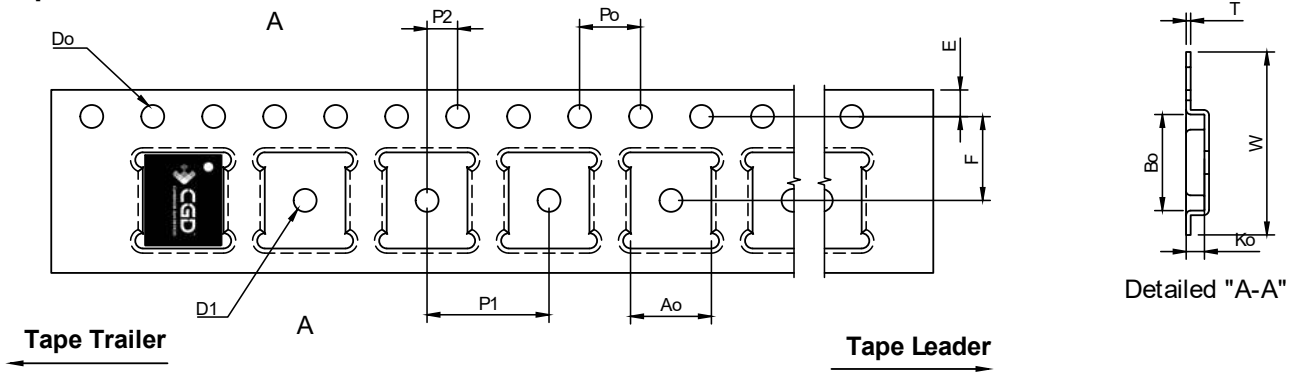
DFN 5x6 mm.

PIN NUMBER	NAME
1	Kelvin Source
2	Gate
3	Current Sense
4	V <sub>DD</sub>
5-8	Drain
9	Source



Like any unwanted electronic device, CGD components should be recycled or otherwise disposed of in accordance with local laws and regulations.

**Tape and Reel Information**

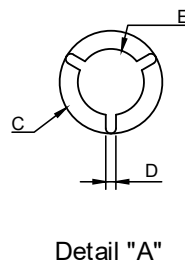
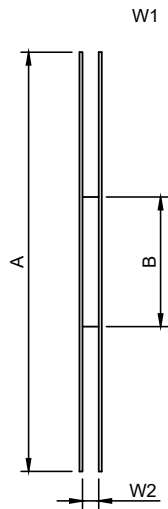
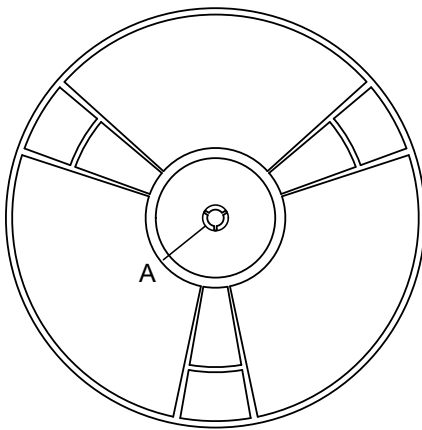


Tape Trailer - a minimum length of 160mm empty cavities sealed with cover tape.  
 Tape Leader - a minimum length of 400mm empty cavities sealed with cover tape.



Isometric View

Dimensions (mm)		
	Nominal	Tolerance
Ao	5.30	± 0.1
Bo	6.30	± 0.1
Ko	1.20	± 0.1
E	1.75	± 0.1
F	5.50	± 0.1
Po	4.0	± 0.1
P1	8.00	± 0.1
P2	2.00	± 0.1
W	12.00	± 0.3
T	0.30	± 0.05
Do	Ø1.55	± 0.05
D1	Ø1.50	+ 0.1 / - 0.0



13" Reel Dimensions (mm)		
	Min	Max
W1		18.2
W2	12.3	13.1
A	328.0	332.0
B	100.0	104.0
C	20.2	
D	1.5	2.5
E	12.8	13.5

**Version History**

This version is 1.0

VERSION	DESCRIPTION	DATE	BY
1.0	Initial Release	December 2022	MA, AB, JZ

*Dare to innovate differently*



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