

Notes:

1. Allow clearance for finger squeeze access from the two sides shown.

2. No tracks or vias in the shaded "KEEP OUT" AREA.

3. No other track or signal within .02" of any contact pad.

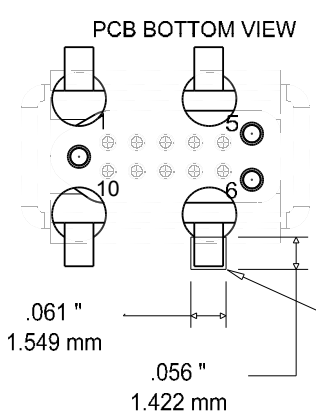
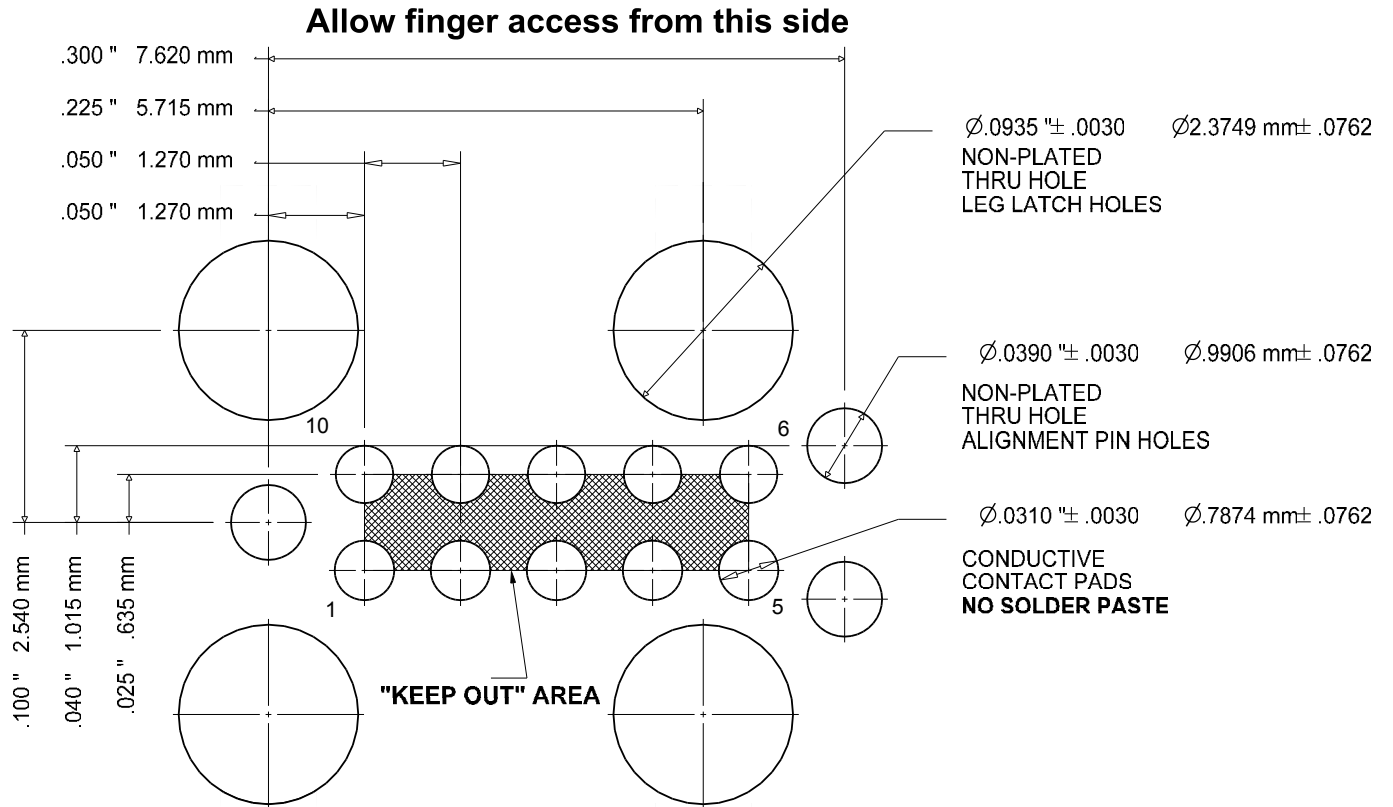
4. Do not allow solder paste on the contact pads. It is essential to eliminate any hole in the solder paste-mask (solder stencil) layer. If this is not possible make the contact pads thru-hole with a finished hole size of .008" or less.

5. Leg and alignment holes may be plated and used as vias but ensure minimum finished hole size meets specified tolerances.

6. To prevent purchasing confusion, please specify DNL in your BOM.

FOOTPRINT FOR TC2050-IDC PLUG-OF-NAILS™ CABLE

ZONE	A	TC2050-IDC-FP	12/2/10	MS
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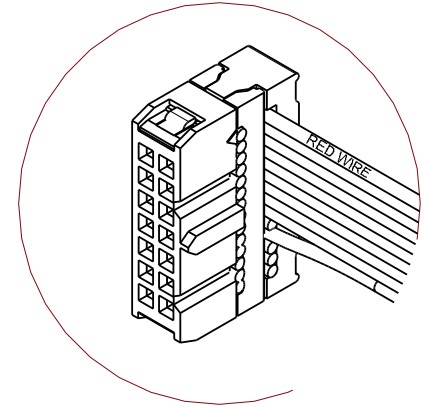
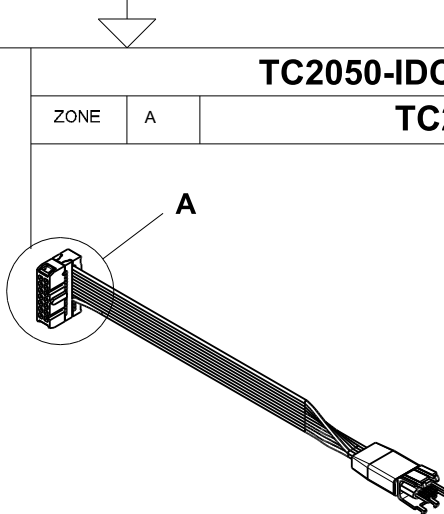
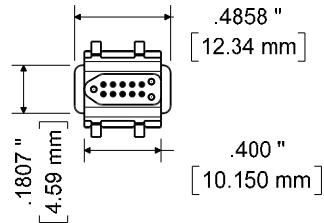
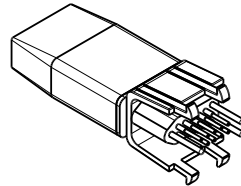
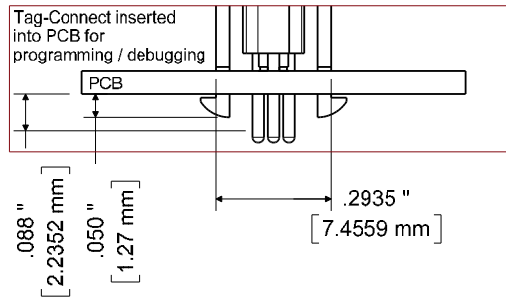
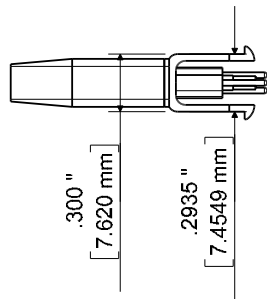
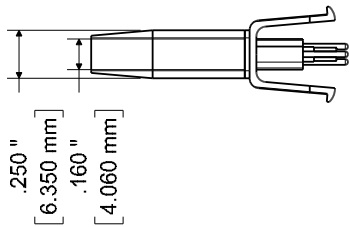
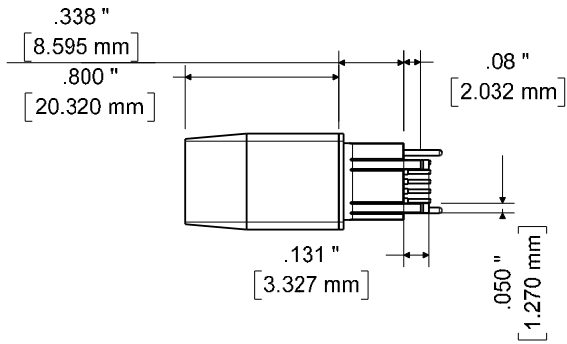
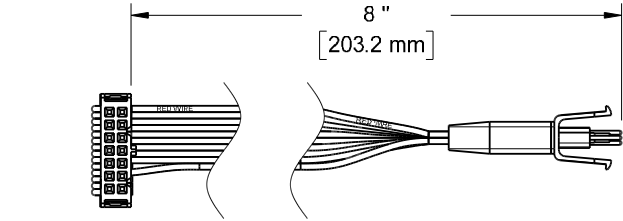


ALLOW A .061 x .056 SQUARE AREA OF CLEARANCE FOR EACH FOOT

SIZE A	FSCM NO.	DWG NO. FOOTPRINT FOR TC2050-IDC-FP	REV A
SCALE 7:1	www.TAG-CONNECT.com	SHEET 1 of 3	

NOTE:
Dimensions subject to change

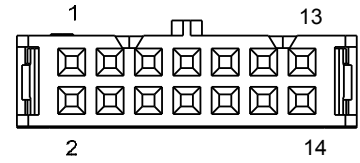
For use with TI MSP-FET and compatible MSP430 JTAG debuggers



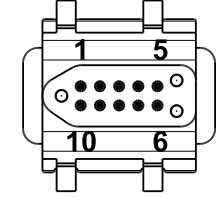
Detail A

ZONE		A	TC2050-IDC-430	11/26/10	MS
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END VIEW
2x7 0.1" PITCH
IDC CONNECTOR



END VIEW
10 PIN
TAG-CONNECT



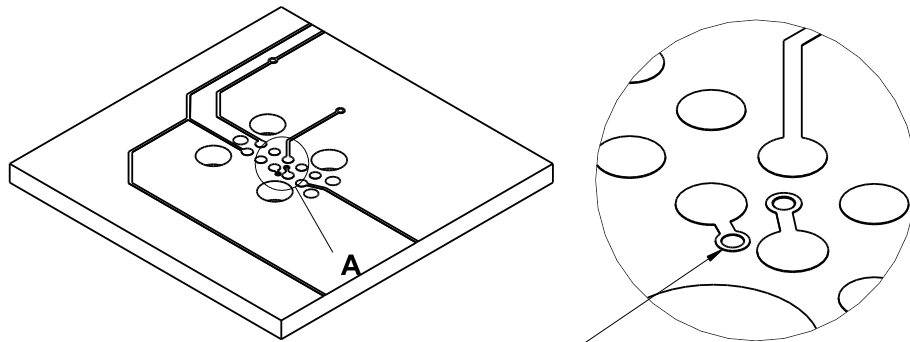
14 pin IDC	10 pin TAG
1	1
2	2
3	3
4	4
5	5

14 pin IDC	10 pin TAG
6	6
7	7
8	8
9	9
11	10

NOTE:
Pins 10,12,13 & 14 are not used

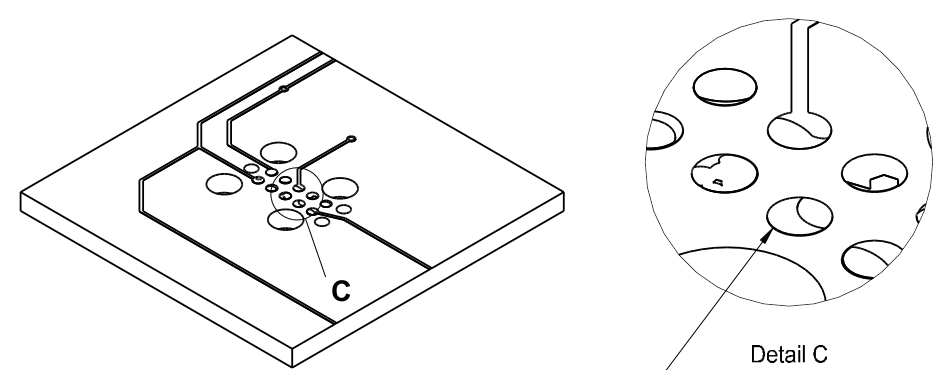
SIZE A	FSCM NO.	DWG NO. TC2050-IDC-430	REV A
SCALE	www.TAG-CONNECT.com		SHEET 2 of 3

Layout Problems to Avoid



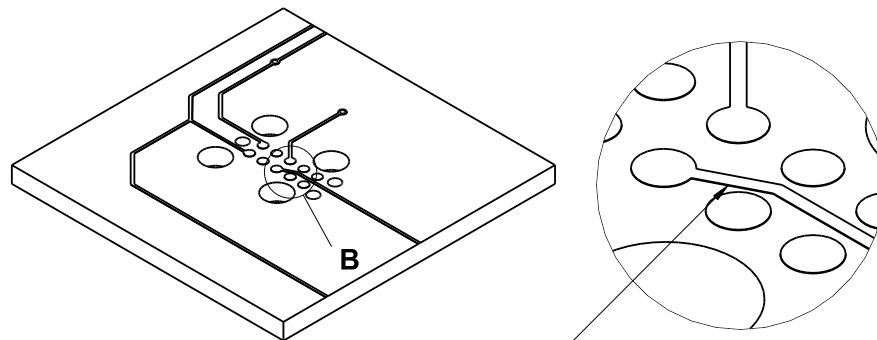
Detail A

Vias between contact pads



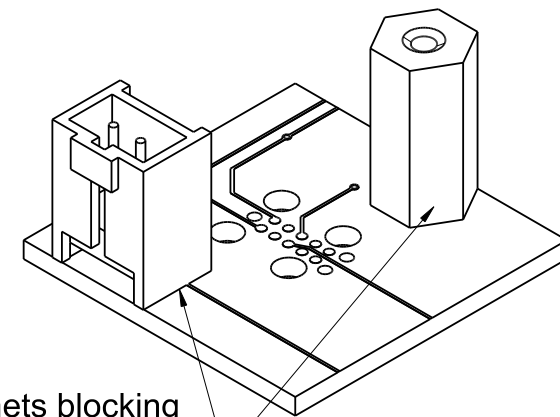
Detail C

Do not deposit solder paste on contact pads. View Solder Paste Mask (Solder Stencil) layer in pad-stack and eliminate any hole.



Detail B

Traces less than .02" away from contact pad or in "KEEP OUT" area



Large componets blocking finger access to the Tag-Connect leg clips