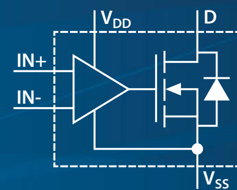
EPC21603 – 40 V, 15 A Peak, eToF™ Laser Driver IC

PRELIMINARY



EFFICIENT POWER CONVERSION

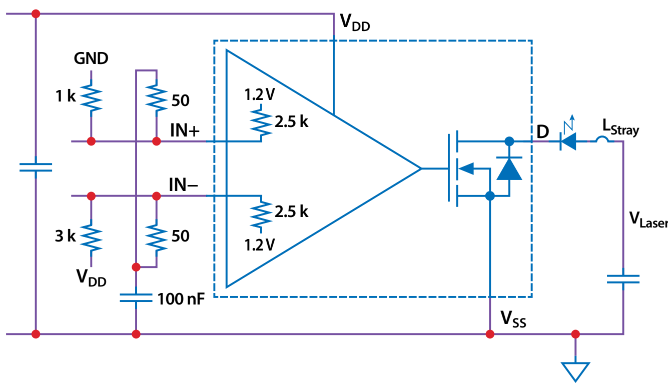
RoHS Halogen-Free

The EPC21603 is a laser driver that is controlled using LVDS logic at high frequencies of up to 100 MHz to modulate laser driving currents of up to 15 Amps. Full driver integration is achieved using EPC's proprietary GaN IC technology.

Wafer-level chip-scale packaging is used resulting in a BGA package that measures only 1.5 x 1 mm. The BGA package has low inductance and lays out very well with the laser system.

The EPC21603 uses a 5 V logic supply and is capable of interfacing to digital controllers. It can switch at frequencies exceeding 100 MHz.

Figure 1: Typical Connection Diagram



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to V_{SS} unless indicated otherwise.

Symbol	Definition	MIN	MAX	UNIT
V_D	Drain Voltage		40	V
V_{DD}	Low Side Supply Voltage (V_{DD} to GND)	-0.3	5.5	
IN	Logic Input	-0.3	5	
I_D	Average Drain Current		1.7	A
T_J	Junction Temperature	-40	125	°C
T_{STG}	Storage Temperature	-40	150	

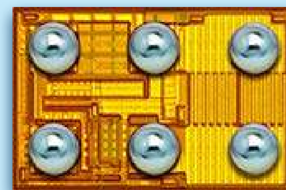
ESD Ratings

(Testing performed at EAG Lab. Need to get the relevant JEDEC specs for ESD ratings)

Symbol	Definition	MIN	UNIT
HBW	Human-body model	+/-250	V
CDM	Charged-device model	n/a	

Thermal Characteristics

Symbol	Definition	MIN	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	5.7	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	23	
$R_{\theta JA\_JEDEC}$	Thermal Resistance, Junction-to-Ambient (using JEDEC 51-2 PCB)	130	
$R_{\theta JA\_EVB}$	Thermal Resistance, Junction-to-Ambient (using EPC9156 EVB)	120	



Die size: 1.5 x 1 mm

EPC21603 eGaN® FETs are supplied in passivated die form with solder bumps.

Features

- V_{Laser} operating range up to 30 V
- 15 Amp peak current
- Switching frequency greater than 100 MHz
- Typical voltage switching time 750 ps
- 5 V nominal logic power supply
- LVDS logic compatible input control
- 1.7 ns minimum output pulse width
- 4 ns delay time from input to output

Applications

- Time of flight measurement
  - Gesture recognition
  - Gaming
  - Driver monitoring
  - Robotic vision
  - Industrial safety
- ToF module using VCEL laser for camera modules, laptops and smart phones

Scan QR code or click link below for more information including reliability reports, device models, demo boards!

https://l.ead.me/EPC21603

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to V_{SS} unless indicated otherwise.

Symbol	Definition	MIN	TYP	MAX	UNIT
V_{Laser}	Laser Driver Voltage[5]	5		30	V
V_{DD}	Logic Supply Voltage[5]		5		V

Truth Table

IN	Laser
V(IN+) ≤ V(IN-), V_{CM} = 1.2 V	Off
V(IN+) > V(IN-), V_{CM} = 1.2 V	On

Electrical Characteristics

All ratings at T_J = 25 ˚C. V_{Laser} = 20 V, I_D = 10 A, V_{DD} = 5 V, V_{CM} = 1.2 V, ΔV_{IN} = ±350 mV unless indicated otherwise.

Symbol	Definition	MIN	TYP	MAX	UNIT
Operating Power Supply, V_{DD}					
$I_{DD\ (Off)}$	V_{DD} Quiescent current with laser driver off		10	16	mA
$I_{DD\ (30\ MHz)}$	Operating current off V_{DD}		50		mA
Input Pins					
V_C[1]	Common mode voltage	0.8	1.2	1.4	V
R_{IN}	Input pulldown resistance		5.5		kΩ
V_{ITH+}	Positive-going differential input voltage			200	mV
V_{ITH-}	Negative-going differential input voltage	-200			mV
Power Stage					
$R_{DS(on)}$[1]	Drain to Source Resistance		40		mΩ
$I_{D(peak)}$[1]	Peak Laser Drive Current Capability, f = 50 MHz	15			A
C_{OSS}[1]	V_{DS} = 20 V, V_{IN} = 0 V		49		pF
Q_{OSS}[1]	V_{DS} = 20 V, V_{IN} = 0 V		1.5		nC
E_{OSS}[1]	V_{DS} = 20 V, V_{IN} = 0 V		13		nJ
$C_{OSS(ER)}$[1,2]	V_{DS} = 0 to 20 V, V_{IN} = 0 V		63		pF
$C_{OSS(TR)}$[1,3]	V_{DS} = 0 to 20 V, V_{IN} = 0 V		73		pF
Dynamic Characteristics					
$t_{D(on)}$[1]	Turn on delay time		4.0	5.0	ns
t_F[1]	Drain fall time		0.78	1.2	ns
$t_{D(off)}$[1]	Turn off delay time		3.4	4.0	ns
t_R[1,4]	Drain rise time		0.32		ns
t_{dPW}[1]	Pulse width distortion	-2.0	-0.7	0.7	ns
$t_{in(min(on))}$[1]	Minimum input pulse width		2.5		ns
$t_{On(Max)}$[1]	Minimum drain pulse width		1.7		ns
$t_{Off(Max)}$[1]	Maximum on time		500		ns
f_{Max}[1]	Maximum frequency, 0 °C to 100 °C		100		mHz

Pinout Description

Pin	Description
V_{DD}	Input Voltage Supply (Decouple to GND with small, low inductance capacitor)
IN+	Differential (LVDS) non-inverting input
IN–	Differential (LVDS) inverting input
D	Power Drain
V_{SS}	Power Source and Signal Return, Internally Connected to Substrate

Notes:

1. Guaranteed by design, but not tested
2. $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}
3. $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}
4. Drain rise time is determined by ZVS charging of the output capacitance
5. See Power Sequencing section in Applications Information for considerations on laser drive voltage
6. Paragraph 2.7 of AEC Q100-011 Rev. D, Jan. 29, 2019 states that CDM specification is not necessary on such a small device.

Performance Curves

Figure 2: Typical Operating Current vs. Frequency

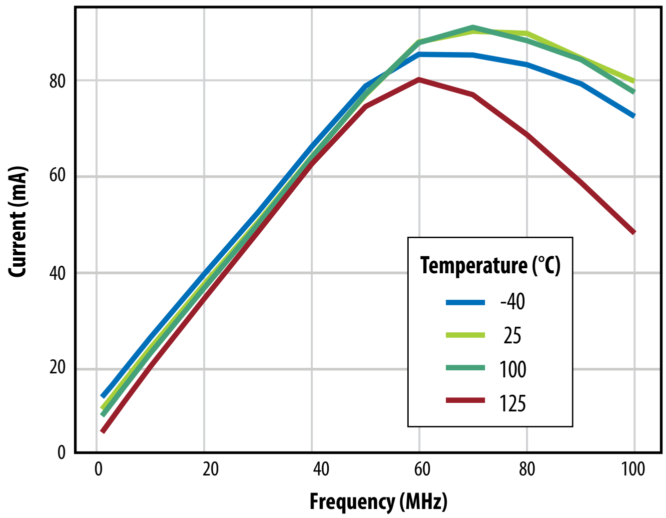


Figure 3: Typical Quiescent Current vs. Temperature

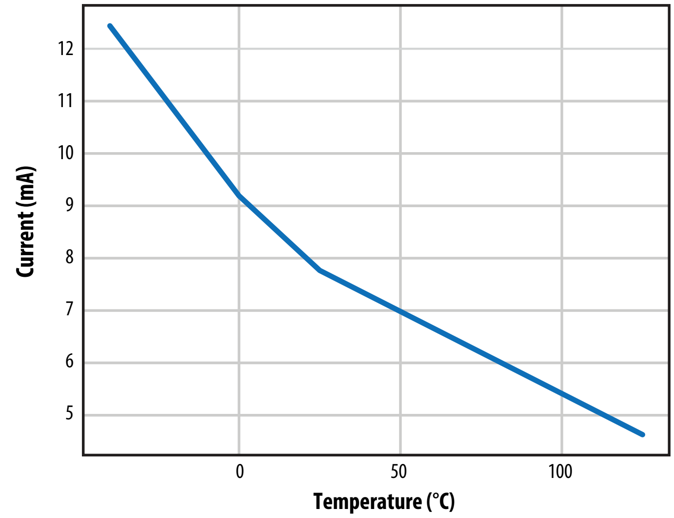


Figure 4: Turn On Propagation Delay vs. Temperature

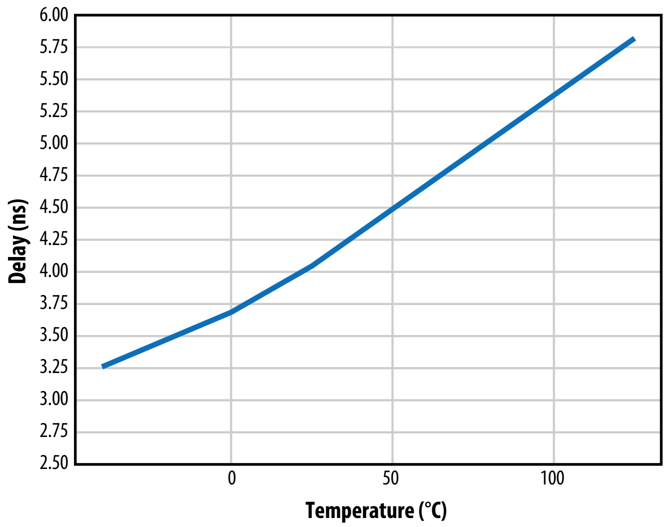


Figure 5: Turn Off Propagation Delay vs. Temperature

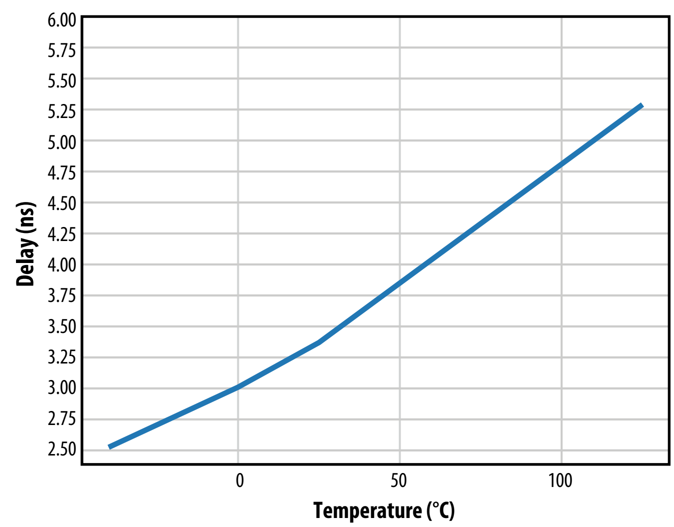


Figure 6: Typical C_{OSS}

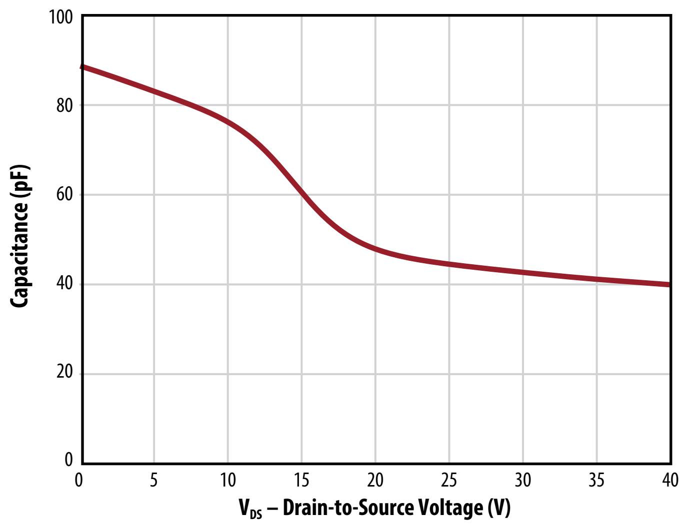


Figure 7: Typical Output Charge and C_{OSS} Stored Energy

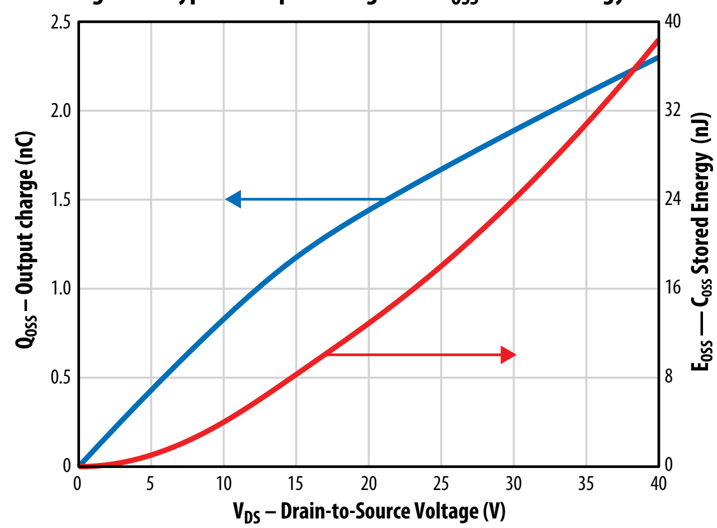
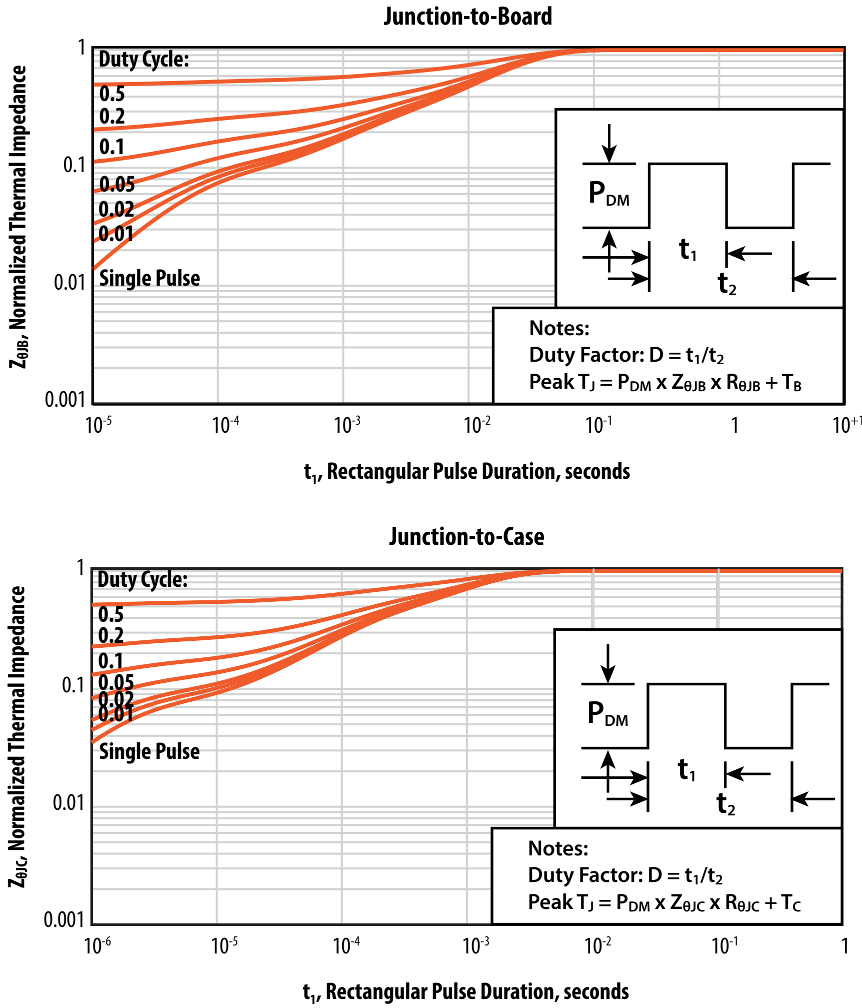


Figure 8: Transient Thermal Impedance



Application Information

Safety Warning

This device is capable of driving laser diodes to generate high power optical pulses. Such pulses are capable of causing **PERMANENT VISION DAMAGE AND BLINDNESS** as well as additional injury or property damage. Laser diodes may emit infrared (IR) light that is invisible to the user, but which can still cause **PERMANENT VISION DAMAGE AND BLINDNESS** as well as additional injury or property damage. User is fully responsible for following proper laser safety procedures to prevent injury or damage.

Power Sequencing

IN **must** be held low during power up sequence. For power up, V_{DD} must be applied before applying voltage to the drain to prevent possible unwanted turn on of the output. For power down, the order must be reversed.

Power Up	IN	V_{DD}	Drain
1	Off, V_{CM} = 0 V	0 V	0 V
2	Off, V_{CM} = 1.2 V	5 V	0 V
3	Off, V_{CM} = 1.2 V	5 V	$V_{Laser\ Drive}$
4	On, V_{CM} = 1.2 V	5 V	$V_{Laser\ Drive}$
Power Down	**IN**	**V_{DD}**	**Drain**
1	Off, V_{CM} = 1.2 V	5 V	$V_{Laser\ Drive}$
2	Off, V_{CM} = 1.2 V	5 V	0 V
3	Off, V_{CM} = 0 V	0 V	0 V

Application Information *(continued)*

Layout and decoupling

Minimizing inductance in both power and gate drive loops is critical. The power loop is primary, and gate drive loop secondary. Short, wide traces are required, and returning in the second layer, using a thin dielectric will cancel much of the inductance. Using multiple ceramic capacitors in parallel will reduce stray inductance and impedance in the power loop. Use high quality NPO or COG capacitors for both power and gate drive. This will increase effective capacitance as capacitors with lower quality materials will lose much more capacitance with voltage. Recommended layout is shown below. Component recommendations for power and gate drive decoupling capacitors are shown in the **EPC9156 demonstration board quick start guide**.

Turn off current is limited by the energy of the power loop stray inductance transferring to the C_{OSS} of the power FET of the laser driver. E_{OSS} vs. V_{DS} curve is in the datasheet.

Start up

V_{DD} should be applied before the laser voltage. For applications where the laser voltage is below 10 V and at elevated temperatures, it may take a few pulses before the pulse width stabilizes.

Input logic

LVDS inputs are used with each input internally pulled to 1.2 V with 2.5 kΩ. For safety IN+ should be pulled to ground with 1 kΩ and IN- should be pulled to V_{DD} with 3 kΩ.

Output Capacitance

Output capacitance (C_{OSS}) is the capacitance between drain and ground. Output charge (Q_{OSS}) is the integral of output capacitance over voltage. Just like discrete power FETs, output capacitance is charged and discharged with each cycle. This takes time and dissipates power. Please refer to FET application notes to determine impact.

Figure 9: Power and Gate Drive Turn On Loops

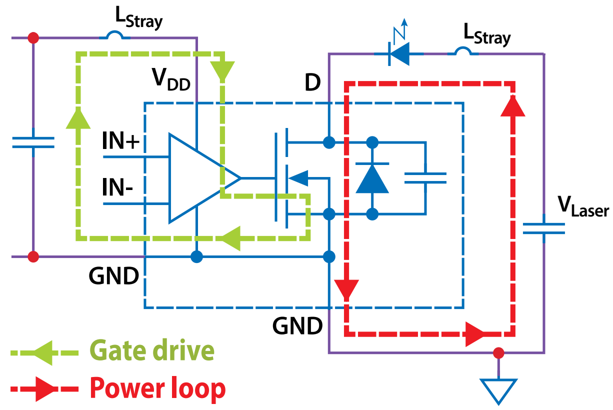


Figure 10: Recommended Layout

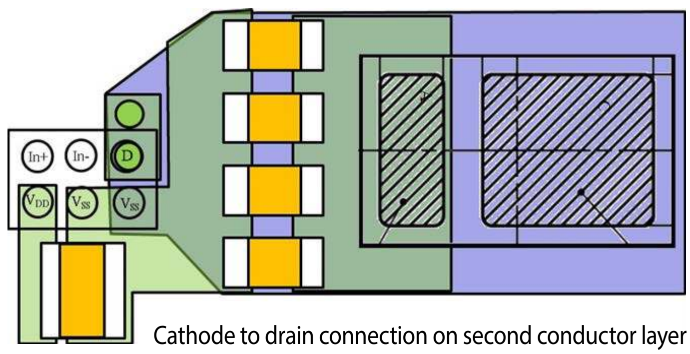


Figure 11: Parameter Measurement Test Circuits

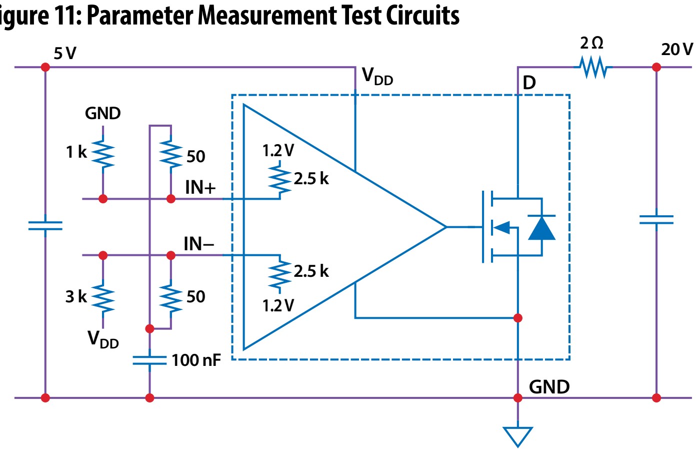
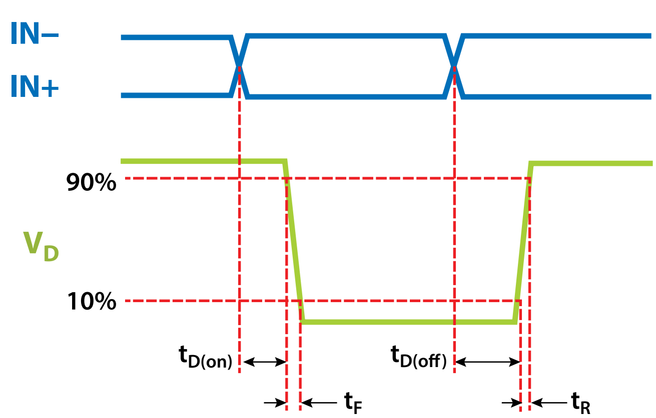


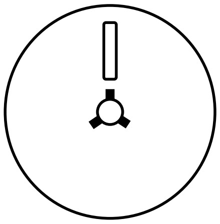
Figure 12: Parameter Measurement Definitions

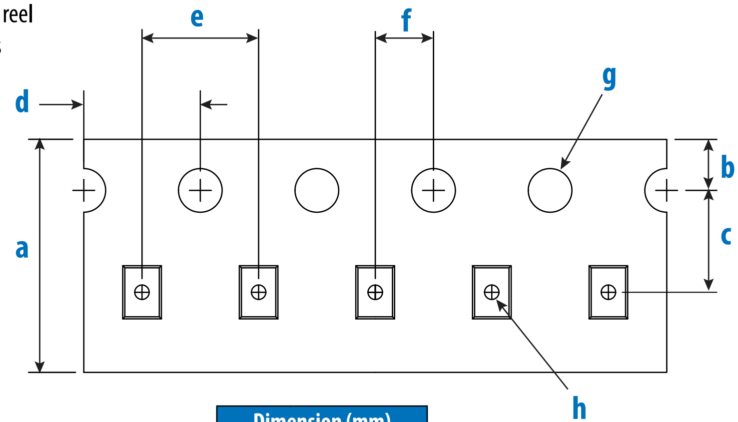


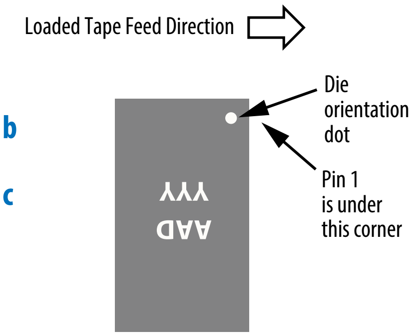
TAPE AND REEL CONFIGURATION

- 4 mm pitch, 8 mm wide tape on 7″ reel
- Standard reel packages 2,500 units

7″ inch reel







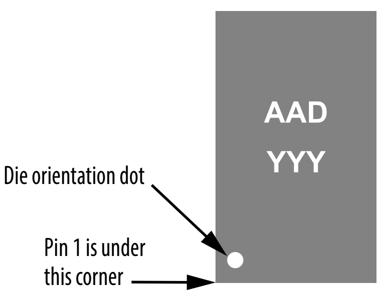
Die is placed into pocket solder bump side down (face side down)

	Dimension (mm)		
EPC21603 (Note 1)	**Target**	**MIN**	**MAX**
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (Note 2)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (Note 2)	2.00	1.95	2.05
g	1.50	1.50	1.60
h	0.50	0.45	0.55

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

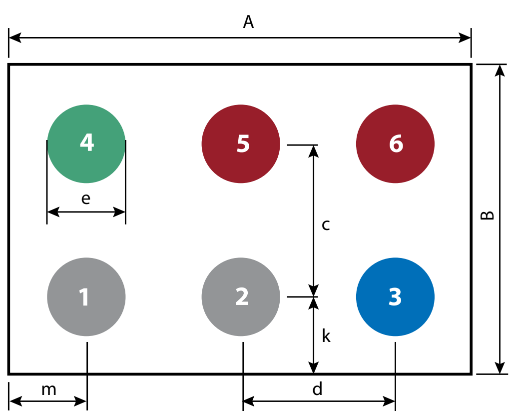
DIE MARKINGS



Part Number	Laser Markings	
	Lot_Date Code Marking Line 1	**Lot_Date Code Marking Line 2**
EPC21603	AAD	YYY

DIE OUTLINE

Solder Bump View



DIM	MICROMETERS		
	MIN	**Nominal**	**MAX**
A	1420	1450	1480
B	920	950	980
c		500	
d		500	
e	238	264	290
k		225	
m		225	

Pad 1 is IN+

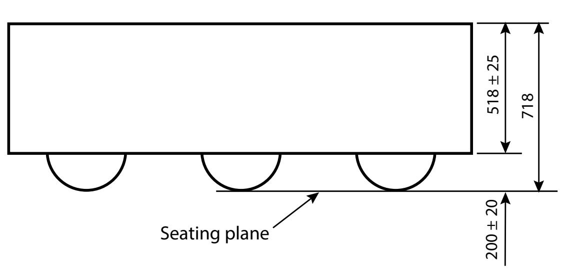
Pad 2 is IN–

Pad 3 is Drain

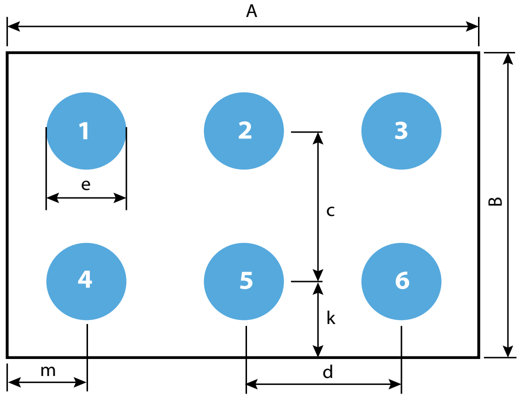
Pad 4 is V_{DD}

Pads 5 & 6 are Source

Side View



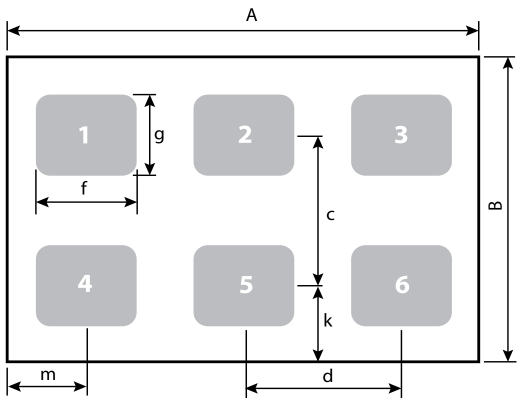
RECOMMENDED LAND PATTERN
(units in µm)



DIM	MICROMETERS
A	1450
B	950
c	500
d	500
e	230
k	225
m	225

Pad 1 is IN+
Pad 2 is IN–
Pad 3 is Drain
Pad 4 is V_{DD}
Pads 5 & 6 are Source

RECOMMENDED STENCIL DRAWING
(measurements in µm)



DIM	MICROMETERS
A	1450
B	950
c	500
d	500
f	300
g	250
k	225
m	225

Recommended stencil should be 4mil (100 µm) thick, must be laser cut, opening per drawing.

The corner has a radius of R60

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Additional assembly resources available at
https://epc-co.com/epc/design-support/assemblybasics