FAIRCHILD SEMICONDUCTOR®

August 2003

FDH15N50 / FDP15N50 / FDB15N50

15A, 500V, 0.38 Ohm, N-Channel SMPS Power MOSFET

Applications

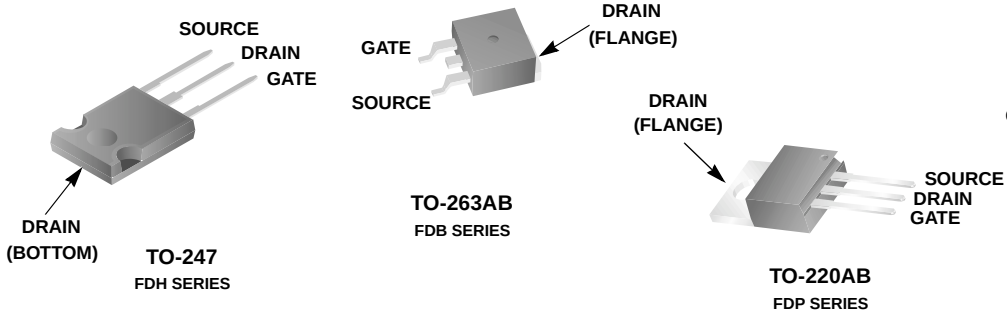
Switch Mode Power Supplies(SMPS), such as

- PFC Boost
- Two-Switch Forward Converter
- Single Switch Forward Converter
- Flyback Converter
- Buck Converter
- High Speed Switching

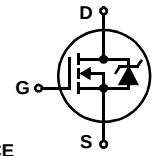
Features

- Low Gate Charge Q_g results in Simple Drive Requirement
- Improved Gate, Avalanche and High Reapplied dv/dt Ruggedness
- Reduced $r_{DS(ON)}$
- Reduced Miller Capacitance and Low Input Capacitance
- Improved Switching Speed with Low EMI
- 175°C Rated Junction Temperature

Package



Symbol



Absolute Maximum Ratings $T_C = 25^oC$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	500	V
V_{GS}	Gate to Source Voltage	±30	V
I_D	Drain Current Continuous ($T_C = 25^oC$, $V_{GS} = 10V$)	15	A
	Continuous ($T_C = 100^oC$, $V_{GS} = 10V$)	11	A
	Pulsed[1]	60	A
P_D	Power dissipation Derate above 25^oC	300 2	W $W/^oC$
T_J, T_{STG}	Operating and Storage Temperature	-55 to 175	^oC
	Soldering Temperature for 10 seconds	300 (1.6mm from case)	^oC

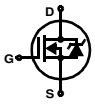
Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance Junction to Case	0.50	$^oC/W$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (TO-247)	40	$^oC/W$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (TO-220, TO-263)	62	$^oC/W$

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDH15N50	FDH15N50	TO-247	Tube	-	30
FDP15N50	FDP15N50	TO-220	Tube	-	50
FDB15N50	FDB15N50	TO-263	330mm	24mm	800

Electrical Characteristics T_J = 25°C (unless otherwise noted)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
Statics							
B_{VDSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V		500	-	-	V
$\Delta B_{VDSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	Reference to 25°C, ID = 1mA		-	0.58	-	V/°C
$r_{DS(ON)}$	Drain to Source On-Resistance	V_{GS} = 10V, I_D = 7.5A		-	0.33	0.38	Ω
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA		2.0	3.4	4.0	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 500V	T_C = 25°C	-	-	25	μA
		V_{GS} = 0V	T_C = 150°C	-	-	250	
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±30V		-	-	±100	nA
Dynamics							
g_{fs}	Forward Transconductance	V_{DD} = 10V, I_D = 7.5A		10	-	-	S
$Q_{g(TOT)}$	Total Gate Charge at 10V	V_{GS} = 10V, V_{DS} = 400V, I_D = 15A		-	33	41	nC
Q_{gs}	Gate to Source Gate Charge			-	7.2	10	nC
Q_{gd}	Gate to Drain “Miller” Charge			-	12	16	nC
$t_{d(ON)}$	Turn-On Delay Time	V_{DD} = 250V, I_D = 15A, R_G = 6.2Ω, R_D = 17Ω		-	9	-	ns
t_r	Rise Time			-	5.4	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time			-	26	-	ns
t_f	Fall Time			-	5	-	ns
C_{ISS}	Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz		-	1850	-	pF
C_{OSS}	Output Capacitance			-	230	-	pF
C_{RSS}	Reverse Transfer Capacitance			-	16	-	pF
Avalanche Characteristics							
E_{AS}	Single Pulse Avalanche Energy[2]			760	-	-	mJ
I_{AR}	Avalanche Current			-	-	15	A
Drain-Source Diode Characteristics							
I_S	Continuous Source Current (Body Diode)	MOSFET symbol showing the integral reverse p-n junction diode. 		-	-	15	A
I_{SM}	Pulsed Source Current[1] (Body Diode)			-	-	60	A
V_{SD}	Source to Drain Diode Voltage	I_{SD} = 15A		-	0.86	1.2	V
t_{rr}	Reverse Recovery Time	I_{SD} = 15A, di_{SD}/dt = 100A/μs		-	470	730	ns
Q_{RR}	Reverse Recovered Charge	I_{SD} = 15A, di_{SD}/dt = 100A/μs		-	5	6.6	μC

Notes:
1: Repetitive rating; pulse width limited by maximum junction temperature
2: Starting T_J = 25°C, L = 7.0mH, I_{AS} = 15A

Typical Characteristics

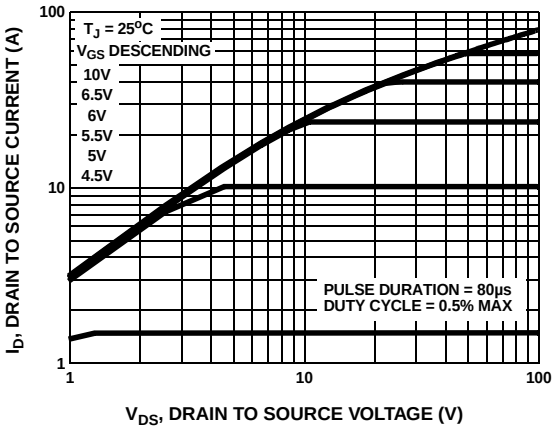


Figure 1. Output Characteristics

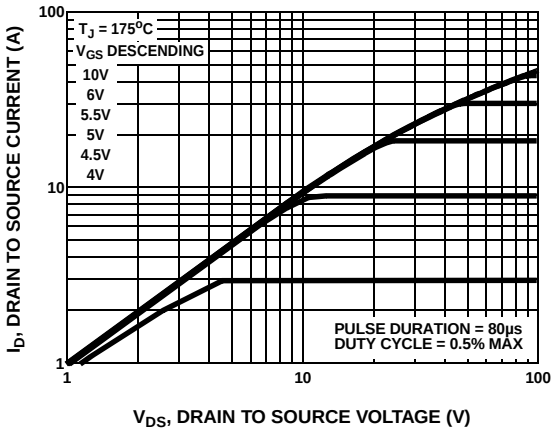


Figure 2. Output Characteristics

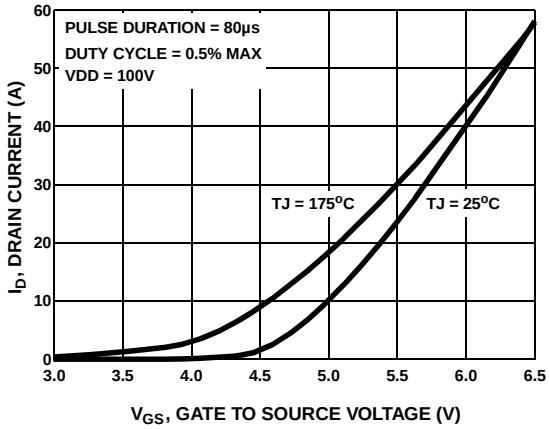


Figure 3. Transfer Characteristics

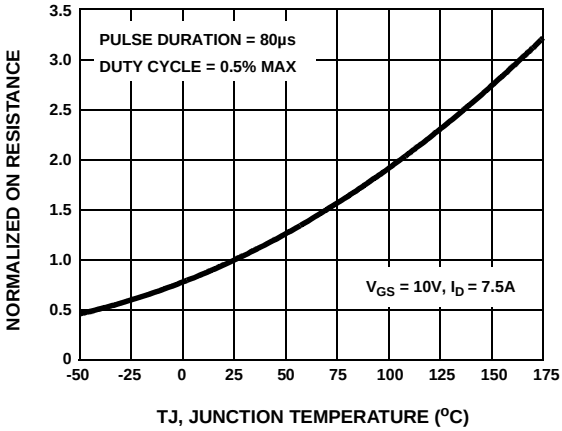


Figure 4. Normalized Drain To Source On Resistance vs Junction Temperature

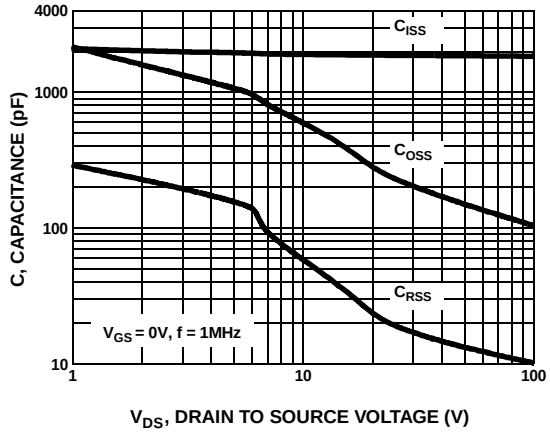


Figure 5. Capacitance vs Drain To Source Voltage

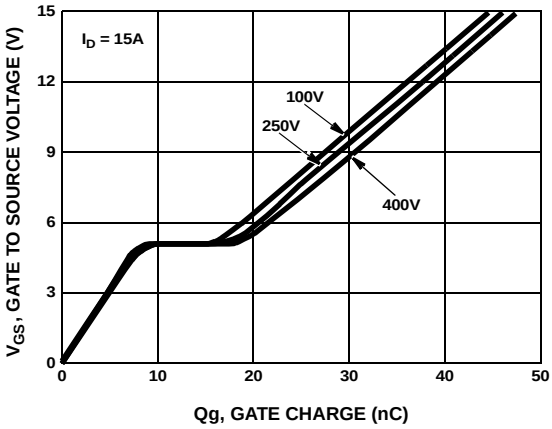


Figure 6. Gate Charge Waveforms For Constant Gate Current

Typical Characteristics

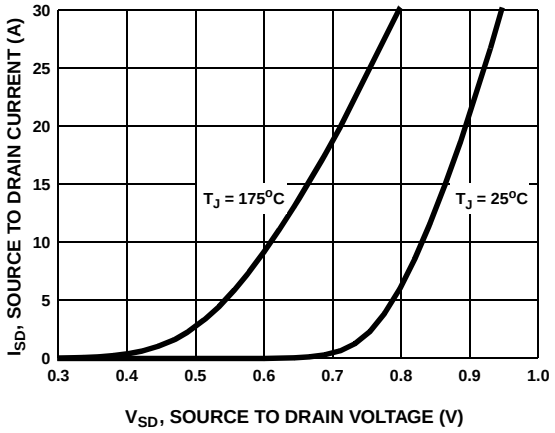


Figure 7. Body Diode Forward Voltage vs Body Diode Current

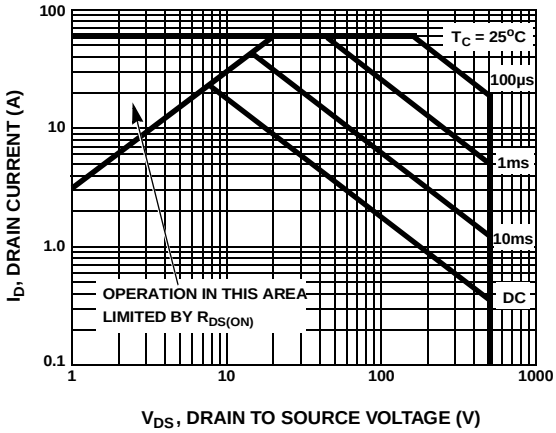


Figure 8. Maximum Safe Operating Area

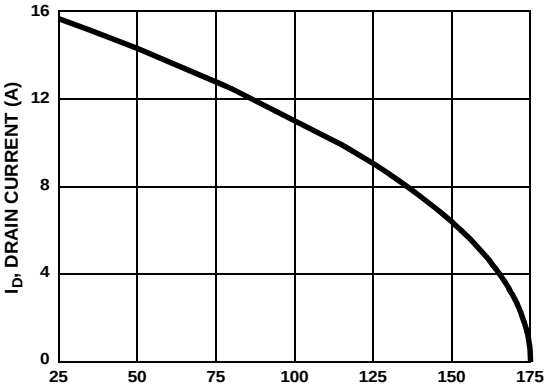


Figure 9. Maximum Drain Current vs Case Temperature

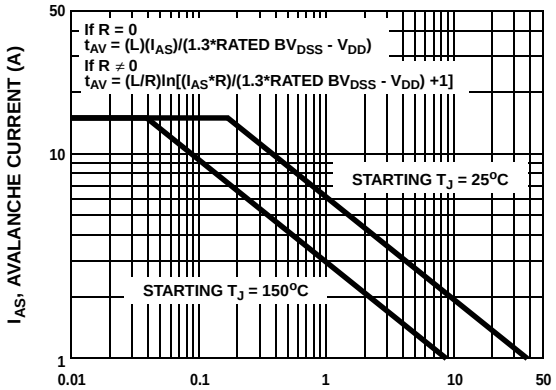


Figure 10. Unclamped Inductive Switching Capability

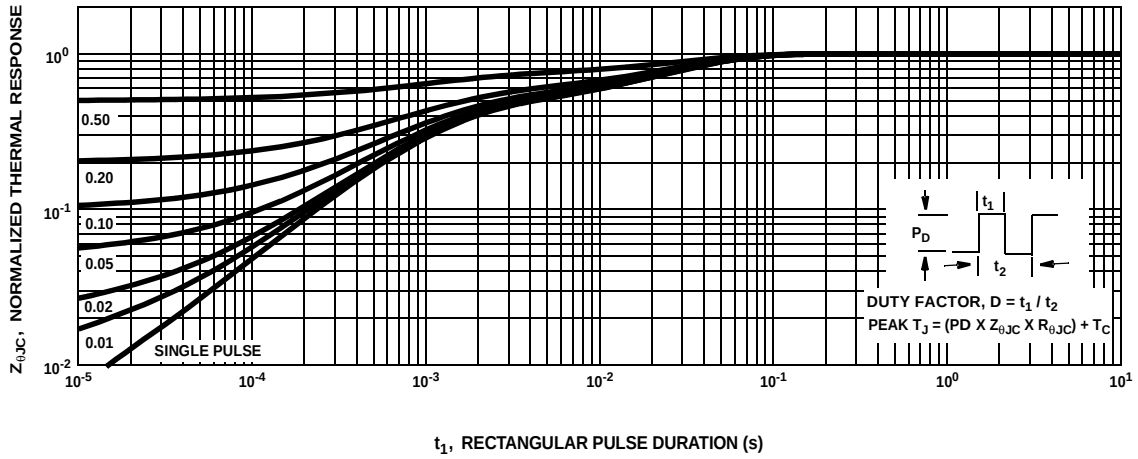


Figure 11. Normalized Transient Thermal Impedance, Junction to Case

Test Circuits and Waveforms

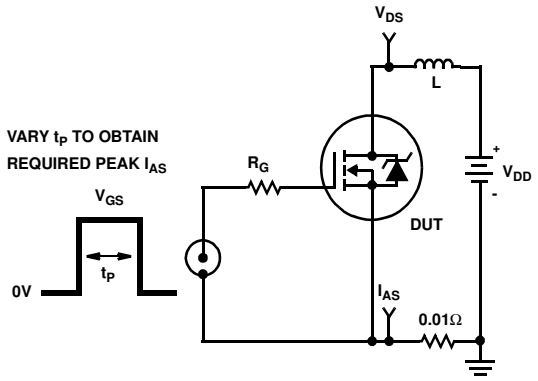


Figure 12. Unclamped Energy Test Circuit

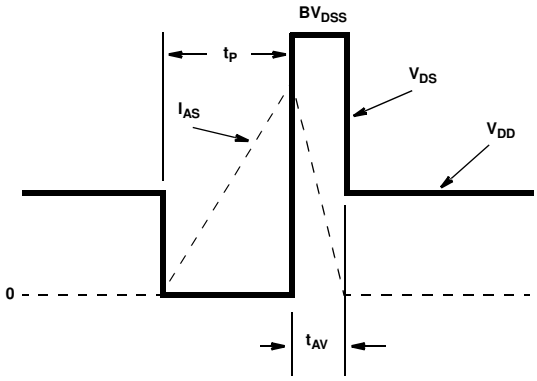


Figure 13. Unclamped Energy Waveforms

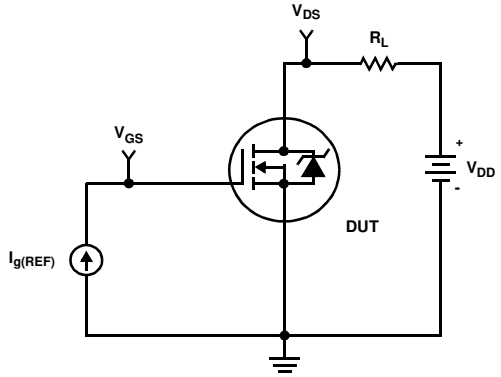


Figure 14. Gate Charge Test Circuit

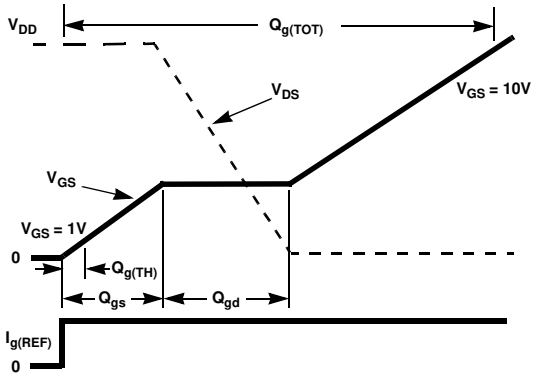


Figure 15. Gate Charge Waveforms

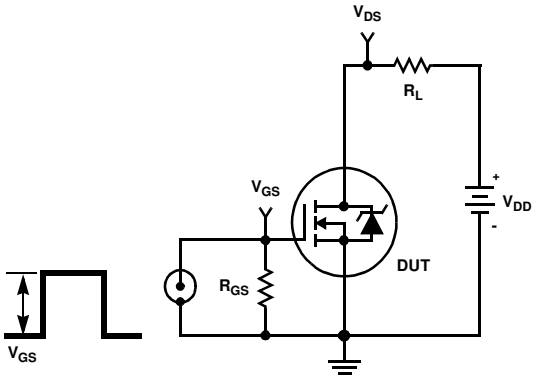


Figure 16. Switching Time Test Circuit

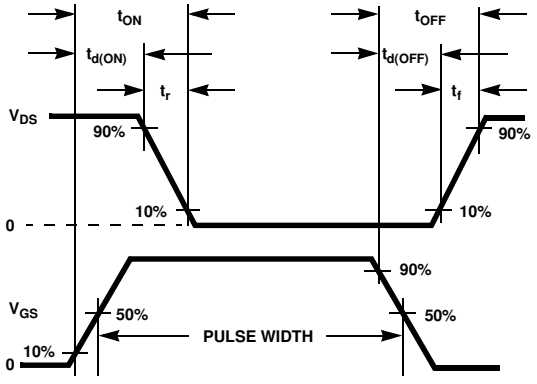


Figure 17. Switching Time Waveform

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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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