

Product Summary (Typ. @ $V_{GS} = -4.5V$, $T_A = +25^{\circ}C$)

BV _{DSS}	R _{DS(ON)}	Q _g	Q _{gd}	I _D
-12V	0.065Ω	2.5nC	0.6nC	-3.3A

Description

This new generation MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$) yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

- Battery managements
- Load switches
- Battery protections

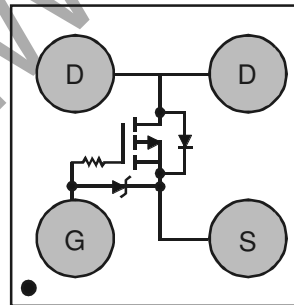
Features

- LD-MOS Technology with the Lowest Figure of Merit: $R_{DS(ON)} = 0.065\Omega$ to Minimize On-State Losses
 $Q_g = 2.5nC$ for Ultra-Fast Switching
- $V_{GS(TH)} = -0.5V$ Typ. for a Low Turn-On Potential
- CSP with Footprint 1.0mm × 1.0mm
- Height = 0.62mm for Low Profile
- ESD = 3kV HBM Protection of Gate
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e.: parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please refer to the related automotive grade (Q-suffix) part. A listing can be found at <https://www.diodes.com/products/automotive/automotive-products/>.**
- **This part is qualified to JEDEC standards (as references in AEC-Q) for High Reliability. <https://www.diodes.com/quality/product-definitions/>**

Mechanical Data

- Package: U-WLB1010-4
- Terminal Connections: See Diagram Below
- Weight: 0.0018 grams (Approximate)

U-WLB1010-4



Top View
Equivalent Circuit



ESD PROTECTED TO 3kV

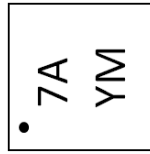
Ordering Information (Note 4)

Part Number	Package	Packing	
		Qty.	Carrier
DMP1081UCB4-7	U-WLB1010-4	3,000	Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
 2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

Marking Information

U-WLB1010-4



7A = Product Type Marking Code
 YM = Date Code Marking
 Y = Year (ex: J = 2022)
 M = Month (ex: 9 = September)

Date Code Key

Year	2016	...	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031
Code	D	...	J	K	L	M	N	O	P	R	S	T

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Value	Unit	
Drain-Source Voltage	V_{DSS}	-12	V	
Gate-Source Voltage	V_{GSS}	-6	V	
Continuous Drain Current (Note 5) $V_{GS} = -4.5\text{V}$	Steady State	$T_A = +25^\circ\text{C}$	-3.3	A
		$T_A = +70^\circ\text{C}$	-2.7	A
Continuous Drain Current (Note 5) $V_{GS} = -2.5\text{V}$	Steady State	$T_A = +25^\circ\text{C}$	-3.0	A
		$T_A = +70^\circ\text{C}$	-2.4	A
Pulsed Drain Current (Note 6)	I_{DM}	20	A	

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Power Dissipation (Note 7)	P_D	0.82	W
Thermal Resistance, Junction to Ambient @ $T_A = +25^\circ\text{C}$ (Note 7)	$R_{\theta JA}$	150	$^\circ\text{C/W}$
Thermal Resistance, Junction to Case @ $T_C = +25^\circ\text{C}$ (Note 7)	$R_{\theta JC}$	42.66	$^\circ\text{C/W}$
Power Dissipation (Note 5)	P_D	1.59	W
Thermal Resistance, Junction to Ambient @ $T_A = +25^\circ\text{C}$ (Note 5)	$R_{\theta JA}$	80.29	$^\circ\text{C/W}$
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

Notes: 5. Device mounted on FR-4 material with 1inch² (6.45cm²), 2oz. (0.071mm thick) Cu.
 6. Repetitive rating, pulse width limited by junction temperature.
 7. Device mounted on FR-4 PCB with minimum recommended pad layout, single sided.

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV _{DSS}	-12	-	-	V	V _{GS} = 0V, I _D = -250μA
Gate-Source Breakdown Voltage	BV _{GSS}	-6.0	-	-	V	V _{DS} = 0V, I _G = -250μA
Zero Gate Voltage Drain Current T _J = +25°C	I _{DSS}	-	-	-1	μA	V _{DS} = -9.6V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	-	-	-100	nA	V _{GS} = -6V, V _{DS} = 0V
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	V _{GS(TH)}	-0.35	-0.5	-0.65	V	V _{DS} = V _{GS} , I _D = -250μA
Static Drain-Source On-Resistance	R _{DS(ON)}	-	0.065	0.08	Ω	V _{GS} = -4.5V, I _D = -500mA
		-	0.077	0.1		V _{GS} = -2.5V, I _D = -500mA
		-	0.108	0.13		V _{GS} = -1.5V, I _D = -500mA
		-	0.4	10		V _{GS} = -0.9V, I _D = -100mA
Forward Transfer Admittance	Y _{fs}	-	4	-	S	V _{DS} = -6V, I _D = -500mA
Diode Forward Voltage	V _{SD}	-	-0.6	-1.0	V	V _{GS} = 0V, I _S = -500mA
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C _{iSS}	-	213	350	pF	V _{DS} = -6V, V _{GS} = 0V, f = 1.0MHz
Output Capacitance	C _{oSS}	-	119	250		
Reverse Transfer Capacitance	C _{rSS}	-	54.4	90		
Total Gate Charge	Q _g	-	2.5	5	nC	V _{GS} = -4.5V, V _{DS} = -6V, I _D = -500mA
Gate-Source Charge	Q _{gs}	-	0.3	-		
Gate-Drain Charge	Q _{gd}	-	0.6	-		
Gate Charge at V _{TH}	Q _{g(TH)}	-	0.15	-		
Turn-On Delay Time	t _{D(ON)}	-	16.7	-	ns	V _{DS} = -6V, V _{GS} = -2.5V, R _G = 20Ω, I _D = -500mA
Turn-On Rise Time	t _r	-	20.6	-		
Turn-Off Delay Time	t _{D(OFF)}	-	38.4	-		
Turn-Off Fall Time	t _f	-	28.4	-		
Reverse Recovery Charge	Q _{RR}	-	2.0	-	nC	V _{DD} = -4.0V, I _F = -0.5A, di/dt = 100A/μs
Reverse Recovery Time	t _{RR}	-	9.5	-	ns	

Notes: 8. Short duration pulse test used to minimize self-heating effect.
9. Guaranteed by design. Not subject to production testing.

NOT RECOMMENDED FOR NEW DESIGN

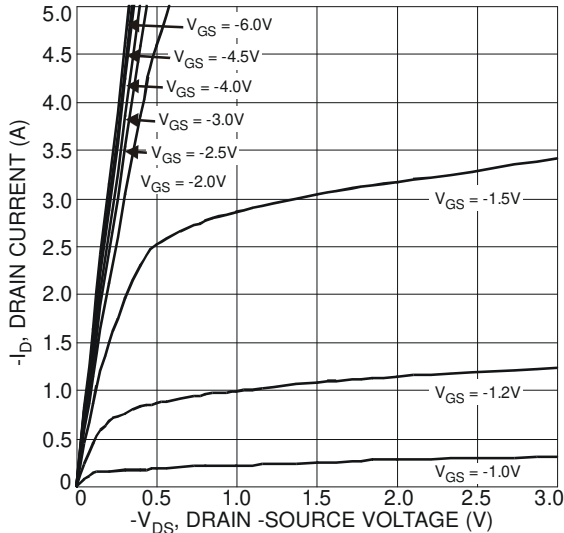


Fig. 1 Typical Output Characteristics

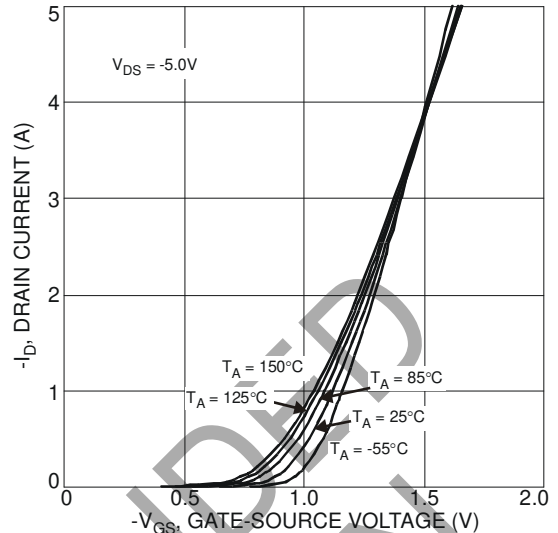


Fig. 2 Typical Transfer Characteristics

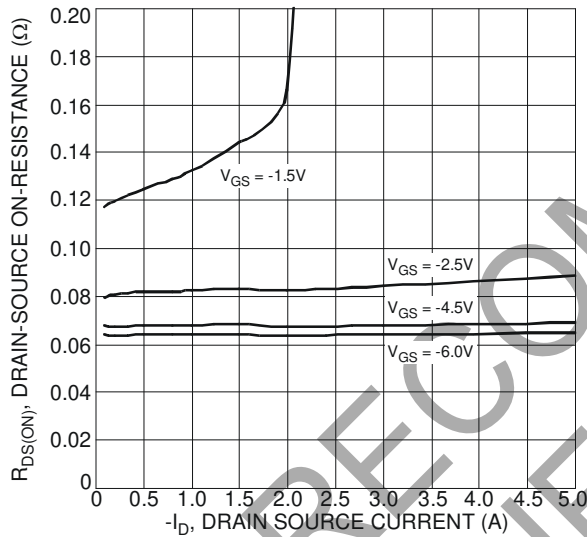


Fig. 3 Typical On-Resistance vs. Drain Current and Gate Voltage

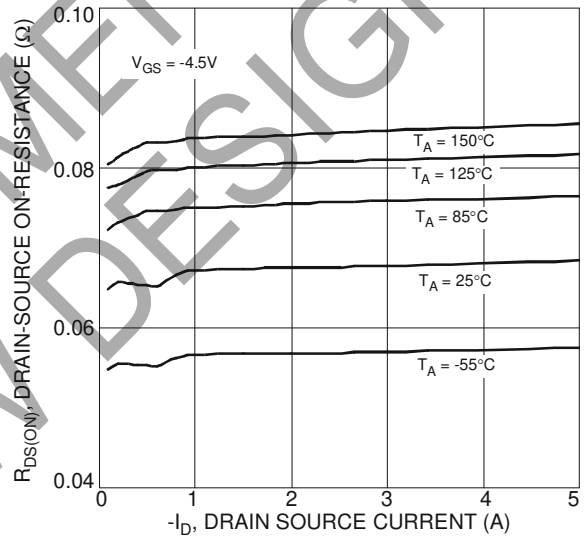


Fig. 4 Typical On-Resistance vs. Drain Current and Temperature

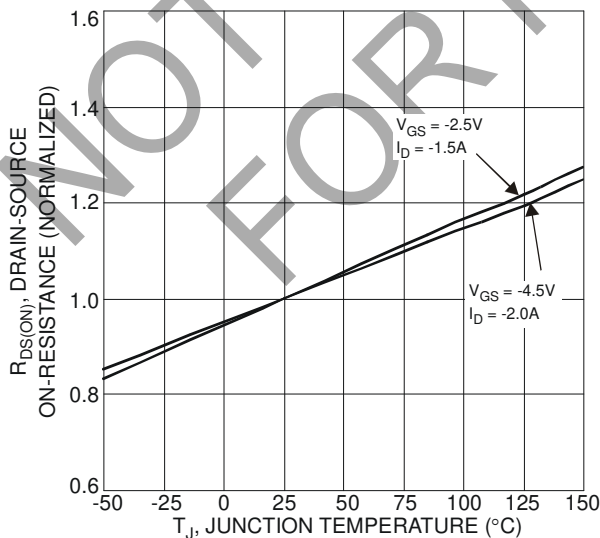


Fig. 5 On-Resistance Variation with Temperature

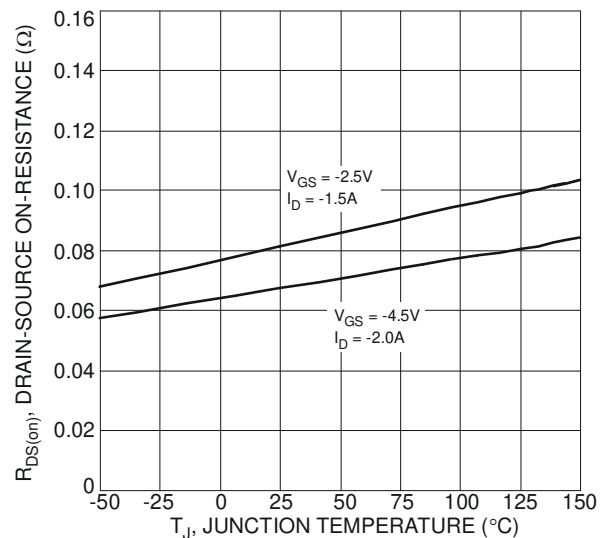


Fig. 6 On-Resistance Variation with Temperature

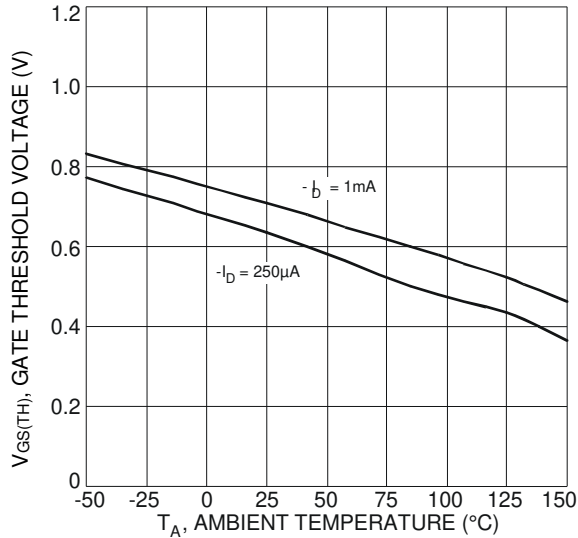


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

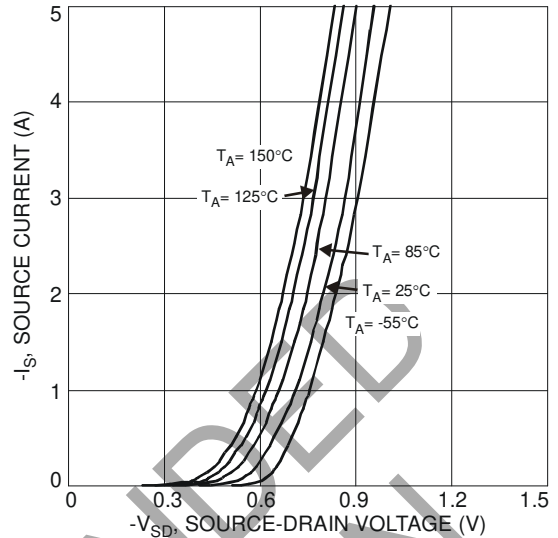


Fig. 8 Diode Forward Voltage vs. Current

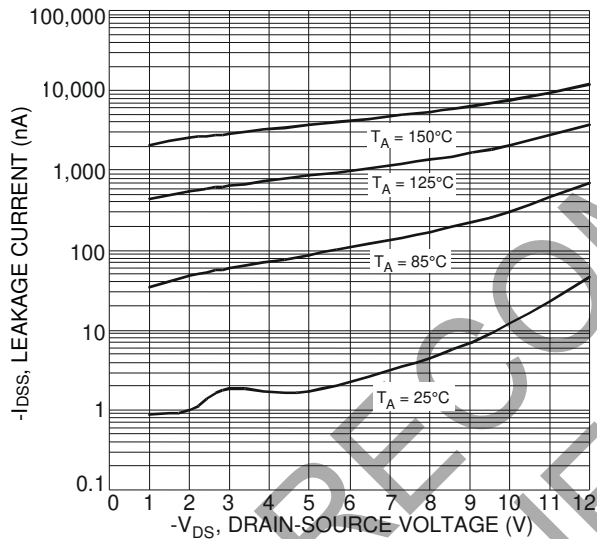


Fig. 9 Typical Drain-Source Leakage Current vs. Voltage

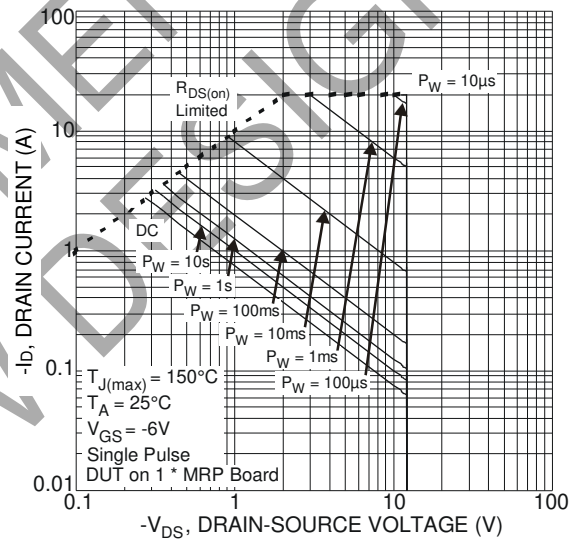


Fig. 10 SOA, Safe Operation Area

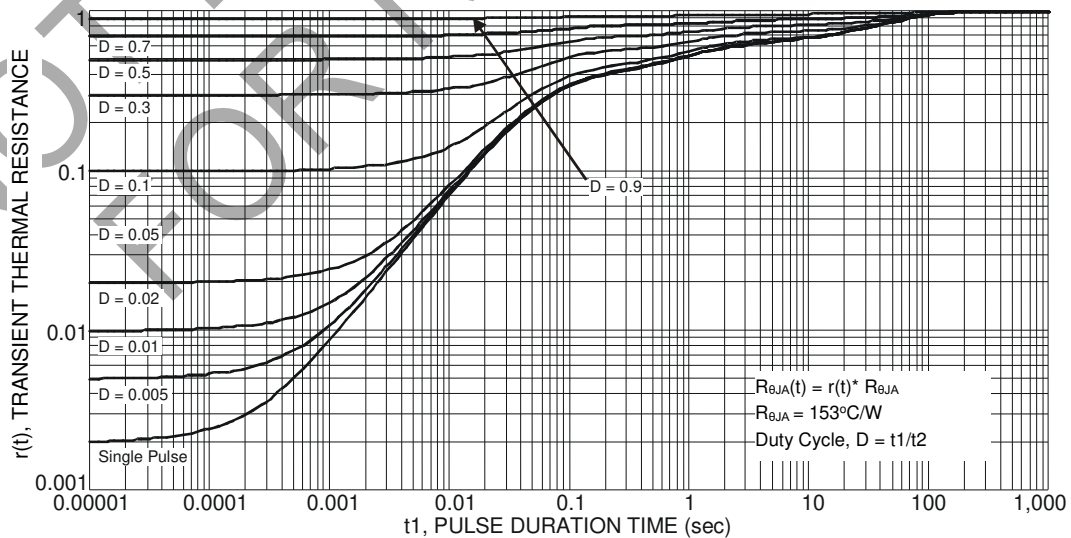
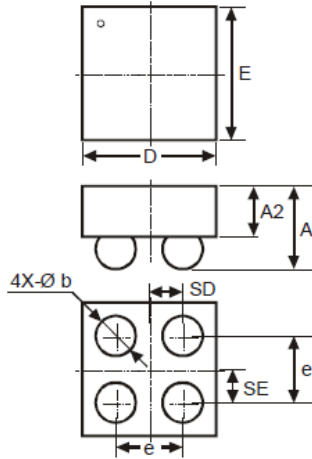


Fig. 11 Transient Thermal Resistance

Package Outline Dimension

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

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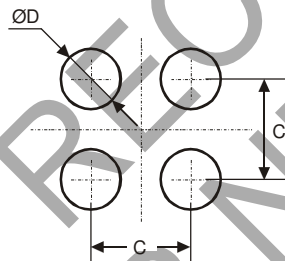
U-WLB1010-4			
Dim	Min	Max	Typ
D	0.95	1.05	1.00
E	0.95	1.05	1.00
A	-	0.62	-
A2	-	-	0.38
b	0.25	0.35	0.30
e	-	-	0.50
SD	-	-	0.25
SE	-	-	0.25

All Dimensions in mm

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

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Dimensions	Value (in mm)
C	0.50
D	0.25

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