19-4113; Rev 1; 10/10

MAXIM

Single/Multiphase, Step-Down, DC-DC Converter Delivers Up to 25A Per Phase

General Description

The MAX8686 current-mode, synchronous PWM step-down regulator with integrated MOSFETs operates from a 4.5V to 20V input supply and generates an adjustable output voltage from 0.7V to 5.5V while delivering up to 25A per phase.

The MAX8686 employs a peak current-mode architecture that operates with an adjustable switching frequency from 300kHz to 1MHz. An adjustable current-limit threshold allows for optimization for different applications with different load currents. Inductor current sense is achieved either using an external sense resistor or using a lossless inductor current-sense scheme. The foldback and hiccup current limit reduces the power dissipation during overload or short-circuit conditions and allows for autorecovery when the fault condition is removed.

The MAX8686 offers the ability to start up monotonically even when there is a prebias output voltage. In addition, an adjustable soft-start capability allows for a controlled turn-on. The MAX8686 features an accurate 1% reference and offers a reference input that allows for a higher accuracy reference to be used for voltage tracking applications such as DDR memory.

The MAX8686 can be paralleled (up to eight) together in a true multiphase mode to deliver up to 200A of output current. When operating in this mode, this device achieves better than 10% current balance between phases at full load. The MAX8686 supports programmable phase shedding to improve system efficiency during light load conditions.

Other features include an enable input and a power-OK (POK) indicator used for power sequencing. The MAX8686 also features latch overvoltage protection that turns on the low-side MOSFET when the output voltage exceeds 120% of the nominal voltage. The MAX8686 is offered in a thermally enhanced 40-pin, 6mm x 6mm TQFN package.

Applications

POL Power Supplies

Module Replacements

Telecom Equipment

Networking Equipment

Servers

DDR Memory

Pin Configuration appears at end of data sheet.

Features

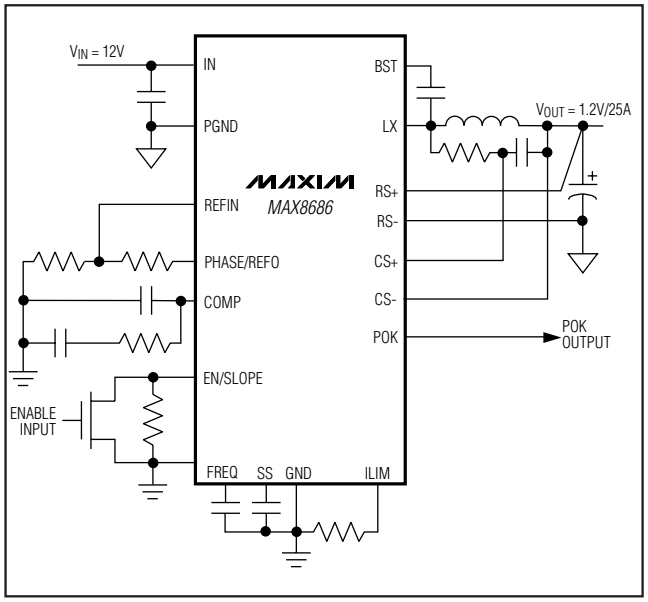
- **Operating Range from 4.5V to 20V Input Supply**
- **1% Reference Voltage Accuracy Over Temperature**
- **Reference Input (REFIN) for Output Tracking or System Reference Voltage**
- **Adjustable Switching Frequency from 300kHz to 1MHz**
- **Single/Multiphase Operation Delivers Up to 25A/200A with Integrated MOSFETs**
- **Adjustable Current Limit**
- **Monotonic Output Voltage at Startup (Prebias)**
- **Output Sink and Source Current Capability**
- **Adjustable Soft-Start**
- **Thermal-Overload Protection**
- **Output Overvoltage Protection**
- **Thermally Enhanced 6mm x 6mm TQFN Package (4W)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX8686ETL+	-40°C to +85°C	40 TQFN-EP*

+Denotes a lead-free package.
**EP = Exposed pad.*

Typical Application Circuit



Single/Multiphase, Step-Down, DC-DC Converter Delivers Up to 25A Per Phase

ABSOLUTE MAXIMUM RATINGS

IN, INA to PGND .....-0.3V to +22V
BST, DH to LX .....-0.3V to +6V
BST to PGND .....-0.3V to +28V
LX to PGND .....-0.3V to (V_{IN} + 0.3V) (-2V for 50ns)
BST to VL .....-0.3V to +22V
AVL to GND .....-0.3V to (V_{VL} + 0.3V)
COMP, ILIM, FREQ, PHASE/REFO, RS+, RS-, POK, REFIN, CS+, CS- to GND .....-0.3V to (V_{AVL} + 0.3V)
VL to PGND .....-0.3V to +6V
EN/SLOPE to GND .....-0.3V to +6V
RTN to PGND to GND to GFREQ .....-0.3V to +0.3V
IN Continuous Current .....$20A_{RMS}$
LX Continuous Current .....$25A_{RMS}$
Continuous Power Dissipation (T_A = +70°C) (Note 1)
40-Pin TQFN (derate 50mW/°C above +70°C) 4000mW
θ_{JC} (thermal resistance from junction to exposed pad) (Note 1) .....3.5°C/W
θ_{JT} (thermal resistance from junction to top) (Note 1) ...3.9°C/W
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations see **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{INA} = 12V, VL = AVL, V_{REFIN} = 1V, V_{RS+} - V_{RS-} = 1V, V_{RS-} = 0V, $V_{EN/SLOPE}$ = 1.25V, V_{CS+} = V_{CS-} = 1V, R_{ILIM} = 122kΩ, C_{VL} = 1µF, C_{AVL} = 0.22µF, C_{FREQ} = 270pF, T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL						
Operating Input-Voltage Range	V_{INA} = V_{IN} , T_A = -40°C to +85°C		6		20	V
Operating Input-Voltage Range	V_{IN} = V_{INA} = V_{VL} = V_{AVL}, T_A = -40°C to +85°C		4.5		5.5	V
IN/INA Shutdown Supply Current	$V_{EN/SLOPE}$ = 0V, V_{IN} = V_{INA} = 20V	T_A = +25°C		450		µA
		T_A = +85°C		500		
IN/INA Quiescent Supply Current	V_{RS+} = 1.1V, no switching; V_{IN} = V_{INA} = 20V, T_A = -40°C to +85°C			5.5	6.6	mA
AVL Undervoltage Lockout Trip Level	Rising, T_A = -40°C to +85°C		4.2	4.35	4.45	V
	Falling			4.03		
VL Output Voltage	6V ≤ V_{IN} = V_{INA} ≤ 20V, 1mA ≤ I_{VL} ≤ 30mA, T_A = -40°C to +85°C		5.2	5.4	5.5	V
SOFT-START (SS)						
SS Shutdown Resistance	$V_{EN/SLOPE}$ = 0V (master mode)			20	100	Ω
SS Soft-Start Current	V_{SS} = 0.4V and 1.1V, T_A = -40°C to +85°C		19	25	31	µA
PHASE COMPARATOR AND REFERENCE (PHASE/REFO)						
Reference Output Voltage	Measured at PHASE/REFO (master mode), T_A = -40°C to +85°C		3.267	3.300	3.333	V
PHASE Comparator Offset	V_{RS-} = V_{AVL} (slave mode), V_{PHASE} = 0.3V and 2.5V, T_A = -40°C to +85°C		-20		+20	mV
REFIN INPUT						
REFIN Input Bias Current	V_{REFIN} = 0.7V or 3.3V		-500		+500	nA
REFIN Input Voltage Range			0		3.3	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{INA} = 12V, VL = AVL, V_{REFIN} = 1V, V_{RS+} - V_{RS-} = 1V, V_{RS-} = 0V, $V_{EN/SLOPE}$ = 1.25V, V_{CS+} = V_{CS-} = 1V, R_{ILIM} = 122kΩ, C_{VL} = 1µF, C_{AVL} = 0.22µF, C_{FREQ} = 270pF, T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ERROR AMPLIFIER						
Remote-Sense Accuracy (Including Error Amplifier Offset)	Measure as V_{RS+} - V_{RS-} (T_A = -40°C to +85°C)	V_{REFIN} = 3.3V	3.267	3.3	3.333	V
		V_{REFIN} = 0.7V	0.693	0.7	0.707	
Transconductance	T_A = -40°C to +85°C		1.1	1.7	2.6	mS
COMP Source Current	V_{RS+} - V_{RS-} = 1.3V		220	300		µA
COMP Sink Current	V_{RS+} - V_{RS-} = 0.7V		220	300		µA
COMP Shutdown Resistance	$V_{EN/SLOPE}$ = 0V			20	100	Ω
RS+/RS- Input Leakage Current				0.2	1.5	µA
RS+ Input Common-Mode Range	V_{IN} = V_{INA} = V_{VL} = V_{AVL} = 4.5V, V_{RS-} = 100mV		0		3.4	V
RS- Input Common-Mode Range			-100		+100	mV
CURRENT-SENSE AMPLIFIER						
Input Offset Voltage	Measure at CS+ and CS-, V_{CS+} = V_{CS-} = 0.7V and 5.5V (T_A = -40°C to +85°C)		-1.5		+1.5	mV
Current-Sense Amplifier Gain	V_{CS-} = 0 to 5V, V_{CS+} - V_{CS-} = 30mV, T_A = -40°C to +85°C		29.0	30.5	32.0	V/V
Input Bias Current	V_{CS+} = V_{CS-} = 5.5V and 0V		-4		+4	µA
CURRENT LIMIT						
ILIM Output Current	V_{ILIM} = 2V, T_A = -40°C to +85°C		9	10	11	µA
Current-Limit Threshold	Measure as V_{CS+} - V_{CS-} (T_A = -40°C to +85°C)	R_{ILIM} = 122kΩ	16	20	23	mV
		R_{ILIM} = 275kΩ	38	45	52	
COMP Clamp Voltage High	R_{ILIM} = 275kΩ, V_{REFIN} = 3.3V, V_{RS+} - V_{RS-} = 2V		3.6	3.8	4.0	V
COMP Clamp Voltage Low	V_{REFIN} = 3.3V, V_{RS+} - V_{RS-} = 3.35V		0.54	0.6	0.66	V
Maximum Peak Positive Current Threshold	R_{ILIM} = 275kΩ, no slope compensation			54		mV

Single/Multiphase, Step-Down, DC-DC Converter Delivers Up to 25A Per Phase

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{INA} = 12V, VL = AVL, V_{REFIN} = 1V, V_{RS+} - V_{RS-} = 1V, V_{RS-} = 0V, $V_{EN/SLOPE}$ = 1.25V, V_{CS+} = V_{CS-} = 1V, R_{ILIM} = 122kΩ, C_{VL} = 1µF, C_{AVL} = 0.22µF, C_{FREQ} = 270pF, T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OSCILLATOR (FREQ)					
Source Current	V_{FREQ} = 2V, T_A = -40°C to +85°C	480	500	520	µA
Switching Frequency	C_{FREQ} = 180pF	0.8	1	1.2	MHz
	C_{FREQ} = 580pF	240	300	360	kHz
Minimum On-Time			100		ns
FREQ Discharge Resistance			10	50	Ω
Ramp Peak Voltage		2.60	V_{AVL}/2	2.85	V
SLOPE COMPENSATION (EN/SLOPE)					
V_{SLOPE} Range		1.25		2.50	V
SLOPE Source Current		8	10	12	µA
THERMAL PROTECTION					
Thermal Shutdown	Rising temperature		160		°C
Thermal-Shutdown Hysteresis			30		°C
POWER-OK (POK)					
POK Threshold	V_{OUT} rising	87	90	93	%V_{OUT}
	V_{OUT} falling		87		
POK Output Voltage Low	V_{RS+} - V_{RS-} = 0.8V, I_{POK} = 2mA		25	200	mV
POK Leakage Current	V_{POK} = 5.5V		0.001	1	µA
OVERVOLTAGE OUTPUT PROTECTION (OVP)					
Overvoltage Fault Trip Level	V_{REFIN} = 3.3V, V_{RS+} rising, percentage of V_{OUT} in regulation	115	120	125	%
ENABLE (EN/SLOPE)					
EN Logic-High		1.2			V
EN Logic-Low				0.7	V
BST					
Internal PMOS On-Resistance			8		Ω

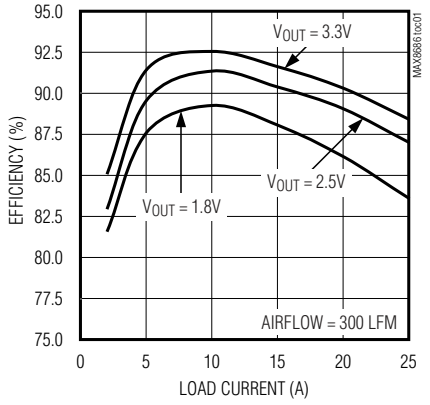
Note 2: Specifications to T_A = -40°C are guaranteed by design and not production tested.

Single/Multiphase, Step-Down, DC-DC Converter Delivers Up to 25A Per Phase

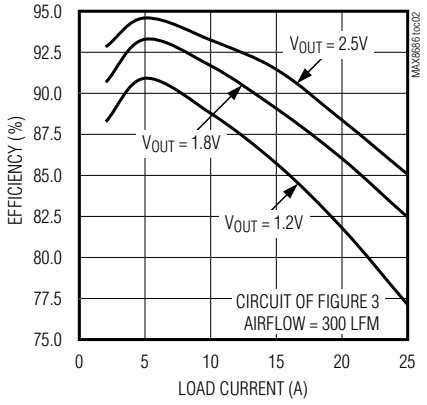
Typical Operating Characteristics

(V_{IN} = 12V, f_{SW} = 500kHz, single phase, circuit of Figure 2, unless otherwise noted.)

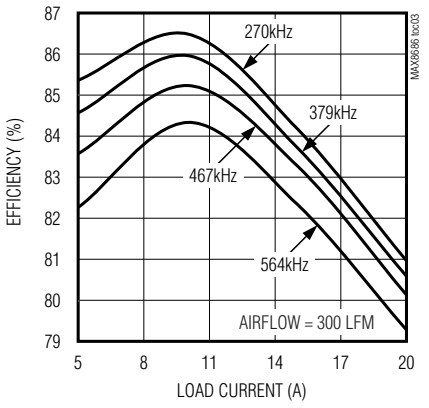
SINGLE-PHASE EFFICIENCY vs. LOAD CURRENT



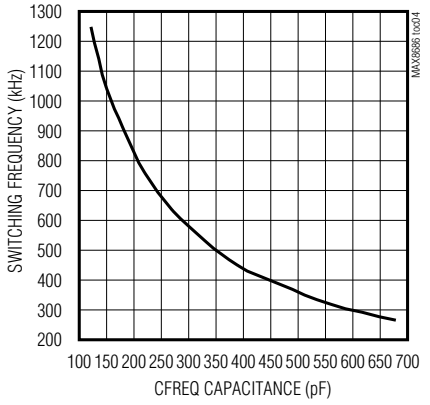
SINGLE-PHASE EFFICIENCY vs. LOAD CURRENT (V_{IN} = 5V)



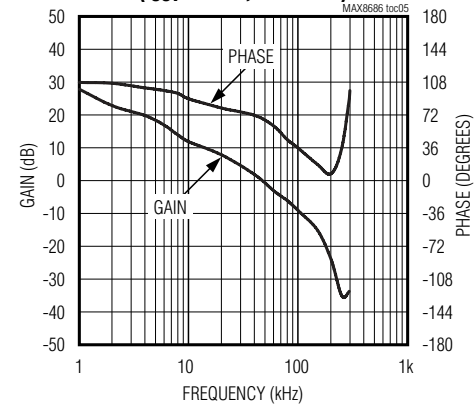
EFFICIENCY vs. LOAD CURRENT



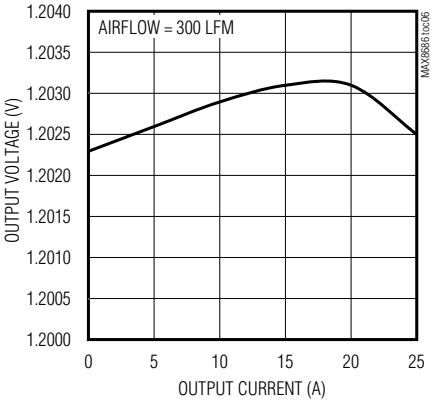
SWITCHING FREQUENCY vs. CFREQ CAPACITANCE



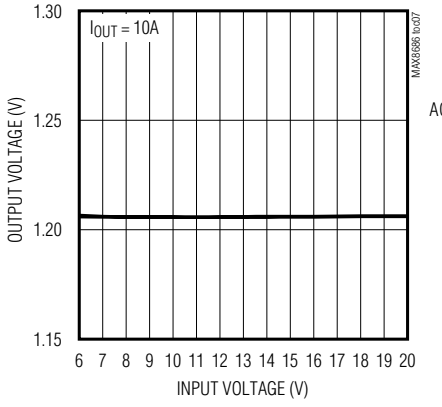
CLOSED-LOOP FREQUENCY RESPONSE (I_{OUT} = 160A, 8 PHASES)



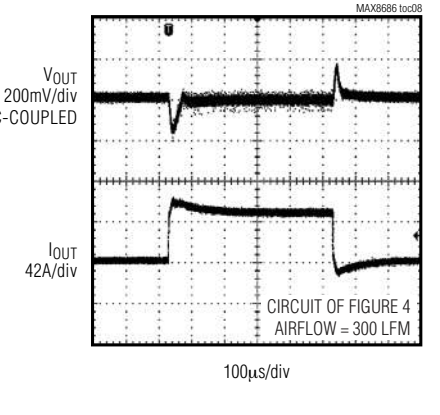
OUTPUT VOLTAGE vs. OUTPUT CURRENT



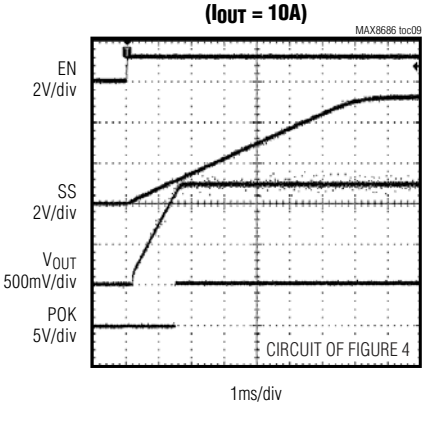
OUTPUT VOLTAGE vs. INPUT VOLTAGE



OUTPUT LOAD TRANSIENT



SOFT-START WITH EN CONTROL (I_{OUT} = 10A)

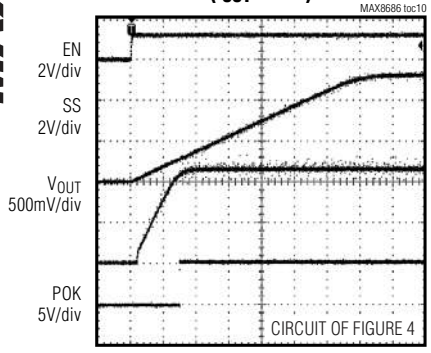


Single/Multiphase, Step-Down, DC-DC Converter Delivers Up to 25A Per Phase

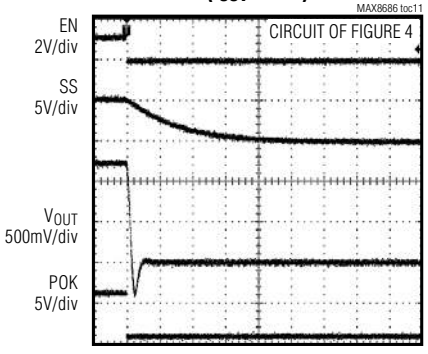
Typical Operating Characteristics (continued)

(V_{IN} = 12V, f_{SW} = 500kHz, single phase, circuit of Figure 2, unless otherwise noted.)

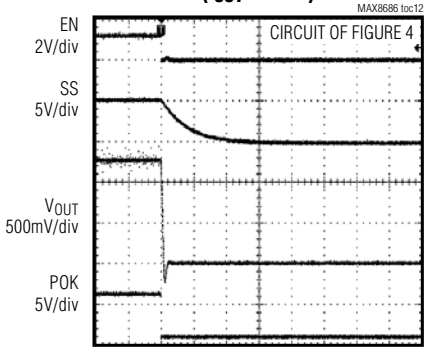
SOFT-START WITH EN CONTROL (I_{OUT} = 10A)



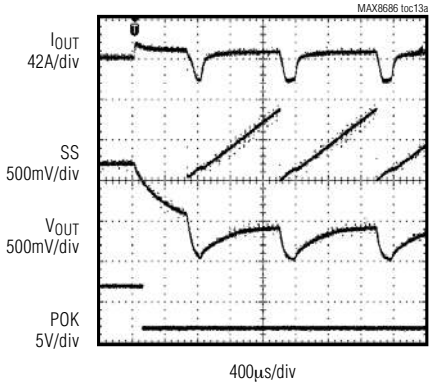
SHUTDOWN WITH EN CONTROL (I_{OUT} = 10A)



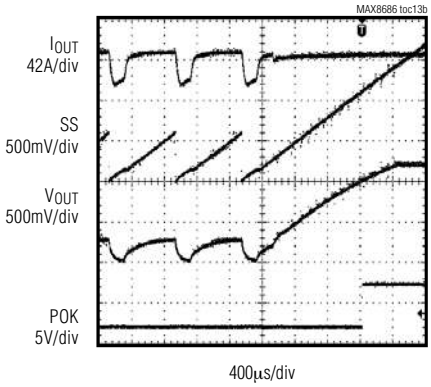
SHUTDOWN WITH EN CONTROL (I_{OUT} = 100A)



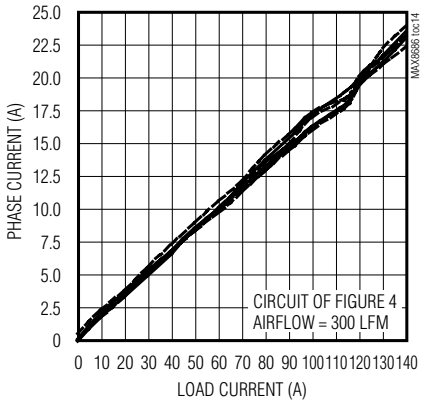
SHORT-CIRCUIT PROTECTION



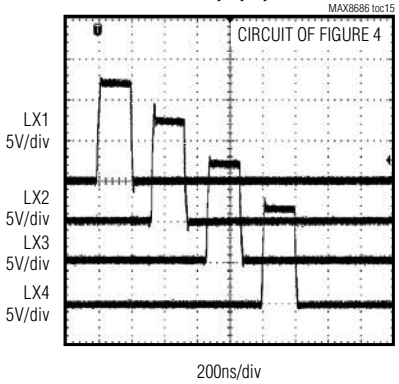
SHORT-CIRCUIT RECOVERY



CURRENT-SHARING ACCURACY



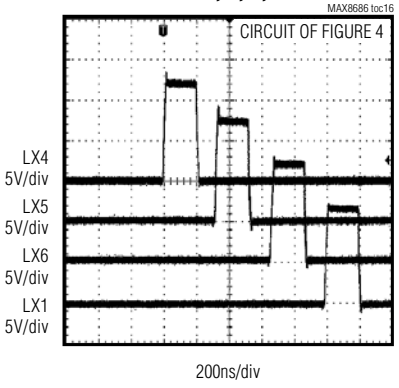
LX_ SWITCHING WAVEFORM FOR PHASES 1, 2, 3, AND 4



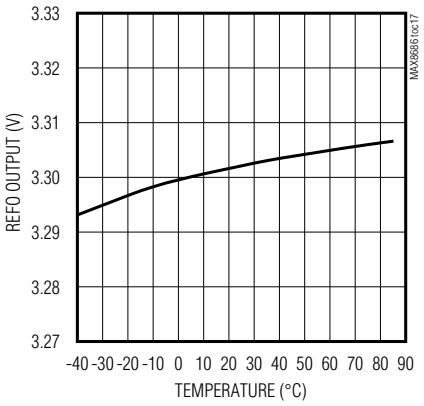
Typical Operating Characteristics (continued)

(V_{IN} = 12V, f_{SW} = 500kHz, single phase, circuit of Figure 2, unless otherwise noted.)

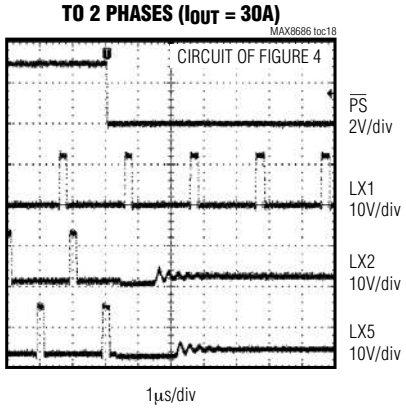
LX_ SWITCHING WAVEFORM FOR PHASES 4, 5, 6, AND 1



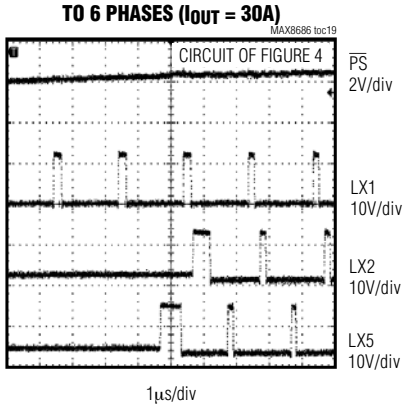
REFO OUTPUT vs. TEMPERATURE



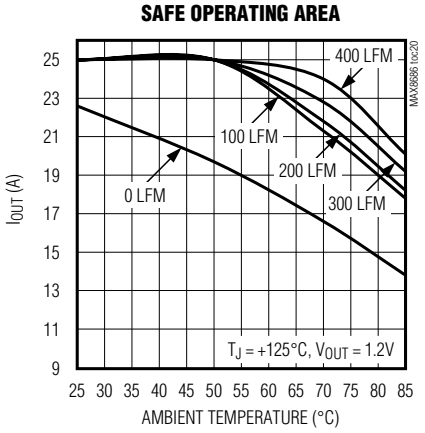
PHASE SHEDDING FROM 6 PHASES TO 2 PHASES (I_{OUT} = 30A)



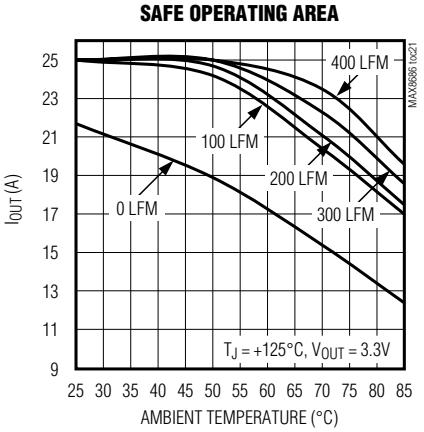
PHASE RECOVERY FROM 2 PHASES TO 6 PHASES (I_{OUT} = 30A)



SAFE OPERATING AREA



SAFE OPERATING AREA



Single/Multiphase, Step-Down, DC-DC Converter Delivers Up to 25A Per Phase

Pin Description

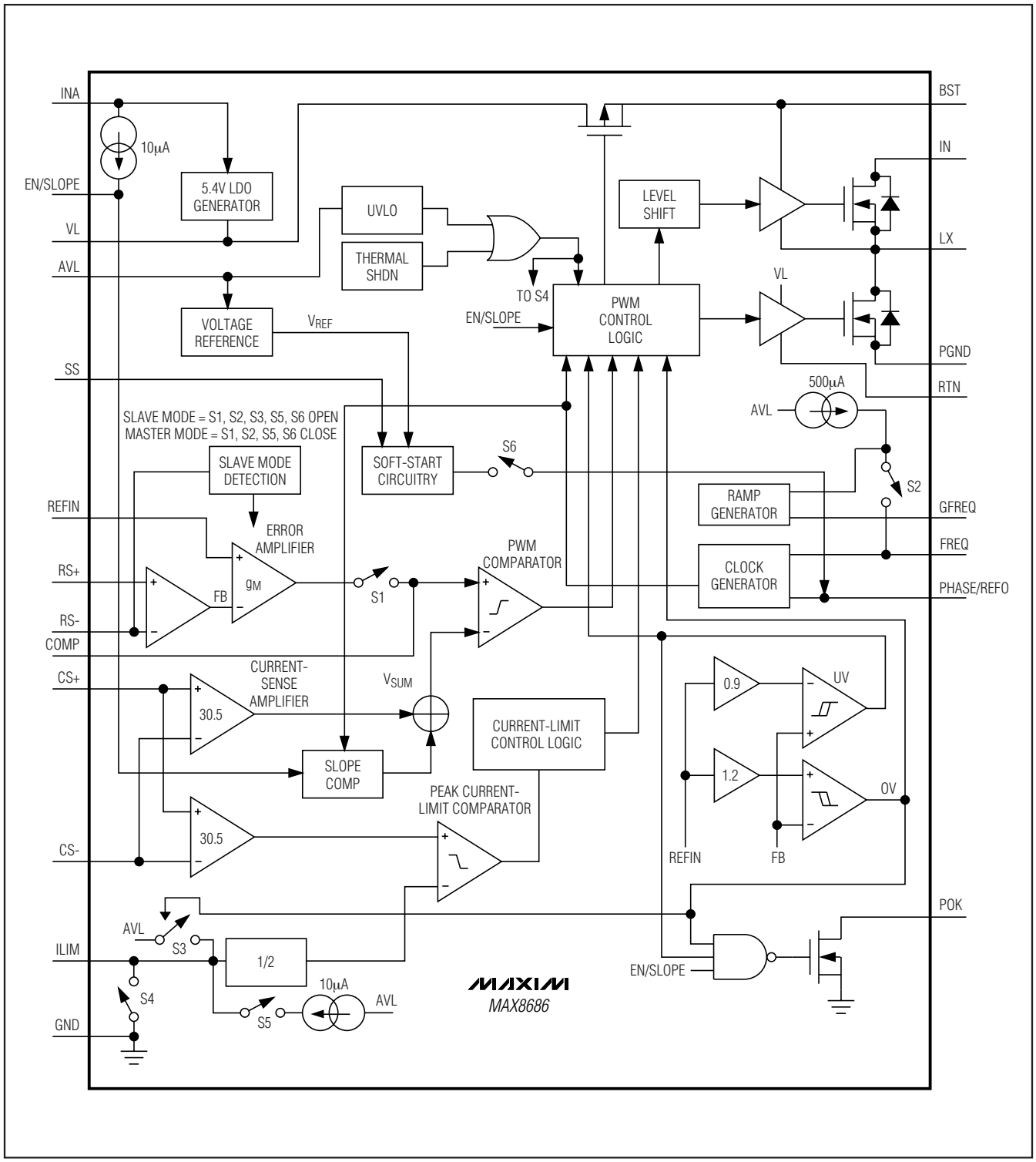
PIN	NAME	FUNCTION
1	CS-	Negative Differential Current-Sense Input. Connect CS- to the output side of the inductor for lossless current sense or to the load side of the current-sense resistor.
2	CS+	Positive Differential Current-Sense Input. Connect CS+ to the inductor through an RC network for lossless current sense or to the inductor side of the current-sense resistor.
3	GFREQ	C_{FREQ} Capacitor Return Terminal. Connect the frequency-setting capacitor C_{FREQ} to GFREQ as close as possible to the device.
4	EN/SLOPE	Enable and Slope Compensation Input. Connect a resistor from EN/SLOPE to GND to set the desired slope compensation ramp voltage. An internal 10µA current source pulls up EN/SLOPE. The device shuts down when the voltage at EN/SLOPE is less than 0.7V. Connect EN/SLOPE to an open-drain or open-collector output for system enable or phase-shedding function.
5, 16	LX	Inductor Connection. LX is high impedance during shutdown.
6	RTN	Power Ground for Low-Side Gate Driver. Connect RTN to PGND plane at the return terminal of the IN bypass capacitor.
7–15	PGND	Power Ground. Low-side MOSFET source connection.
17	N.C.	No Connection. Not internally connected.
18–26	IN	Power Input. Connect IN to the input voltage source. Connect input bypass capacitor from IN to PGND as close as possible to the device. Connect IN, INA, and VL together for 5V operation (see Figure 3).
27	INA	Input of the Internal VL Linear Regulator. Bypass INA with a 0.1µF capacitor to PGND.
28	GND	Analog Ground
29	AVL	Input Voltage to the Device's Internal Analog Circuitry. Connect AVL to VL through a lowpass RC filter.
30	VL	Internal 5.4V Linear Regulator Output. Connect a ceramic capacitor of at least 1µF from VL to RTN. INA is the input to this linear regulator. Connect VL to INA when V_{INA} is less than 5.5V. VL provides power for the MOSFET drivers.
31	BST	Boost Capacitor Connection. Connect a 0.22µF ceramic capacitor from BST to LX.
32	POK	Power-Good Output. POK is an open-drain output that is high impedance when the output voltage is at its nominal regulated voltage. The POK rising threshold is 90% of the reference voltage at REFIN. POK is internally pulled low during shutdown. Connect POK to GND for slave mode operation.

Pin Description (continued)

PIN	NAME	FUNCTION
33	FREQ	Frequency-Setting Input. Connect a capacitor from FREQ to GFREQ to set the switching frequency. The triangle ramp runs between 0 and AVL/2. In multiphase applications, connect FREQ of the master and all slave devices together. FREQ is internally pulled to GFREQ during shutdown.
34	SS	Soft-Start Input. For master-mode or single-phase operation, connect a capacitor from SS to GND to set the soft-start time. A 25µA internal current source charges the capacitor. SS is pulled to GND in shutdown. Connect SS to GND for slave mode operation.
35	ILIM	Analog Programmable Current Limit. Connect a resistor from ILIM to GND to set the current limit. A 10µA current source through this resistor sets the current-limit threshold. In multiphase applications, connect ILIM of the master and all slave devices together.
36	REFIN	Voltage Error-Amplifier Reference Input. For master-mode or single-phase operation, connect REFIN to PHASE/REFO through a resistor-divider to set the output voltage from 0 to 3.3V. To use an external reference, connect REFIN to the system reference voltage, and use an RC network at REFIN to implement soft-start if the external reference does not provide this function. Connect REFIN to GND for slave mode operation.
37	PHASE/REFO	Phase Selection Input/Reference Voltage Output. For single-phase or master-mode operation, the 3.3V output with 1% accuracy can be used as a reference voltage. For multiphase operation, connect PHASE/REFO of each slave device to the center tap of a resistor-divider from the master AVL to GND. The resistor values are selected to set phase delay between phases. The PWM cycle starts 60ns after the rising edge of V_{FREQ} crosses V_{PHASE}.
38	COMP	Compensation and Output of the Voltage-Error Amplifier. Connect a Type II compensation network at COMP. COMP is internally pulled to GND in shutdown. In multiphase applications, connect COMP of the master and all slave devices together.
39	RS+	Positive Input of the Output-Voltage Remote Sense. For master-mode or single-phase operation, connect RS+ to the output-voltage sense point at the load. Connect RS+ to AVL (slave) for slave mode operation.
40	RS-	Negative Input of the Output-Voltage Remote Sense. For master-mode or single-phase operation, connect RS- to the remote ground at the load. Connect RS- to AVL (slave) for slave mode operation.
—	GND_EP	Ground Exposed Paddle. Connect GND_EP to GND.
—	IN_EP	Input Exposed Paddle. Connect IN_EP to IN.
—	LX_EP	LX Exposed Paddle. Connect LX_EP to LX.

Single/Multiphase, Step-Down, DC-DC Converter Delivers Up to 25A Per Phase

Functional Diagram



Detailed Description

DC-DC Converter Control Architecture

The MAX8686 step-down regulator uses a PWM, current-mode control scheme. An internal transconductance amplifier establishes an integrated error voltage. The heart of the PWM controller is a PWM comparator that compares the integrated voltage-feedback signal against the amplified current-sense signal plus an adjustable slope-compensation ramp, which is summed with the current signal to ensure stability. At each rising edge of the internal clock, the internal high-side MOSFET turns on until the PWM comparator trips or the maximum duty cycle is reached. During this on-time, current ramps up through the inductor, storing energy in the inductor while sourcing current to the output. The current-mode feedback system regulates the peak inductor current as a function of the output-voltage error signal. The circuit acts as a switch-mode transconductance amplifier and pushes an output LC filter pole normally found in a voltage-mode PWM to a higher frequency. See the *Functional Diagram*.

During the second half of the cycle, the internal high-side MOSFET turns off and the internal low-side MOSFET turns on. The inductor releases the stored energy as the current ramps down, providing current to the load. The output capacitor stores charge when the inductor current exceeds the required load current and discharges when the inductor current is lower, smoothing the voltage across the load. Under soft-overload conditions, when the peak inductor current exceeds the selected current limit (see the *Current-Limit Circuit* section), the high-side MOSFET is turned off immediately and the low-side MOSFET is turned on and remains on to let the inductor current ramp down until the next clock cycle. Under severe-overload or short-circuit conditions, the foldback/hiccup current limit is enabled to reduce power dissipation.

The MAX8686 operates in a forced-PWM mode. The converter maintains a constant switching frequency, regardless of load, to allow for easier filtering of the switching noise.

Internal Linear Regulator (VL)

The MAX8686 contains an internal LDO regulator that provides a 5.4V supply for the MOSFET gate drivers. Connect at least a 1µF ceramic capacitor from VL to RTN. VL also provides power to the internal analog circuit through AVL. Connect an RC lowpass filter (R = 10Ω, C = 0.22µF) from VL to AVL.

Undervoltage Lockout

When AVL drops below 4.03V, the MAX8686 assumes that the supply voltage is too low to make valid decisions, so the undervoltage-lockout (UVLO) circuitry inhibits switching and turns off both power MOSFETs. When AVL rises above 4.35V, the regulator enters the startup sequence and then resumes normal operation.

When operating in a multiphase configuration, the AVL of all the devices must exceed the UVLO threshold before any switching begins. This is achieved through the shared ILIM pin, which is pulled low in UVLO.

Startup, Soft-Start, and Prebias Operation

The internal soft-start circuitry gradually ramps up the reference voltage in order to control the rate of rise of the output voltage and reduce input surge currents during startup. The soft-start time is determined by the value of the capacitor from SS to GND and is approximately equal to 50ms per microfarad of the capacitor.

In addition, the MAX8686 features monotonic output-voltage rise (prebias); therefore, both power MOSFETs are kept off if the voltage between the remote sense input (RS+, RS-) is higher than the voltage at REFIN. This allows the MAX8686 to start up into a prebiased output without pulling the output voltage down.

Before the MAX8686 can begin the soft-start and power-up sequence, the following conditions must be met: AVL exceeds the 4.35V UVLO threshold, EN is at logic-high, and the thermal limit is not exceeded.

Reference Output (PHASE/REFO)/Reference Input (REFIN)

The reference voltage REFO can be used to set the output voltage by scaling this voltage down with a resistive divider and using it as the input voltage to the reference input, REFIN. The 3.3V reference voltage is 1% accurate over temperature and can source up to 20µA.

The reference input REFIN allows the reference value of the device to be set by an external reference. In most applications, the 3.3V voltage with 1% accuracy from the PHASE/REFO pin should be used as the reference. This can be achieved by dividing the 3.3V voltage to the desired output voltage.

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For using an external reference on REFIN, SS needs to be tied to REFIN either directly or indirectly through a resistor for soft-start. For REFIN voltage lower than 1.25V, connect a resistor between SS and REFIN such that the voltage drop across the resistor due to the soft-start current (31µA max) coming out of SS, causing the final SS voltage to be at least 1.25V (see Figure 1a).

The external reference should be able to sink at least 31µA. Calculate R_{REFIN} as follows:

$$R_{REFIN} = \frac{1.25 - V_{EXT}}{19\mu A}$$

where V_{EXT} is the external reference voltage.

In a multiphase converter, only REFIN of the master device is connected to a reference voltage, and the REFIN of all slave devices should be tied to GND.

The REFIN also allows for coincident voltage tracking of multiple converters during power-up/power-down by applying the same voltage on REFIN of the master device in each converter.

Enable, Phase Shedding, and Slope Compensation Input (EN/SLOPE)

An internal 10µA current source pulls the EN/SLOPE input high. The device shuts down when the voltage at the EN/SLOPE falls below 0.7V. By connecting an open-drain or open-collector switch to the EN/SLOPE, this pin can be used to enable/disable a single-phase or multiphase converter system.

A separate system signal can be used to shed some phases of the converter at light load to eliminate all the power loss from these phases and thus improve the system efficiency. The phase shedding signal is connected to the EN/SLOPE pins of the slave devices to be shed.

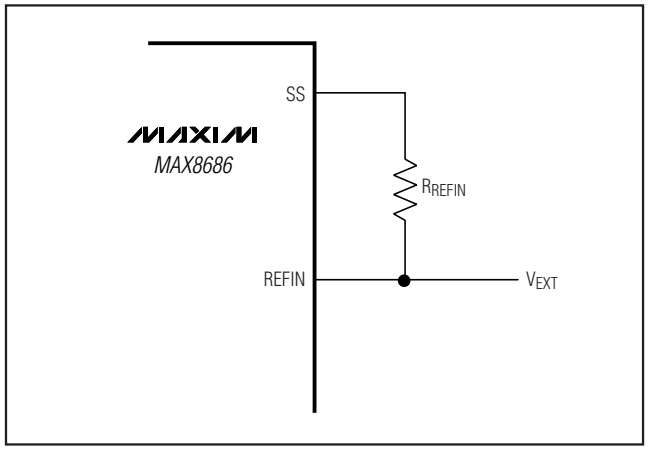

Figure 1a. Using an External Reference

The right timing of the phase shedding signal from the system is critical for the safe operation of the multiphase converter. Only after the load current drops below a certain level, should the phase shedding signal become high. When the open-drain or open-collector switch is logic-low, it shuts down the slave phases connected to the switch to reduce power loss. Before the load current increases to a certain level, the phase shedding signal should become logic-high to release the EN/SLOPE of these slave devices, thus turning these phases back on again to prepare for the higher load current. A minimum load of 2A per phase in the remaining phases is required for the shedded phase(s) to turn on.

The transfer function of the power stage is different with a different number of phases. As the number of phases increases, the power stage gain increases. The compensation network should be designed such that the converter is always stable with the maximum number of phases.

The EN/SLOPE input is also used to set the slope compensation ramp voltage by connecting a resistor from this input to GND. The slope compensation is used to stabilize the converters when the duty cycle is more than 40%.

High-Side Gate-Drive Supply (BST)

A flying capacitor between BST and LX generates the gate-drive voltage for the internal high-side n-channel MOSFET. When the low-side MOSFET is turned on, the capacitor is charged by VL to 5.4V minus the drop across the internal boost switch. When the low-side MOSFET is turned off, the stored voltage of the capacitor is stacked above LX to provide the necessary turn-on voltage (V_{GS}) for the high-side MOSFET. An internal switch between BST and the internal high-side MOSFET's gate closes to turn the MOSFET on.

Current-Sense Amplifier

The current-sense circuit amplifies the differential current-sense voltage (V_{CS+} - V_{CS-}). This amplified current-sense signal and the internal-slope-compensation signal are summed (V_{SUM}) together and fed into the PWM comparator's inverting input. The high-side MOSFET is turned on by the clock in the device and is shut off when V_{SUM} exceeds the error-amplifier output voltage (V_{COMP}) at the noninverting input of the PWM comparator. The differential current sense is also used to provide peak inductor current limiting. The limit can be set by adjusting the analog current-limit input (ILIM).

The current-sense amplifier is used to measure the current across the inductor by connecting to the inductor through an RC network for lossless current sensing or connecting to a current-sense resistor for higher accuracy. The input common-mode voltage range of the current-sense amplifier is from 0 to 5.5V.

Current-Limit Circuit

The current-limit threshold is set by a resistor between ILIM and GND. Under soft-overload conditions, when the peak inductor current exceeds the selected current limit, the high-side MOSFET is turned off immediately and the low-side MOSFET is turned on and remains on to let the inductor current ramp down until the next clock cycle. The converter does not stop switching and the output voltage regulation is not guaranteed. Under severe-overload or short-circuit conditions, the foldback and hiccup current limit is simultaneously activated to reduce power dissipation in the inductor, internal power MOSFETs, and the upstream power source. Thus, the circuit can withstand short-circuit conditions continuously without causing overheating of any component. If the device experiences a persistent overload condition, the device will autoretry with a soft-start. The converter will resume normal operation after the overload condition is removed.

The current-limit input is also used to communicate faults between the devices in a multiphase configuration. With any fault on the slave or master device (such as UVLO or overtemperature), the ILIM input is pulled low, which causes the other devices to turn off both MOSFETs.

Current Sharing

Accurate current sharing is required in a multiphase converter to prevent some phases from overheating during soft-start, steady-state, and load transient. For a converter with current-mode control, the current is proportional to the error-amplifier output in the voltage feedback loop. The error-amplifier output (COMP) of the master is connected to the current comparator input of all slave devices. The current-sharing accuracy is determined by the tolerances of the inductance and inductor DCR, the input offset voltage, the gain of the current-sense amplifiers, and the slope compensation circuits.

The peak current-mode control is an open-loop current-sharing scheme, and therefore no compensation for current sharing is needed and no stability issue exists.

Switching Frequency and Ramp Generation (FREQ)

The MAX8686 has an adjustable internal oscillator that can be set to any frequency from 300kHz to 1MHz. To set the switching frequency, connect a capacitor from the FREQ to GFREQ (see *Setting the Switching Frequency* section).

A triangle ramp from 0 to AVL/2 is generated across FREQ capacitor. In a multiphase application, the capacitor needs to be connected to the master device. The FREQ inputs of the master and slave devices need to be connected together. FREQ is internally pulled down to GFREQ during shutdown.

Phase Selection Input (PHASE/REFO)

For single-phase or master device operation, the PHASE/REFO can be used as a reference for the converter output voltage (see the *Reference Output (PHASE/REFO)/Reference Input (REFIN)* section). For multiphase operation, connect the PHASE/REFO of each slave device to the center tap of the resistor-divider from AVL of the master to GND. The resistor values are selected to set delay time between phases (see the *Calculating the Phase Voltage* section). The PWM clock cycle of slave devices starts 60ns after the rising edge of the voltage at FREQ crosses the voltage at PHASE/REFO. The PWM clock cycle of the master device starts at the beginning of the ramp.

Remote Sense Input (RS+, RS-)

For single-phase or master operation, connect RS+ to the sense point at the load and RS- to the GND sense point of the load. The connections should be at the output regulation point to eliminate the voltage-sense error caused by voltage drop between the device and load. The RS+ and RS- traces should be laid out in parallel to reduce noise coupling. A common-mode filter to each sense trace should be added if further noise reduction is needed.

For an output voltage higher than 3.3V, tie PHASE/REFO to REFIN and use a resistor-divider from the output regulation point to the remote sense inputs (RS+, RS-), as shown in Figure 1b.

For multiphase operation, connect RS+ and RS- to AVL (slave) to select the slave mode.

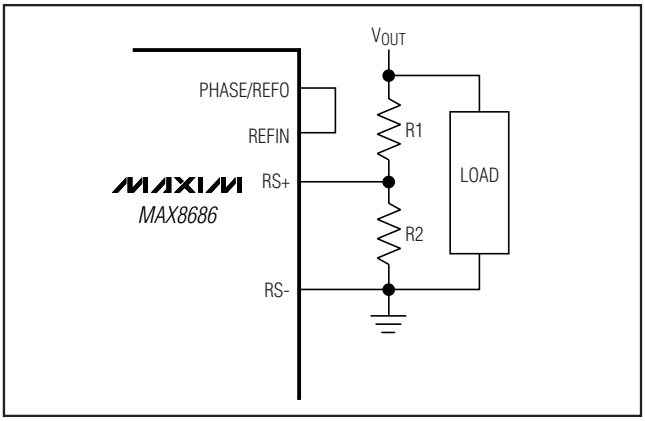

Figure 1b. Output Voltage Above 3.3V

Single/Multiphase, Step-Down, DC-DC Converter Delivers Up to 25A Per Phase

Overvoltage Protection

The MAX8686 provides output overvoltage protection (OVP). The OVP threshold is set at 20% above the set output voltage. When the overvoltage condition is experienced, the output is latched to PGND through the low-side MOSFET. To clear the latch, the EN/SLOPE input should be pulled logic-low and then reinitialized. The output starts up in a soft-start mode. To prevent the overvoltage protection from initializing during power-up, some consideration should be given to the soft-start timing to reduce the inrush current. In addition, the proper compensation network would prevent overshoot during power-up.

Power-OK (POK) Signal

POK is an open-drain output that monitors the output voltage. When the output is above 90% of its nominal regulation voltage, POK goes high impedance. There is a 3% hysteresis to prevent the POK output from chattering. The POK indicator can be used for sequencing.

Thermal-Overload Protection

Thermal-overload protection limits total power dissipation in the MAX8686. When the junction temperature exceeds +160°C, an internal thermal sensor shuts down the device, allowing it to cool down. The thermal sensor turns the device on again after the junction temperature cools by 30°C, resulting in a pulsed output during continuous thermal-overload conditions. See Figures 2, 3, and 4.

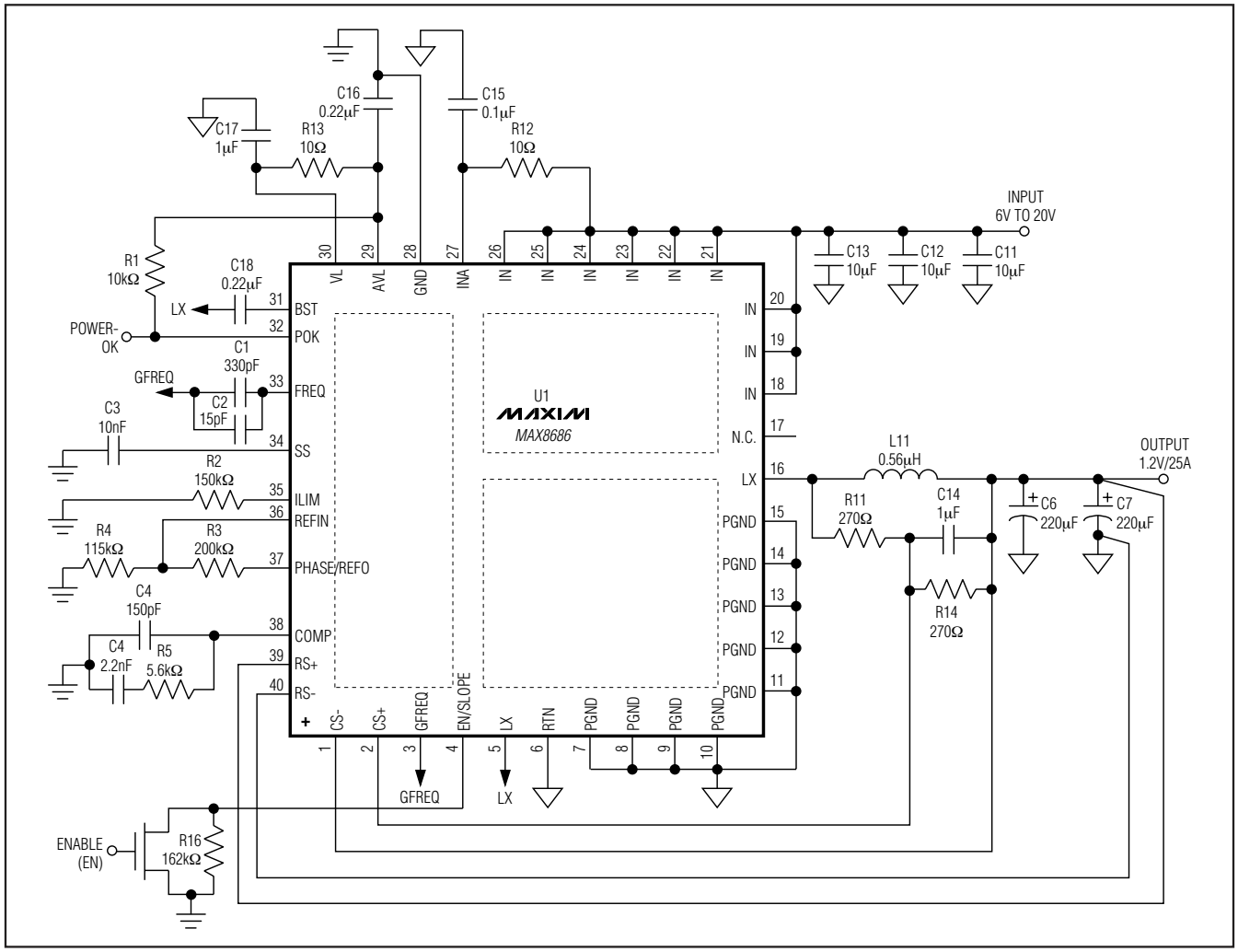

Figure 2. Single-Phase Application Circuit Operating at V_{IN} = 12V

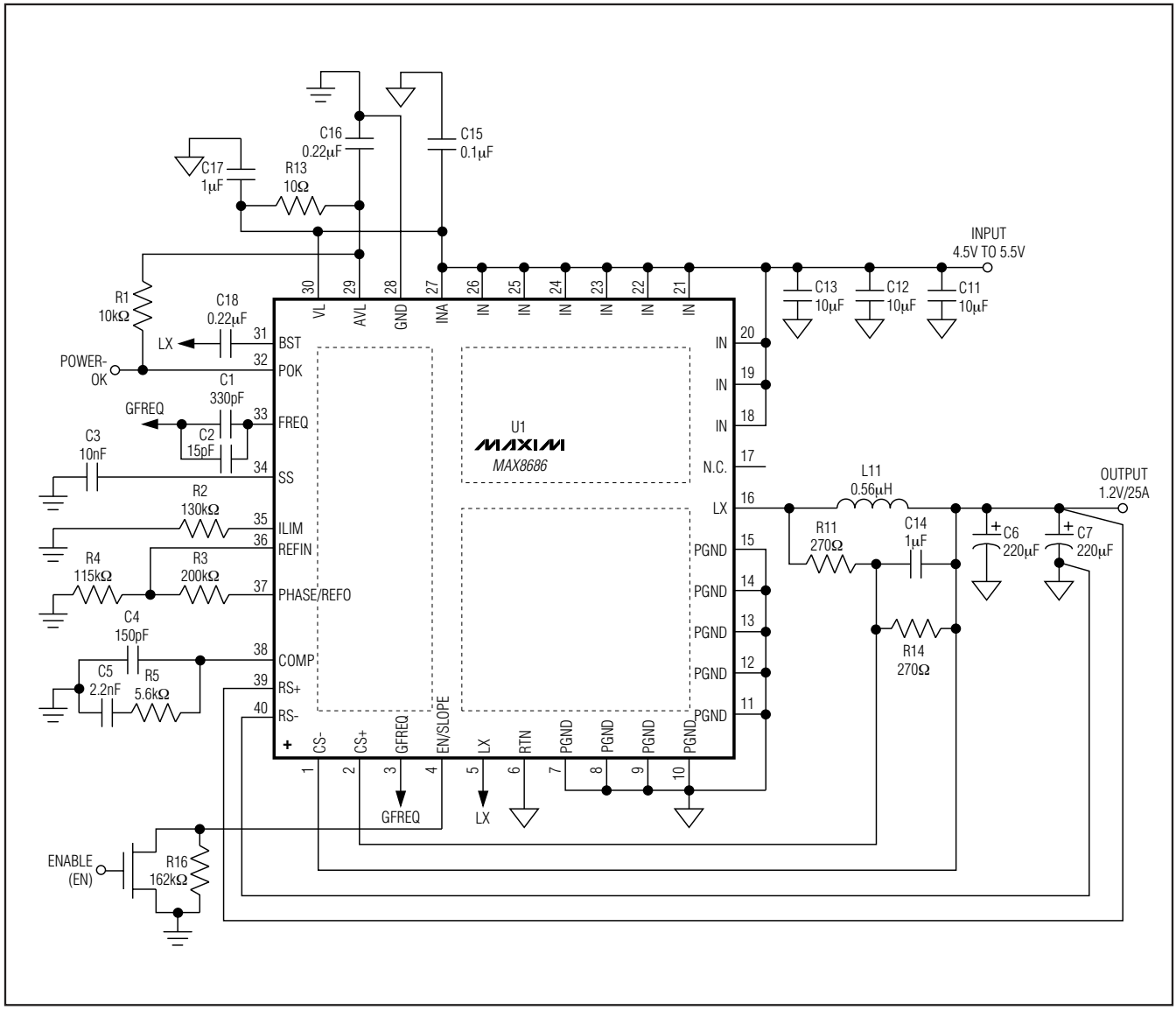

Figure 3. Single-Phase Application Circuit Operating at V_{IN} = 5V

Single/Multiphase, Step-Down, DC-DC Converter Delivers Up to 25A Per Phase

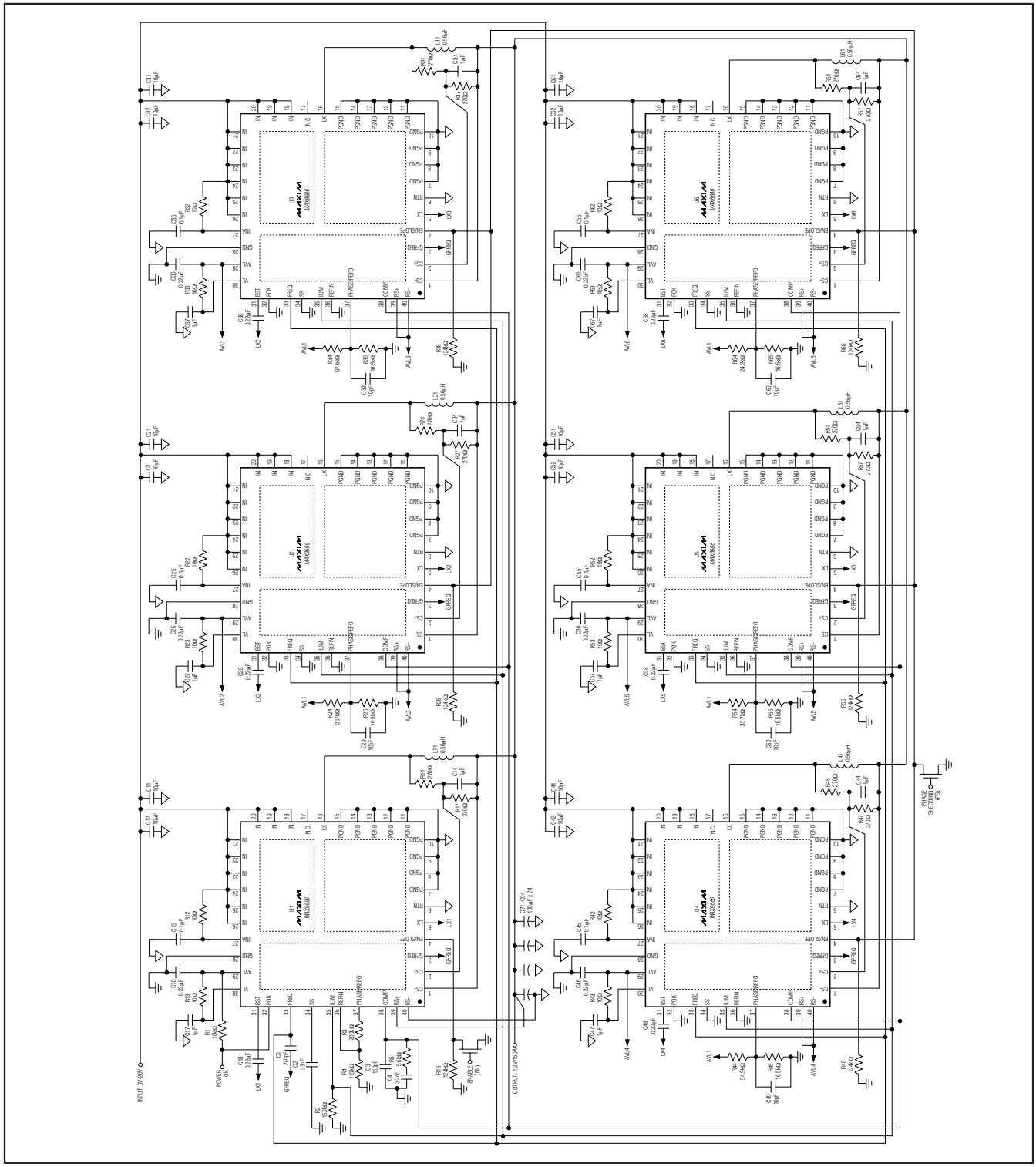

Figure 4. Multiphase Application at V_{IN} = 12V

Design Procedures

Setting the Output Voltage

To set the output voltage for the MAX8686, connect REFIN to the center of an external resistor-divider from PHASE/REFO to GND (R3 and R4 of Figures 2, 3, or 4). The sum of R3 and R4 should exceed 165kΩ.

Preselect R4 and calculate R3 using the following equation:

$$R3 = R4 \times \left(\frac{3.3}{V_{OUT}} - 1 \right)$$

where V_{OUT} is the desired output voltage and 3.3V comes from the reference voltage ($V_{PHASE/REFO}$). The resistor-divider should be placed as close as possible to REFIN. If an external reference is used, see the *Reference Output (PHASE/REFO)/Reference Input (REFIN)* section for more details.

Inductor Selection

The output inductor is selected based on the desired amount of inductor ripple current. A larger inductance value minimizes output ripple current and increases efficiency but slows down the output-inductor-current slew rate during a load transient. LIR is the ratio of ripple current to the total current per phase. For the best tradeoff of efficiency and transient response, an LIR of 30% to 60% is recommended (LIR = 0.3 to 0.6). Choose a higher LIR when more phases are used to take advantage of ripple-current cancellation. The inductor value is determined from:

$$L \geq \frac{V_{OUT} \times (1 - D) \times N}{LIR \times f_{SW} \times I_{OUT\_MAX}}$$

where f_{SW} is the per-phase switching frequency, I_{OUT_MAX} is the maximum-rated output current, D is the duty ratio (V_{OUT}/V_{IN}), N is the number of phases, and V_{OUT} is the output voltage. The selected inductor should have low DC resistance, and the saturation current should be greater than the peak inductor current, I_{PEAK}. I_{PEAK} is found from:

$$I_{PEAK} = \frac{I_{OUT\_MAX}}{N} \times \left(1 + \frac{LIR}{2} \right)$$

When the DC resistance (R_{DC}) of the output inductor is used for current sensing, the DC resistance should be selected to ensure a sufficient current-sense signal for robust current-mode control. The following equation can be used as a guideline.

$$\frac{I_{OUT\_MAX}}{N} \times LIR \times R_{DC} \geq 10mV$$

where R_{DC} is the sense resistance value of the inductor or sense resistor at the highest operating temperature.

It is also important to choose lower LIR to keep the current-sense signal below 45mV, which is the maximum current limit:

$$\frac{I_{OUT\_MAX}}{N} \left[1 + \frac{LIR}{2} \right] \times R_{DC} \leq 45mV$$

If this condition is not met, then the LIR must be adjusted or the input signal to the current-sense amplifier must be scaled down with a resistor-divider.

Setting the Switching Frequency

To set the switching frequency, connect a capacitor from FREQ to GFREQ. Calculate the capacitor value from the following equation:

$$C_{FREQ} = \frac{5 \times 10^5 - 30 \times f_{SW}}{2.7 \times f_{SW}}$$

where f_{SW} is the desired switching frequency in kilohertz and C_{FREQ} is the total capacitance in picofarads. The operating frequency range is from 300kHz to 1MHz, so the capacitance at FREQ should be between 600pF and 180pF. Parasitic capacitance from device pads and PCB layout should be deducted from the above calculation especially at high switching frequencies. In the estimation of parasitic capacitance, 15pF per phase should be used. GFREQ may be connected to GND (quiet ground).

Setting the Slope Compensation

For most applications where the duty cycle is less than 40%, set EN/SLOPE = 1.25V. For applications with a duty cycle greater than 40%, set the slope compensation with a resistor (R_{SLOPE}) from EN/SLOPE to GND.

Calculate the R_{SLOPE} using the following formula:

$$R_{SLOPE} = \frac{1.22 \times 10^7 R_{DC}}{f_{SW} \times L} \times \left(V_{OUT} - 0.182 \times V_{IN\_MIN} \right)$$

where R_{DC} is the DC resistance of the inductor, V_{IN_MIN} is the minimum operating input voltage, and f_{SW} is the switching frequency.

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Setting the Peak Current Limit

The peak current-limit threshold (V_{CS+} - V_{CS-}) is set by a resistor connected from ILIM to GND. An internal 10µA current source flows through this resistor to set a voltage that is 61 times higher than the current-limit threshold. For example, a 300kΩ resistor sets the current-limit threshold at (10µA x 300kΩ)/61 or 49mV:

$$V_{TH} = V_{CS+} - V_{CS-} = \frac{10 \times R_{ILIM}}{61}$$

where R_{ILIM} is in kilohms, V_{TH} is in millivolts, and corresponds to the peak voltage across the sensing element (inductor resistance or current-sense resistor).

This allows a maximum average DC output current of (ILIM):

$$I_{LIM} = \frac{V_{TH}}{R_{DC}} - \frac{I_{P-P}}{2}$$

where R_{DC} is the DC resistance of the inductor or sense resistor and I_{P-P} is the peak-to-peak inductor current.

To ensure maximum output current, use the minimum value of V_{TH} from each setting and the maximum R_{DC} values at the highest expected operating temperature. The DC resistance of the inductor's copper wire has a +0.38%/°C temperature coefficient.

When using a sense resistor, the current through the sense resistor sets a voltage compared with the peak current limit.

To provide a more efficient and lower cost design, the current can be measured through the inductor using a DCR method (voltage across the DC resistance of the inductor) as shown in Figure 5.

An RC circuit is connected across the inductor. The RC time constant is set to be 1.1 to 1.2 times the inductor time constant (L/R_{DC}). Pick the value of C1 in the 1µF to 4.7µF range, and then calculate R1 from:

$$R1 = \frac{1.2 \times L1}{R_{DC} \times C1}$$

R2 is added in some applications to scale down the current signal. R2 and LIR should be selected to meet the following condition.

$$\frac{I_{OUT\_MAX}}{N} \times \left(1 + \frac{LIR}{2}\right) \times R_{DC} \times \frac{R2}{R1 + R2} \le 45mV$$

Calculating the Phase Voltage

In the multiphase converter, the phases are interleaved to reduce the output voltage ripple. The master starts conduction at the beginning of the FREQ ramp. The phase delay time, t_{PHASE}, is the conduction delay time of slaves from the master. Determine the phase delay time as follows:

$$t_{PHASEX} = \frac{X}{f_{SW} \times 10^3 \times N}$$

where X is the number of the slave (X = 1 to 5 for 6 phase converters) f_{SW} is the switching frequency per phase in kilohertz, and N is the total number of phases. Calculate the phase voltage of each slave from:

$$V_{PHASEX} = \frac{t_{PHASEX} \times 5 \times 10^8 - 30}{C_{FREQ}}$$

where C_{FREQ} is the total capacitance (in picofarads) at FREQ (see the *Setting the Switching Frequency* section). For better jitter immunity, V_{PHASE} should be limited between 0.3V and 2.5V.

Then determine resistor-divider for each slave. Preselect more than 10kΩ for phase resistor RX5 (X = 2 to 6, R25, R35, R45, R55, and R65) in Figure 4, and calculate RX4 (R24, R34, R44, R54, and R64) as follows:

$$RX4 = RX5 \times \frac{5.4V - V_{PHASE(X)}}{V_{PHASE(X)}}$$

Input Capacitor

The input capacitor reduces the peak current drawn from the power source and reduces the noise and voltage ripple on the input DC voltage bus caused by the circuit's switching. The input capacitors must meet the

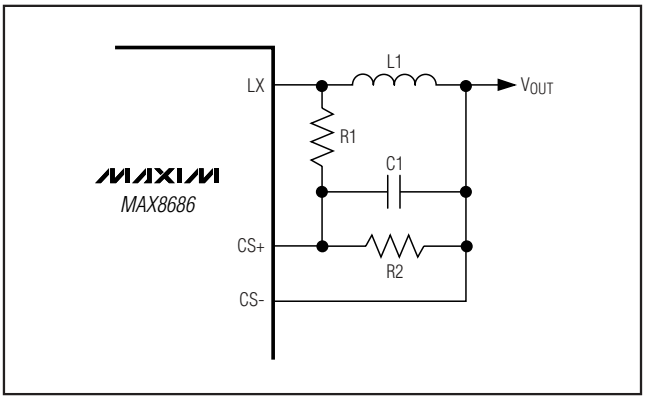

Figure 5. Current Sense Using the Inductor's DC Resistance

ripple-current requirement (I_{RMS}) imposed by the switching currents as defined by the following equations:

$$I_{RMS} = D \times I_{OUT\_MAX} \times \sqrt{\frac{1}{N \times D} - 1}$$

for (N x D) ≤ 1:

$$I_{RMS} = D \times I_{OUT\_MAX} \times \sqrt{\frac{3}{N \times D} - \frac{2}{(N \times D)^2} - 1}$$

for (N x D) > 1.

where N is the number of phases, D is the duty cycle, and I_{OUT_MAX} is the maximum output current.

Use the minimum input voltage for calculating the duty cycle to obtain the worst-case input-capacitor RMS ripple current. Low-ESR aluminum electrolytic, polymer, or ceramic capacitors should be used to avoid large voltage transients at the input during a large step load change at the output. The ripple-current specifications provided by the manufacturer should be carefully reviewed for temperature derating. Additional small-value, low-ESL ceramic capacitors (1µF to 10µF with proper voltage rating) can be used in parallel to reduce any high-frequency ringing.

Output Capacitor

The minimum output capacitance, $C_{OUT(MIN)}$, is required to meet load-dump requirements. The worst-case load dump is a sudden transition from full load current ($I^2_{OUT\_MAX}$) to minimum load current ($I^2_{OUT\_MIN}$). $C_{OUT(MIN)}$ is estimated based on energy balance from:

$$C_{OUT(MIN)} \geq \frac{\frac{L}{N} \times \left(I^2_{OUT\_MAX} - I^2_{OUT\_MIN}\right)}{\left(V_{FIN} + V_{OV}\right)^2 - V_{INIT}{}^2}$$

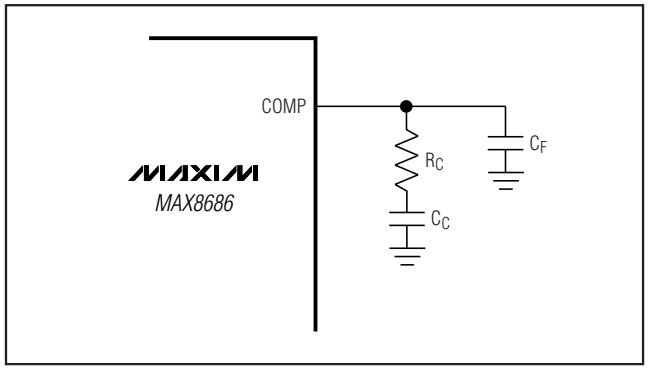

Figure 6. Compensation Components

where $I^2_{OUT\_MAX}$ and $I^2_{OUT\_MIN}$ are the initial and final values of the load current during the worst-case load dump, $V_{INIT}{}^2$ is the voltage prior to the load dump, V_{FIN} is the steady-state voltage after the load dump, and V_{OV} is the allowed voltage overshoot above V_{FIN}. The term (V_{FIN} + V_{OV}) represents the maximum transient output voltage reached during the load dump. The above equation is an approximation, and the output capacitance value obtained serves as a good starting point. The final value should be obtained from actual measurements. For ceramic output capacitors, the output capacitor requirement is determined mostly by load dump requirements due to their low ESR and ESL. See Figures 7 and 8.

Compensation Design

The MAX8686 uses an internal transconductance error amplifier whose output compensates the control loop. The external inductor, output capacitor, compensation

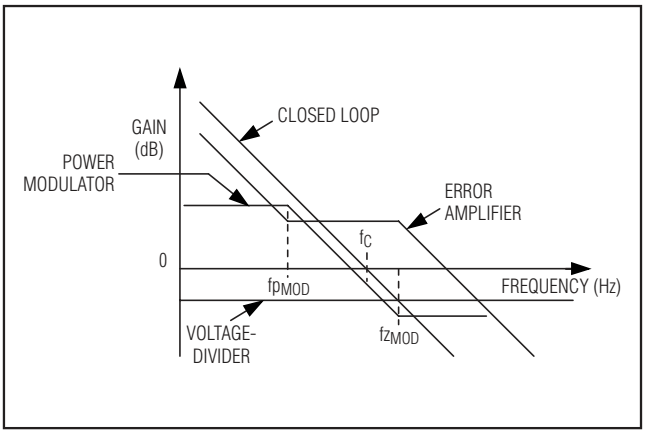

Figure 7. Simplified Gain Plot for the $f_{ZMOD} > f_C$ Case

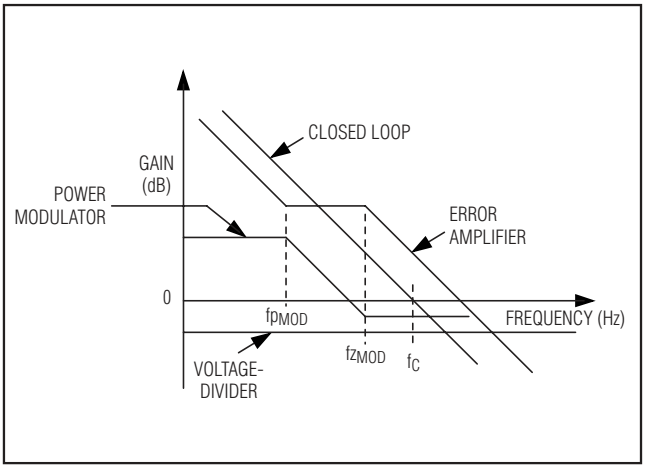

Figure 8. Simplified Gain Plot for the $f_{ZMOD} < f_C$ Case

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resistor, and compensation capacitors determine the loop stability. The inductor and output capacitor are chosen based on performance, size, and cost. Additionally, the compensation resistor and capacitors are selected to optimize control-loop stability. The component values, shown in Figures 2, 3, and 4, yield stable operation over the given range of input-to-output voltages.

The regulator uses a current-mode control scheme that regulates the output voltage by forcing the required current through the external inductor. The voltage drop across the DC resistance of the inductor or the alternate series current-sense resistor is used to measure the inductor current. Current-mode control eliminates the double pole in the feedback loop caused by the inductor and output capacitor resulting in a smaller phase shift and requiring a less elaborate error-amplifier compensation than voltage-mode control. A simple series R_C and C_C is all that is needed to have a stable, high-bandwidth loop in applications where ceramic capacitors are used for output filtering. For other types of capacitors, due to the higher capacitance and ESR, the frequency of the zero created by the capacitance and ESR is lower than the desired closed-loop crossover frequency. To stabilize a nonceramic output-capacitor loop, add another compensation capacitor from COMP to GND to cancel this ESR zero. See Figure 6.

The basic regulator loop is modeled as a power modulator, an output feedback divider, and an error amplifier. The power modulator has DC gain set by $g_{mc} \times R_{LOAD}$, with a pole and zero pair set by R_{LOAD}, the output capacitor (C_{OUT}), and its equivalent series resistance (ESR). Below are equations that define the power modulator:

$$G_{MOD(DC)} = g_{mc} \times \frac{R_{LOAD}}{\left[1+\frac{R_{LOAD}}{L \times f_{SW}} \times \left[\left(K_S \times (1-D)\right) - 0.5\right]\right]}$$

where $R_{LOAD} = V_{OUT}/[I_{OUT(MAX)}/N]$, f_{SW} is the switching frequency, L is the output inductance, $g_{mc} = 1/(A_{VCS} \times R_{DC})$, where A_{VCS} is the gain of the current-sense amplifier (30.5 typ), R_{DC} is the DC resistance of the inductor, the duty cycle $D = V_{OUT}/V_{IN}$. K_S is a slope compensation factor calculated from the following equation:

$$K_S = 1 + \frac{V_{OUT} - 0.182 \times V_{IN\_MIN}}{f_{SW} \times L \times (V_{IN} - V_{OUT})}$$

Find the pole and zero frequencies created by the power modulator as follows:

$$f_{pMOD} = \frac{N}{2\pi \times R_{LOAD} \times C_{OUT}} + \left[\frac{N}{2\pi \times L \times f_{SW} \times C_{OUT}} \times \left[K_S \times (1-D) - 0.5\right]\right]$$

$$f_{zMOD} = \frac{1}{2\pi \times C_{OUT} \times ESR}$$

when C_{OUT} comprises "n" identical capacitors in parallel, the resulting $C_{OUT} = n \times C_{OUT(EACH)}$, and $ESR = ESR_{(EACH)}/n$. Note that the capacitor zero for a parallel combination of like capacitors is the same as for an individual capacitor.

The transconductance error amplifier has a DC gain, $G_{EA(DC)} = g_{mEA} \times R_O$, where g_{mEA} is the error-amplifier transconductance, which is equal to 1.7mS, and R_O is the output resistance of the error amplifier, which is 30MΩ. A dominant pole (f_{pdEA}) is set by the compensation capacitor (C_C), the amplifier output resistance (R_O), and the compensation resistor (R_C); a zero (f_{zEA}) is set by the compensation resistor (R_C) and the compensation capacitor (C_C). There is an optional pole (f_{pEA}) set by C_F and R_C to cancel the output capacitor ESR zero if it occurs near the crossover frequency (f_C). Thus:

$$f_{pdEA} = \frac{1}{2\pi \times C_C \times (R_O + R_C)}$$

$$f_{zEA} = \frac{1}{2\pi \times C_C \times R_C}$$

$$f_{pEA} = \frac{1}{2\pi \times C_F \times R_C}$$

The crossover frequency, f_C, should be much higher than the power-modulator pole f_{PMOD}. Also, f_C should

be less than or equal to 1/5 the switching frequency. Select a value for f_C in the range:

$$f_{pMOD} << f_C \le \frac{f_{SW}}{5}$$

The feedback voltage-divider gain (V_{REF}/V_{OUT}) should be included for an output voltage higher than 3.3V, where V_{REFIN} is equal to 3.3V.

At the crossover frequency, the total loop gain must equal 1, and is expressed as:

$$G_{EA(fc)} \times G_{MOD(fc)} \times \frac{V_{REFIN}}{V_{OUT}} = 1$$

For the case where f_{zMOD} is greater than f_C:

$$G_{EA(fc)} = g_{mEA} \times R_C$$

$$G_{MOD(fc)} = G_{MOD(dc)} \times \frac{f_{pMOD}}{f_C}$$

Then R_C can be calculated as:

$$R_C = \frac{V_{OUT}}{g_{mEA} \times V_{REFIN} \times G_{MOD(fc)}}$$

where g_{mEA} = 1.7mS.

The error-amplifier compensation zero formed by R_C and C_C should be set at the modulator pole f_{PMOD}. Calculate the value of C_C as follows:

$$C_C = \frac{1}{2\pi \times f_{pMOD} \times R_C}$$

If f_{PMOD} is less than 5 x f_C, add a second capacitor C_F from COMP to GND. The value of C_F is:

$$C_F = \frac{1}{2\pi \times R_C \times f_{zMOD}}$$

As the load current decreases, the modulator pole also decreases; however, the modulator gain increases accordingly and the crossover frequency remains the same.

For the case where f_{zMOD} is less than f_C:

The power modulator gain at f_C is:

$$G_{MOD(fc)} = G_{MOD(dc)} \times \frac{f_{pMOD}}{f_{zMOD}}$$

The error-amplifier gain at f_C is:

$$G_{EA(fc)} = g_{mEA} \times R_C \times \frac{f_{zMOD}}{f_C}$$

R_C is calculated as:

$$R_C = \frac{V_{OUT}}{V_{FB}} \times \frac{f_C}{g_{mEA} \times G_{MOD(fc)} \times f_{zMOD}}$$

where g_{mEA} = 1.7mS.

C_C is calculated from:

$$C_C = \frac{1}{2\pi \times f_{pMOD} \times R_C}$$

C_F is calculated from:

$$C_F = \frac{1}{2\pi \times R_C \times f_{zMOD}}$$

The current-mode control model on which the above design procedure is based requires an additional high-frequency term, $G_S(s)$, to account for the effect of sampling the peak inductor current. The term $G_S(s)$ produces additional phase lag at crossover and should be modeled to estimate the phase margin obtainable by the selected compensation components. As a final step, it is useful to plot the dB gain and phase of the following loop-gain transfer function and check the obtained phase margin. A phase margin of at least 45° is recommended:

$$G_{LOOP}(s) = \frac{R_{LOAD} \times g_{MC}}{\left[1 + \frac{R_{LOAD}}{L \times f_{SW}} \times \left[(Ks \times (1-D)) - 0.5\right]\right]} \times \frac{(1 + s / 2\pi \times f_{zMOD})}{(1 + s / 2\pi \times f_{pMOD})} \times \frac{(1 + s / 2\pi \times f_{zEA})}{(1 + s / 2\pi \times f_{pEA}) \times (1 + s / 2\pi \times f_{pdEA})} \times \frac{g_{mEA} \times Ro \times V_{REFIN}}{V_{OUT}} G_S($$

$$G_S(s) = \frac{1}{\left(1 + \frac{s}{\pi \times Q_c \times f_{SW}} + \frac{s^2}{(\pi \times f_{SW})^2}\right)}$$

where the sampling effect quality factor is:

$$Q_C = \frac{1}{\left[\pi \times (K_S \times (1-D) - 0.5)\right]}$$

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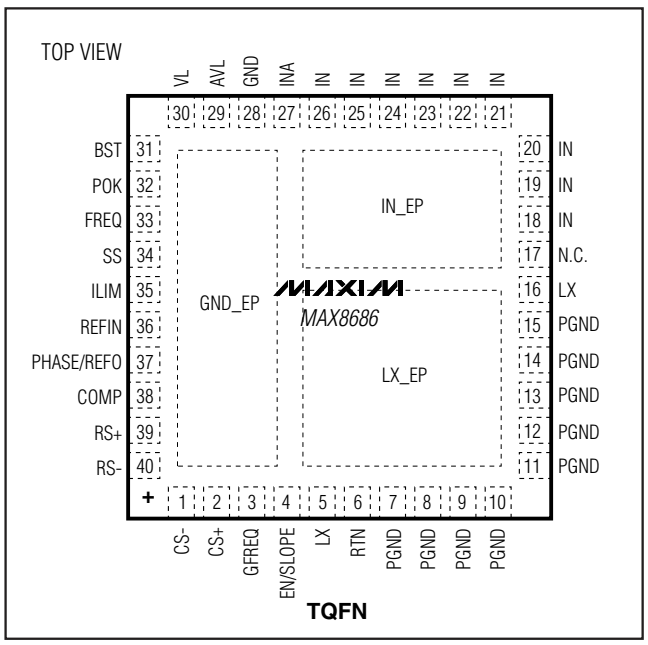
Applications Information

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. The switching power stage requires particular attention. Follow these guidelines for good PCB layout:

1) Place IC decoupling capacitors as close to the IC pins as possible. Separate the power and analog ground planes. Place the input ceramic decoupling capacitor directly across and as close as possible to IN and PGND. This is to help contain the high switching current within this small loop.
2) For output current greater than 10A, a four-layer PCB is recommended. Pour an analog ground plane in the second layer underneath the IC to minimize noise coupling.
3) Connect input and output capacitor to the PGND plane and the VL capacitor to RTN. Connect all analog signals to GND. The frequency-setting capacitor should be connected to GFREQ.
4) Connect PGND, GND, and RTN at the return path of the input bypass capacitor.
5) Signals shared by the master and slave (ILIM, COMP, and FREQ) should not run close to switching signals.
6) Place the inductor current-sense resistor and capacitor as close to the inductor as possible. Make a Kelvin connection to minimize the effect of PCB trace resistance.
7) Connect the exposed pad sections to the corresponding IC pins and allow sufficient copper area to help cooling the device.
8) Place the REFIN and compensation components as close to the IC pins as possible.
9) Connect remote-sense input RS+ and RS- directly to the load voltage regulation point and use Kelvin connection for the two traces.
10) Refer to the MAX8686 Evaluation Kit for an example layout.

Pin Configuration



Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
40 TQFN	T4066M+1	21-0177
40 TQFN	T4066MN+1	21-0177

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/08	Initial release	—
1	10/10	Modified TOC 5, Figure 4, *Setting the Switching Frequency* section, *Calculating the Phase Voltage* section, and the *Compensation Design* section	5, 16, 17, 18, 21