Using the CSD86330EVM-717

User's Guide

Texas Instruments

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User's Guide

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Synchronous Buck NexFET Power Block

1 Introduction

The CSD86330EVM-717 evaluation module (EVM) uses the CSD86330. The CSD86330 power block is an optimized design for synchronous buck applications offering high-current, high-efficiency, and high-frequency capability in a small 3.3-mm x 3.3-mm outline. CSD86330EVM-717 also uses TPS53219 as a small size single-buck controller with adaptive on-time D-CAP ™ mode control. The EVM provides a fixed 1.2-V output at up to 10 A from a 12-V input bus.

2 Description

The CSD86330EVM-717 is designed to use a regulated 12-V bus to produce a regulated 1.2-V output at up to 10 A of load current. The CSD86330EVM-717 is designed to demonstrate the CSD86330 device in a typical low-voltage application while providing test points to evaluate the performance of the board.

2.1 Typical Applications

- Point-of-Load Systems
- Storage Computer
- Server Computer
- Multi-Function Printer
- Embedded Computing

2.2 Features

The CSD86330EVM-717 features:

- 10-A DC Steady State Output Current
- High Efficiency and High-Power Density by Using TI Power Block MOSFET (CSD86330)
- Convenient Test Points for Probing Critical Waveforms

3 Electrical Performance Specifications

Table 1. CSD86330EVM-717 Electrical Performance Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Characteristics					
Voltage range	VIN	9	12	13.2	V
Maximum input current	VIN = 9 V, I_O = 10 A		1.6		A
No load input current	V_{IN} = 13.2 V, I_O = 0 A		1		mA
Output Characteristics					
Output voltage VOUT	I_O = 5 A	1.164	1.2	1.236	V
Output voltage regulation	Line regulation(V_{IN} = 9 V 13.2 V. I_O=0 A - 10 A)		0.5%		
	Load regulation(V_{IN} = 12 V, I_O = 0 A - 10 A)		0.5%		
Output voltage ripple	V_{IN} = 12 V, I_O = 10 A		40		mV_{PP}
Output load current		0		10	A
Output over current			12		
Systems Characteristics					
Switching frequency			500		kHz
Peak efficiency	V_{IN} = 9 V, 1.2 V/5 A		92%		
Full load efficiency	V_{IN} = 12 V, 1.2 V/10 A		89.4%		
Operating temperature			25		°C

4 Schematic

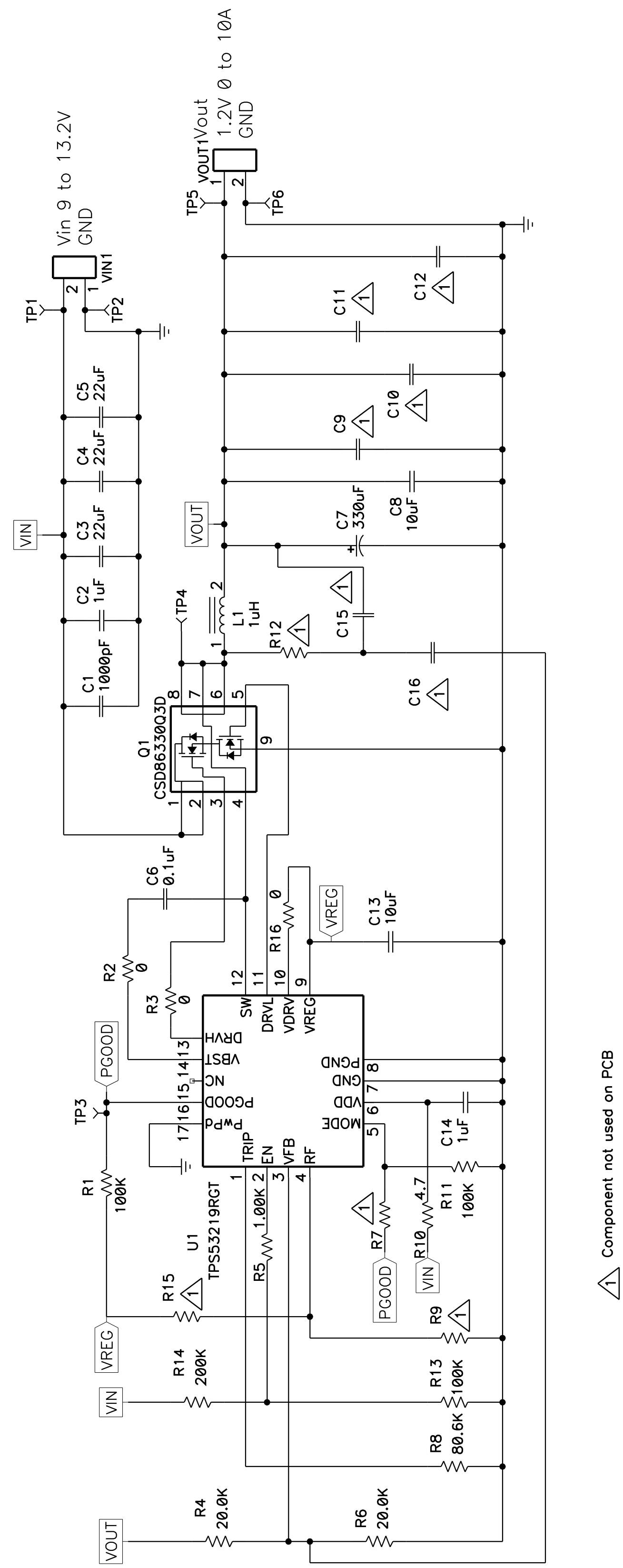

Figure 1. CSD86330EVM-717 Schematic

5 Test Setup

5.1 Test Equipment

Voltage Source: The input voltage source V_{IN} should be a 0-V to 13.2-V variable DC source capable of supplying 4 A_{DC}. Connect V_{IN} to board as shown in Figure 3.

Multimeters:

- V1: V_{IN} at TP1 (V_{IN}) and TP2 (GND).
- V2: V_{OUT} at TP5 (V_{OUT}) and TP6 (GND).
- A1: V_{IN} input current.

Output Load: The output load should be an electronic constant resistance mode load capable of 0 A_{DC} to 10 A_{DC} at 1.2 V.

Oscilloscope: A digital or analog oscilloscope can be used to measure the output ripple. The oscilloscope should be set for 1-MΩ impedance, 20-MHz bandwidth, AC coupling, 1-µs/division horizontal resolution, 50-mV/division vertical resolution. Test points TP5 and TP6 can be used to measure the output ripple voltage by placing the oscilloscope probe tip through TP5 and holding the ground barrel TP6 as shown in Figure 2. Using a leaded ground connection may induce additional noise due to the large ground loop.

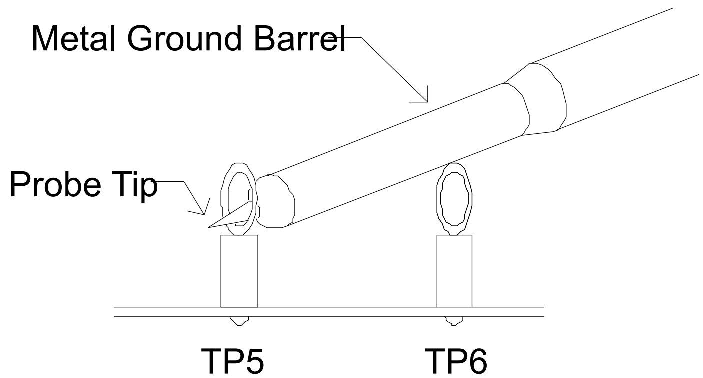

Figure 2. Tip and Barrel Measurement for V_{OUT} Ripple

Fan: Some of the components in this EVM may approach temperatures of 60°C during operation. A small fan capable of 200 LFM to 400 LFM is recommended to reduce component temperatures while the EVM is operating. The EVM should not be probed if the fan is not running.

Recommended Wire Gauge:

- **VIN to VIN1(12-V input):** The recommended wire size is 1x AWG #18 per input connection, with the total length of wire less than 4 feet (a 2 foot input and a 2 foot return).

VOUT1 to LOAD: The recommended wire size is 1x AWG #18, with the total length of wire less than 4 feet (a 2 foot input and a 2 foot return).

5.2 Recommended Test Setup

Figure 3 is the recommended test set up to evaluate the CSD86330EVM-717. Working at an ESD workstation, make sure that any wrist straps, bootstraps or mats are connected referencing the user to earth ground before power is applied to the EVM.

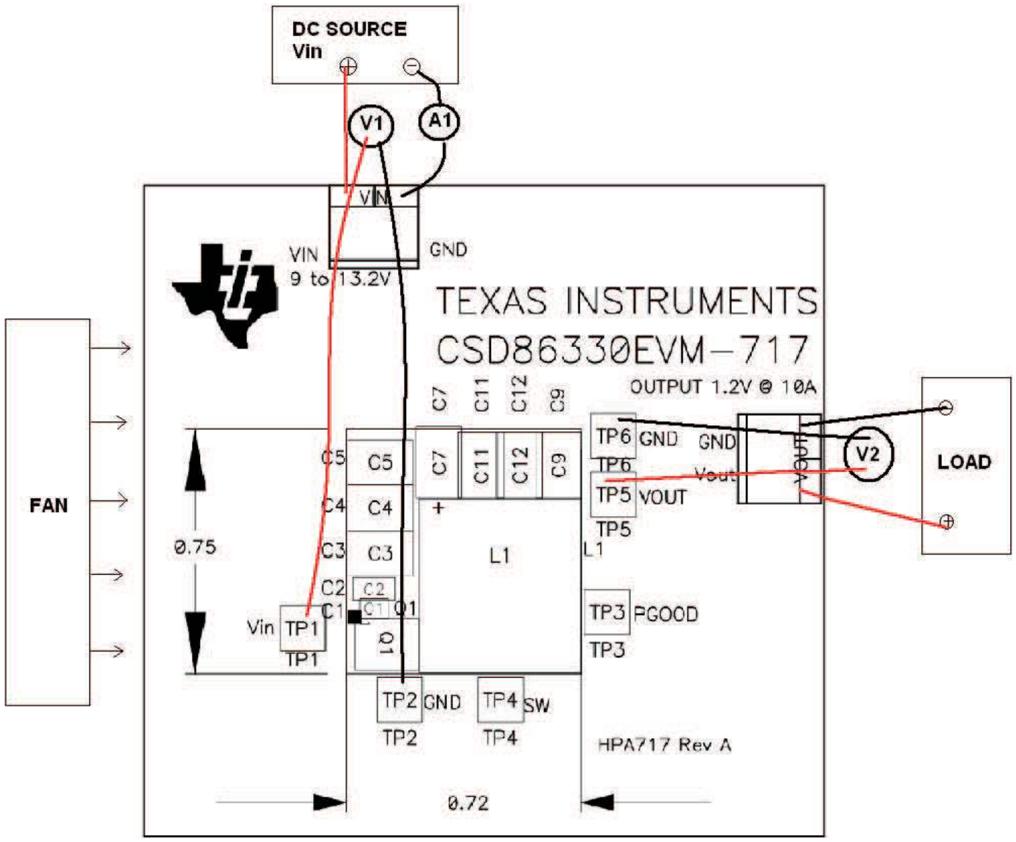

Figure 3. CSD86330EVM-717 Recommended Test Set Up

Input Connections:

- Prior to connecting the DC input source V_{IN}, it is advisable to limit the source current from V_{IN} to 10 A maximum. Make sure V_{IN} is initially set to 0 V and connected as shown in Figure 3.
- Connect a voltmeter V1 at TP1(V_{IN}) and TP2(GND) to measure the input voltage.
- Connect a current meter A1 to measure the input current.

Output Connections:

- Connect load to VOUT1 and set load to constant resistance mode to sink 0 A_{DC} before V_{IN} is applied.
- Connect a voltmeter V2 at TP5 (V_{OUT}) and TP6 (GND) to measure the output voltage.

Other Connections: Place a fan as shown in Figure 3 and turn on, making sure air is flowing across the EVM.

6 Test Procedure

6.1 Line/Load Regulation and Efficiency Measurement Procedure

1. Set up the EVM as described in Section 5 and Figure 3.
2. Ensure load is set to constant resistance mode and to sink 0 A_{DC}.
3. Ensure all configuration settings are as per Section 6.
4. Increase V_{IN} from 0 V to 12 V. Using V1 to measure input voltage.
5. Use V2 to measure V_{OUT} voltage.
6. Vary load from 0 A_{DC} to 10 A_{DC}, V_{OUT} should remain in load regulation.
7. Vary V_{IN} from 9 V to 13.2 V, V_{OUT} should remain in line regulation.
8. Decrease load to 0 A.
9. Decrease V_{IN} to 0 V.

6.2 List of Test Points

Table 2. Test Point Functions

TEST POINTS	NAME	DESCRIPTION
TP1	V_{IN}	Input voltage measurement point
TP2	GND	Ground for V_{IN} measurements
TP3	PGOOD	Power Good monitoring point
TP4	SW	Switch Node monitoring point
TP5	V_{OUT}	Output Voltage measurement point
TP6	GND	Ground for output voltage measurements

6.3 Equipment Shutdown

1. Shut down load
2. Shut down V_{IN}
3. Shut down fan

7 Performance Data and Typical Characteristic Curves

Figure 4 through Figure 11 present typical performance curves for CSD86330EVM-717.

7.1 *Efficiency*

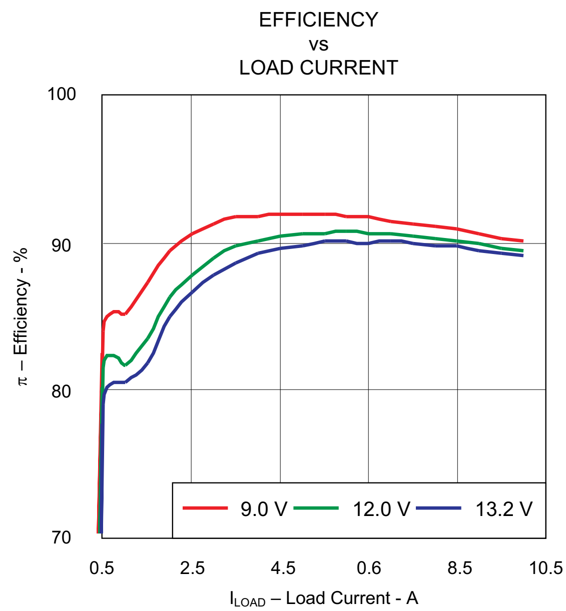

Figure 4. Efficiency

7.2 *Light-Load Efficiency*

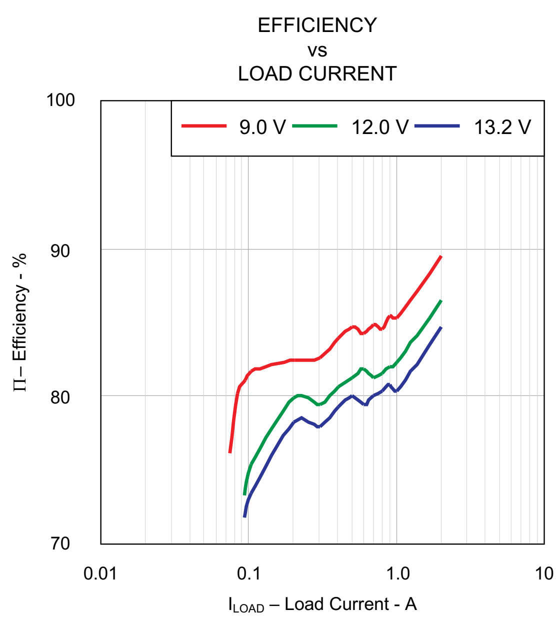

Figure 5. Light-Load Efficiency

7.3 Load Regulation

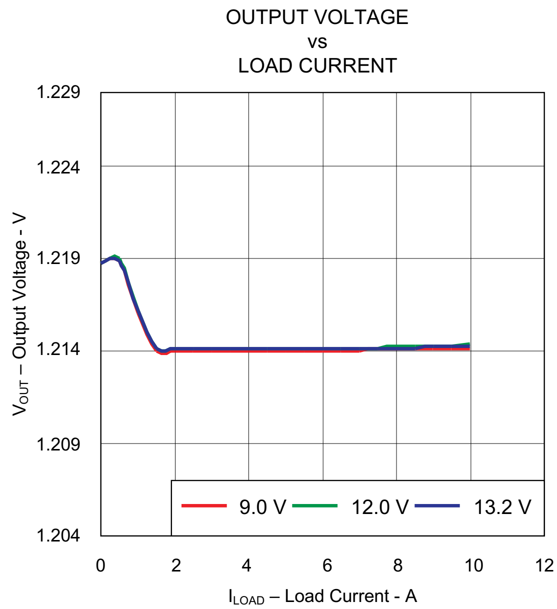

Figure 6. Load Regulation

7.4 Output Transient

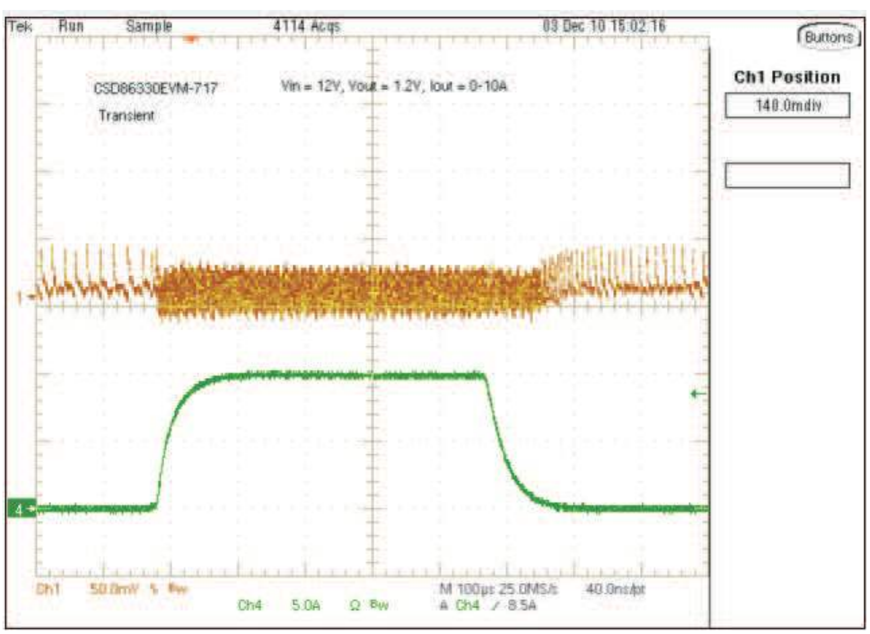

Figure 7. Output-Load Transient

7.5 Output Ripple

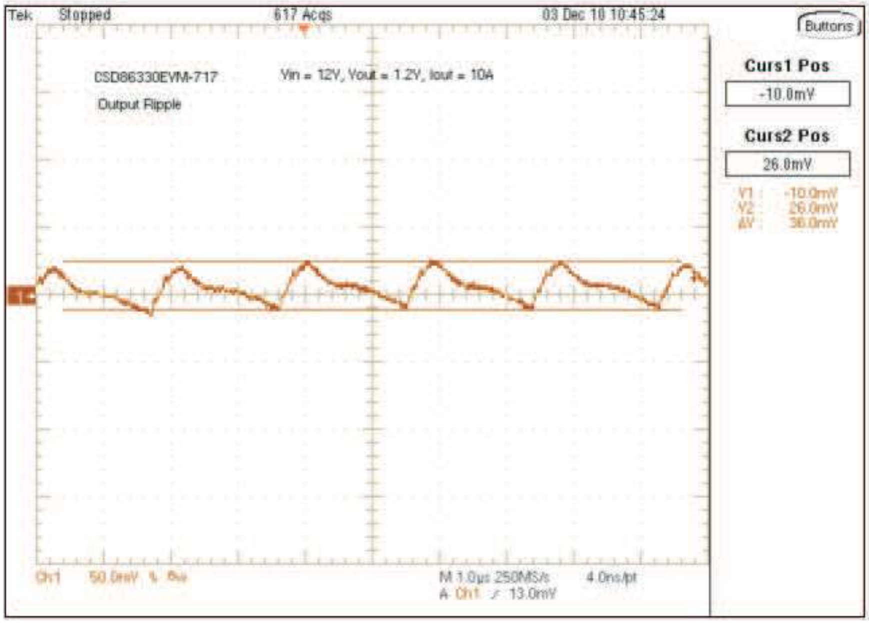

Figure 8. Output Ripple

7.6 Switching Node

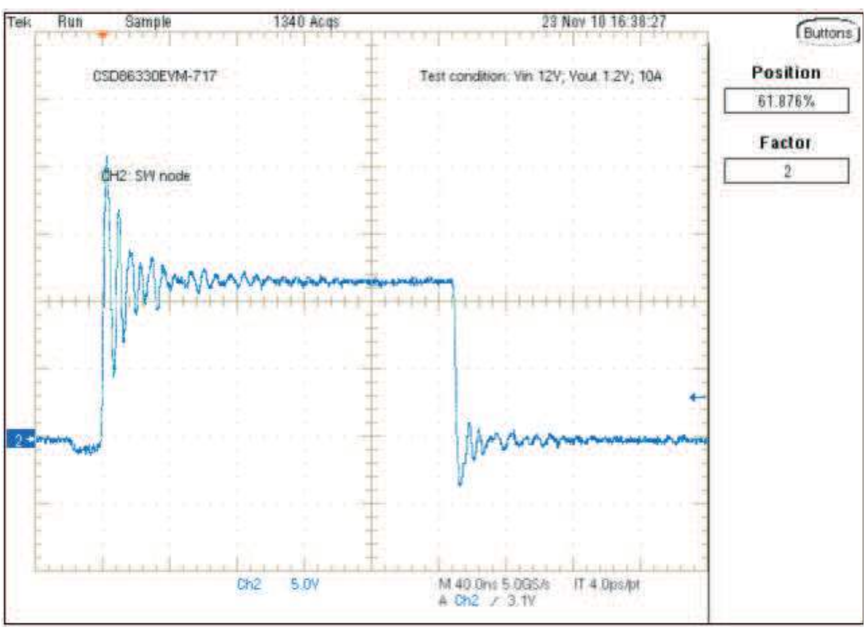

Figure 9. Output Ripple

7.7 Thermal Image

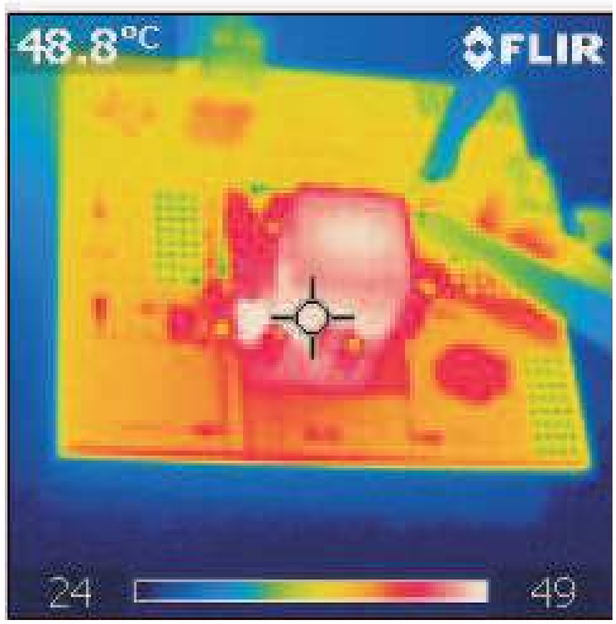

Figure 10. Top Board at 12 V_{IN}, 1.2 V/10 A with natural air convection

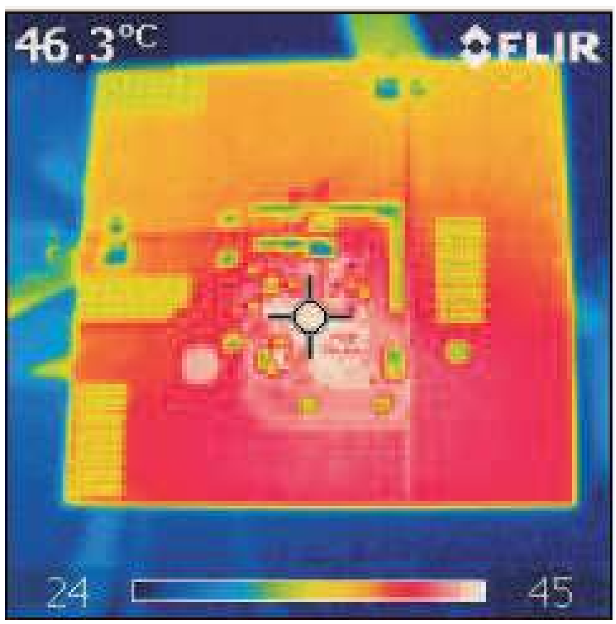

Figure 11. Bottom Board at 12 V_{IN}, 1.2 V/10 A with natural air convection

8 CSD86330EVM-717 Assembly Drawing and PCB Layout

The following figures (Figure 12 through Figure 19) show the design of the CSD86330EVM-717 printed circuit board. The EVM has been designed using six layers and a 2-oz copper circuit board.

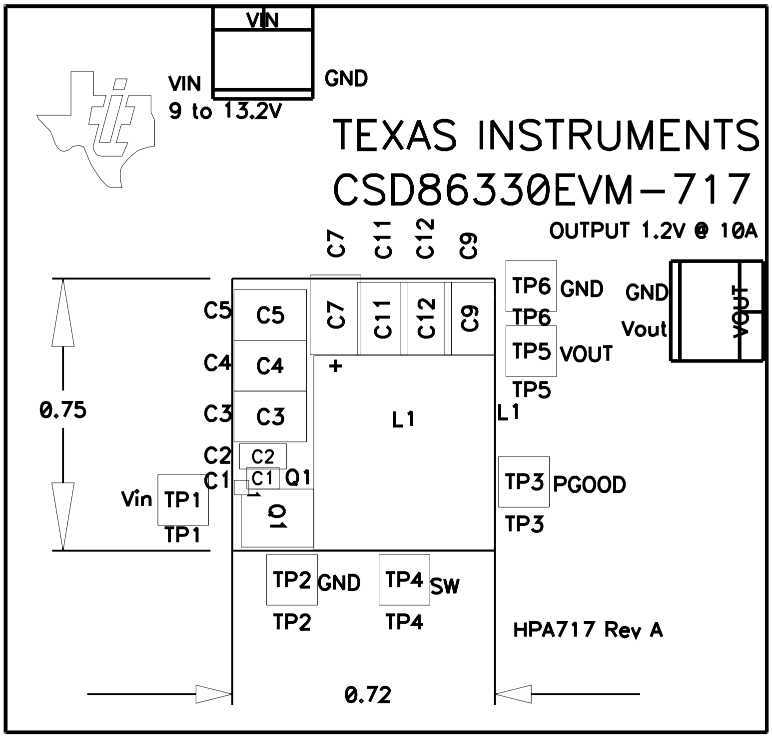

Figure 12. Top Layer Assembly Drawing (top view)

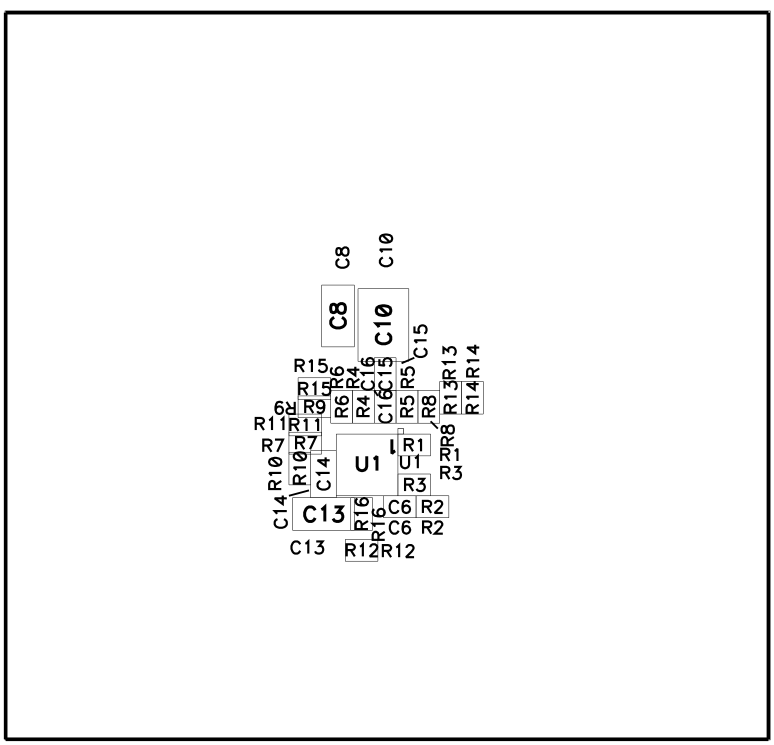

Figure 13. Bottom Layer Assembly Drawing (bottom view)

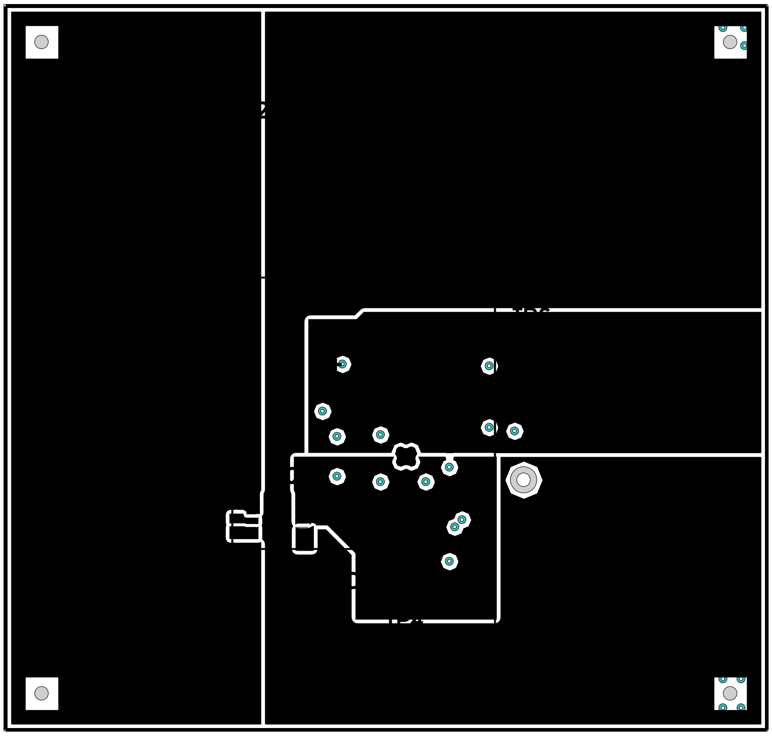

Figure 14. Top Copper

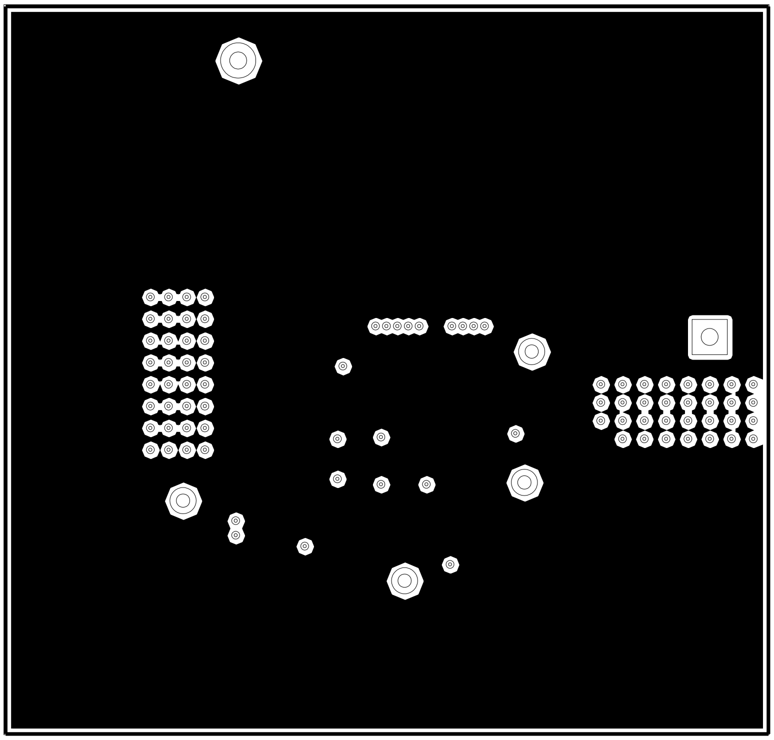

Figure 15. Layer 2

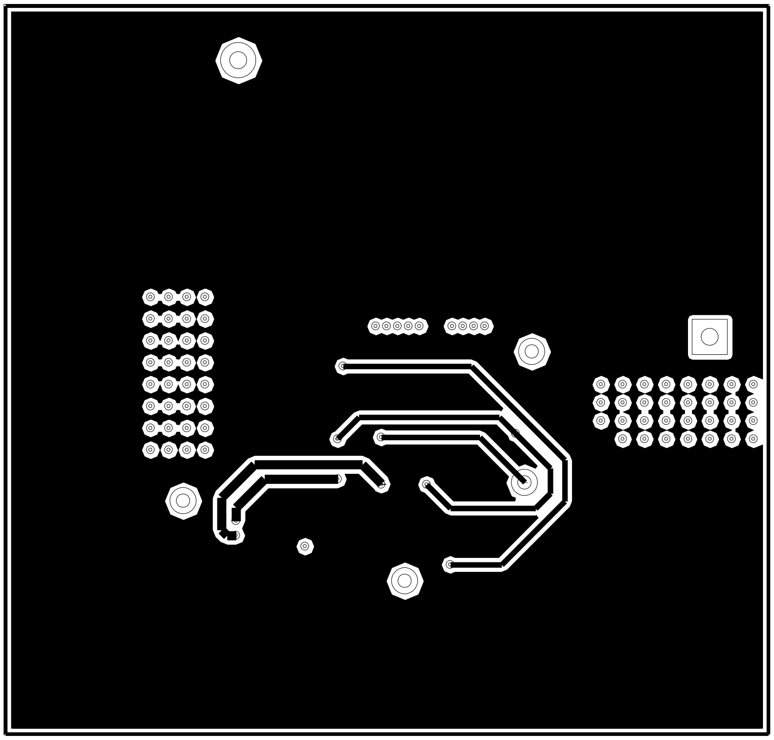

Figure 16. Layer 3

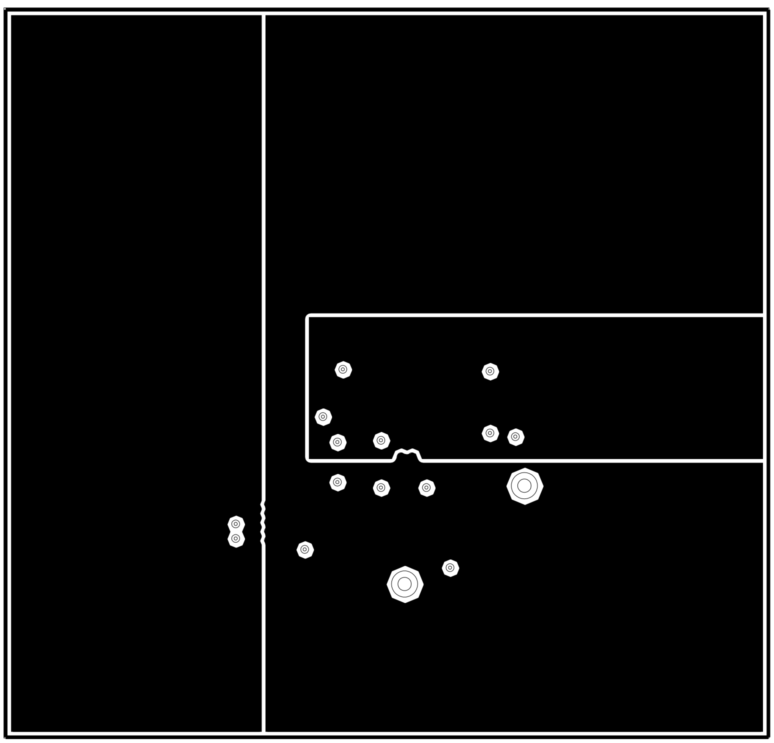

Figure 17. Layer 4

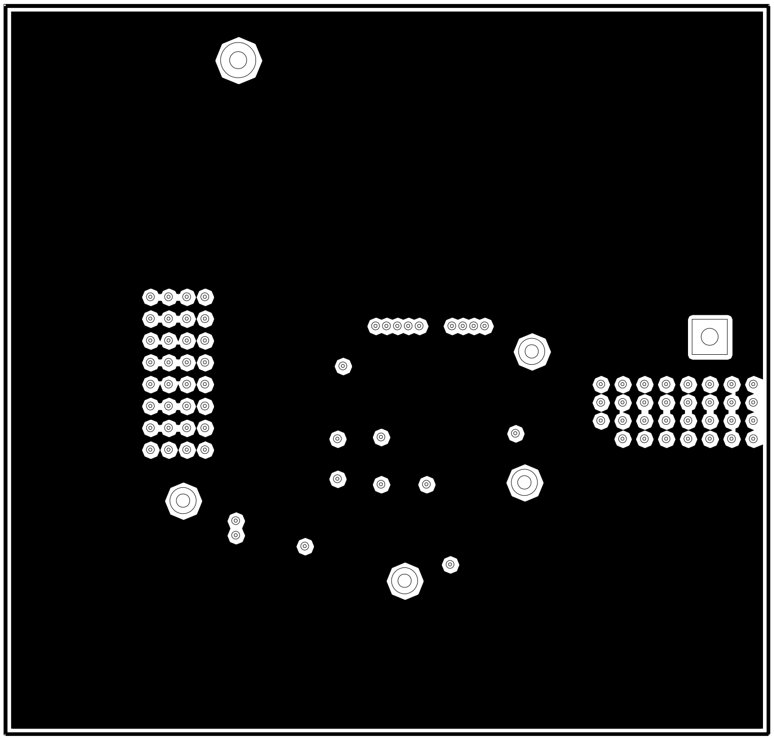

Figure 18. Layer 5

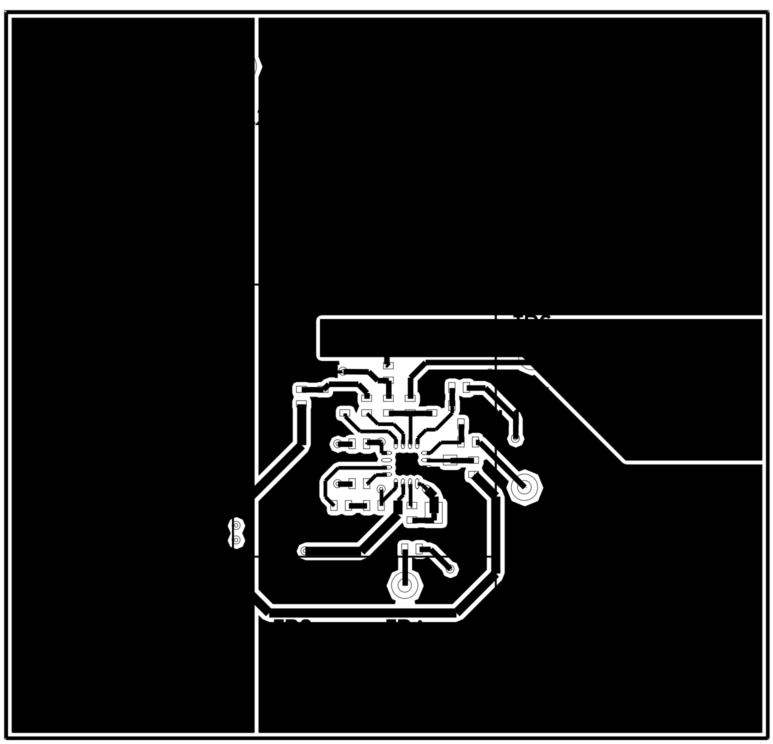

Figure 19. Bottom Layer

9 List of Materials

The EVM components list according to Figure 1.

Table 3. List of Materials

QTY	REF DES	DESCRIPTION	MFR	PART NUMBER
1	C1	Capacitor, ceramic, 25 V, X7R, 10%, 402	Std	Std
2	C2, C14	Capacitor, ceramic, 25 V, X5R, 20%, 603	Std	Std
3	C3, C4, C5	Capacitor, ceramic, 25 V, X5R, 20%, 1210	Std	Std
2	C6	Capacitor, ceramic, 16 V, X7R, 10%, 402	Std	Std
1	C7	Capacitor, POSCAP, 330 µF, 2.5 V, 0.009 Ω, 20%, Case B2805, 3528(B)	Sanyo	2R5TPE330MA9R
2	C8, C13	Capacitor, ceramic, 10 V, X5R, 20%,	Std	Std
0	C9, C10, C11, C12, C15, C16	Capacitor, ceramic, 6.3 V, X5R, 20%, 1210	Std	Std
1	L1	Inductor, SMT, 24 A, 1.17 mΩ, 0.288 inch x 0.288 inch	Wurth Elektronik	7443320100
1	Q1	MOSFET, Synchronous Buck NexFET Power Block, QFN-8 Power	TI	CSD86330Q3D
3	R1, R11, R13	Resistor, chip, 1/16 W, 1%, 402	Std	Std
1	R10	Resistor, chip, 1/16 W, 1%, 402	Std	Std
1	R14	Resistor, chip, 1/16 W, 1%, 402	Std	Std
3	R2, R3, R16	Resistor, chip, 1/16 W, 1%, 402	Std	Std
2	R4, R6	Resistor, chip, 1/16 W, 1%, 402	Std	Std
1	R5	Resistor, chip, 1/16 W, 1%, 402	Std	Std
0	R7, R9, R12, R15	Resistor, chip, 1/16 W, 1%, 402	Std	Std
1	R8	Resistor, chip, 1/16 W, 1%, 402	Std	Std
1	U1	Single Synchronous Step-Down Controller, QFN-16	TI	TPS53219RGT

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 10 VDC to 14 VDC and the output voltage range of 0 ADC to 20ADC.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 100° C. The EVM is designed to operate properly with certain components above 100° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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