LP38859 3-A Fast-Response High-Accuracy LDO Linear Regulator With Soft Start

1 Features

- Input Voltage: 1.1 V to 5.5 V
- Wide V_{BIAS} Supply Operating Range: 3 V to 5.5 V
- Standard V_{OUT} Values: 0.8 V and 1.2 V
- Stable With 10-µF Ceramic Capacitors
- Dropout Voltage of 240 mV (typical) at 3-A Load Current
- Programmable Soft-Start Time
- Precision Output Voltage Across All Line and Load Conditions:
  - ±1% V_{OUT} for T_J = 25°C
  - ±2% V_{OUT} for 0°C ≤ T_J ≤ +125°C
  - ±3% V_{OUT} for –40°C ≤ T_J ≤ +125°C
- Overtemperature and Overcurrent Protection
- Operating Temperature Range: −40°C to +125°C

2 Applications

- ASIC Power Supplies In:
  - Desktops, Notebooks, Graphics Cards, and Servers
  - Gaming Set Top Boxes, Printers, and Copiers
- Server Core and I/O Supplies
- DSP and FPGA Power Supplies
- SMPS Post-Regulator

3 Description

The LP38859 is a high-current, fast-response regulator which can maintain output voltage regulation with extremely low input to output voltage drop. Fabricated on a CMOS process, the device operates from two input voltages: V_{BIAS} provides voltage to drive the gate of the N-MOS power transistor, while V_{IN} is the input voltage which supplies power to the load. The use of an external bias rail allows the part to operate from ultra-low V_{IN} voltages. Unlike bipolar regulators, the CMOS architecture consumes extremely low quiescent current at any output load current. The use of an N-MOS power transistor results in wide bandwidth, yet minimum external capacitance is required to maintain loop stability.

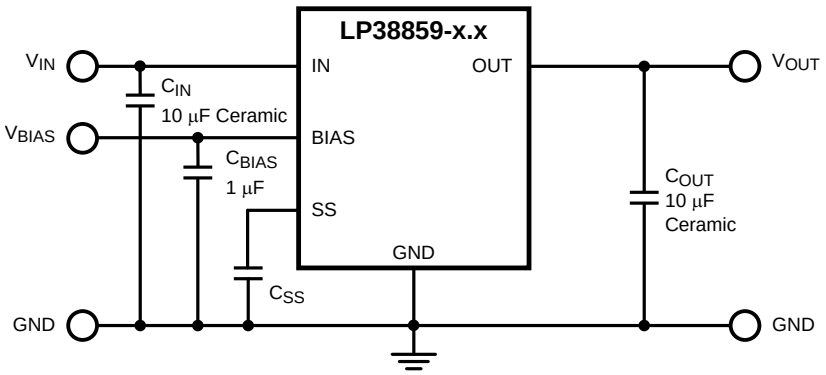
The fast transient response of this device makes it suitable for use in powering DSP microcontroller core voltages and switch-mode power-supply post-regulators. The LP38859 is available in 5-pin TO-220 and DDPAK/TO-263 packages.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP38859	DDPAK/TO-263 (5)	10.16 mm × 8.42 mm
	TO-220 (5)	14.986 mm × 10.16 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (April 2013) to Revision F — **Page**

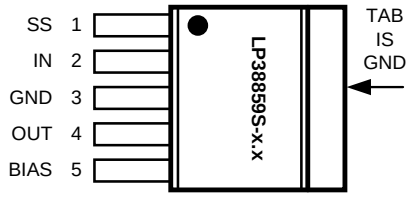
- Added *Device Information*, *Pin Configuration and Functions* and *ESD Ratings* sections, update *Thermal Values*, add *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections ... 1

Changes from Revision D (April 2013) to Revision E — **Page**

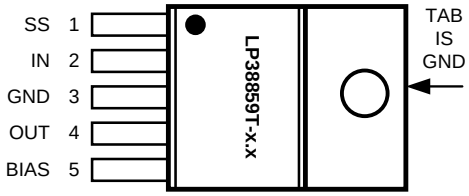
- Changed layout of National data sheet to TI format ... 1

5 Pin Configuration and Functions

KTT Package
5-Pin DDPAK/TO-263
Top View



NDH Package
5-Pin TO-220
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NUMBER		
BIAS	5	I	The supply for the internal control and reference circuitry.
GND	3	—	Ground
IN	2	I	The unregulated voltage input pin.
OUT	4	O	The regulated output voltage pin.
SS	1	I	Soft-start capacitor connection. Used to slow the rise time of V_{OUT} at turnon.
TAB	TAB	—	The TAB is a thermal connection that is physically attached to the backside of the die, and used as a thermal heat-sink connection. See the *Application and Implementation* section for details.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1][2]

	MIN	MAX	UNIT
V_{IN} supply voltage (survival)	−0.3	6	V
V_{BIAS} supply voltage (survival)	−0.3	6	V
V_{SS} soft-start voltage (survival)	−0.3	6	V
V_{OUT} voltage (survival)	−0.3	6	V
I_{OUT} current (survival)	Internally limited		
Power dissipation[3]	Internally limited		
Junction temperature	40	150	°C
Storage temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, contact the TI Sales Office/ Distributors for availability and specifications.
(3) Device power dissipation must be de-rated based on device power dissipation (P_D), ambient temperature (T_A), and package junction to ambient thermal resistance ($R_{\theta JA}$). Additional heat-sinking may be required to ensure that the device junction temperature (T_J) does not exceed the maximum operating rating. See the *Application and Implementation* section for details.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
V_{IN} supply voltage	(V_{OUT} + V_{DO})		V_{BIAS}	V
V_{BIAS} supply voltage	3		5.5	V
I_{OUT}	0		3	A
Junction temperature[1]	−40		125	°C

(1) Device power dissipation must be de-rated based on device power dissipation (P_D), ambient temperature (T_A), and package junction to ambient thermal resistance ($R_{\theta JA}$). Additional heat-sinking may be required to ensure that the device junction temperature (T_J) does not exceed the maximum operating rating. See the *Application and Implementation* section for details.

6.4 Thermal Information

THERMAL METRIC[1]		LP38859		UNIT
		KTT (DDPAK/TO-263 5 PINS	NDH (TO-220) 5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	43.2	70.7[2]	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.5	43.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.1	n/a[2]	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.6	23.6[2]	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.0	52.2[2]	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.1	1.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The NDH (TO-220) package is vertically mounted in center of JEDEC High-K test board (JESD 51-7) with no additional heat sink. This is a *through-hole* package; this is NOT a surface mount package.

6.5 Electrical Characteristics

Unless otherwise specified: $V_{IN} = V_{OUT(NOM)} + 1$ V, $V_{BIAS} = 3$ V, $I_{OUT} = 10$ mA, $C_{IN} = C_{OUT} = 10$ µF, $C_{BIAS} = 1$ µF, C_{SS} = open. Typical limits apply for $T_J = 25°C$; minimum and maximum limits apply over the junction temperature (T_J) range of -40°C to +125°C, unless otherwise specified. Minimum and maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at $T_J = 25°C$, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT}	V_{OUT} accuracy	$V_{OUT(NOM)} + 1$ V ≤ V_{IN} ≤ V_{BIAS} 3 V ≤ V_{BIAS} ≤ 5.5 V 10 mA ≤ I_{OUT} ≤ 3 A, $T_J = 25°C$	-1%		1%	
		$V_{OUT(NOM)} + 1$ V ≤ V_{IN} ≤ V_{BIAS} 3 V ≤ V_{BIAS} ≤ 5.5 V 10 mA ≤ I_{OUT} ≤ 3 A	–3%		3%	
		$V_{OUT(NOM)} + 1$ V ≤ V_{IN} ≤ V_{BIAS} 3 V ≤ V_{BIAS} ≤ 5.5 V 10 mA ≤ I_{OUT} ≤ 3 A 0°C ≤ T_J ≤ +125°C	–2%		2%	
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation, V_{IN} (1)	$V_{OUT(NOM)} + 1$ V ≤ V_{IN} ≤ V_{BIAS}		0.04		%/V
$\Delta V_{OUT}/\Delta V_{BIAS}$	Line regulation, V_{BIAS} (1)	3 V ≤ V_{BIAS} ≤ 5.5 V		0.10		%/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Output voltage load regulation (2)	10 mA ≤ I_{OUT} ≤ 3 A		0.2		%/A
V_{DO}	Dropout voltage (3)	I_{OUT} = 3 A, $T_J = 25°C$		240	300	mV
		I_{OUT} = 3 A			450	
$I_{GND(IN)}$	Quiescent current drawn from V_{IN} supply	LP38859-0.8 10 mA ≤ I_{OUT} ≤ 3 A, $T_J = 25°C$		7	8.5	mA
		LP38859-0.8 10 mA ≤ I_{OUT} ≤ 3 A			9	
		LP38859-1.2 10 mA ≤ I_{OUT} ≤ 3 A, $T_J = 25°C$		11	12	
		LP38859-1.2 10 mA ≤ I_{OUT} ≤ 3 A			15	
$I_{GND(BIAS)}$	Quiescent current drawn from V_{BIAS} supply	10 mA ≤ I_{OUT} ≤ 3 A, $T_J = 25°C$		3	3.8	mA
		10 mA ≤ I_{OUT} ≤ 3 A			4.5	
UVLO	Undervoltage lockout threshold	V_{BIAS} rising until device is functional $T_J = 25°C$	2.2	2.45	2.7	V
		V_{BIAS} rising until device is functional	2		2.9	
$UVLO_{(HYS)}$	Undervoltage lockout hysteresis	V_{BIAS} falling from UVLO threshold until device is non-functional $T_J = 25°C$	60	150	300	mV
		V_{BIAS} falling from UVLO threshold until device is non-functional	50		350	
I_{SC}	Output short-circuit current	$V_{IN} = V_{OUT(NOM)} + 1$ V		6.2		A
		V_{BIAS} = 3 V, V_{OUT} = 0 V				
SOFT-START						
r_{SS}	Soft-start internal resistance	LP38859-0.8	11	13.5	16	kΩ
		LP38859-1.2	13.5	16	18.5	
t_{SS}	Soft-start time $t_{SS} = C_{SS} \times r_{SS} \times 5$	LP38859-0.8, C_{SS} = 10 nF		675		µs
		LP38859-1.2, C_{SS} = 10 nF		800		

(1) Output voltage line regulation is defined as the change in output voltage from nominal value resulting from a change in input voltage.
(2) Output voltage load regulation is defined as the change in output voltage from nominal value as the load current increases from no load to full load.
(3) Dropout voltage is defined the as input to output voltage differential ($V_{IN} – V_{OUT}$) where the input voltage is low enough to cause the output voltage to drop no more than 2% from the nominal value.

Electrical Characteristics (continued)

Unless otherwise specified: $V_{IN} = V_{OUT(NOM)} + 1$ V, $V_{BIAS} = 3$ V, $I_{OUT} = 10$ mA, $C_{IN} = C_{OUT} = 10$ µF, $C_{BIAS} = 1$ µF, C_{SS} = open. Typical limits apply for $T_J = 25$°C; minimum and maximum limits apply over the junction temperature (T_J) range of -40°C to +125°C, unless otherwise specified. Minimum and maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at $T_J = 25$°C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PARAMETERS						
PSRR (V_{IN})	Ripple rejection for V_{IN} input voltage	$V_{IN} = V_{OUT(NOM)} + 1$ V $f = 120$ Hz		80		dB
		$V_{IN} = V_{OUT(NOM)} + 1$ V $f = 1$ kHz		65		
PSRR (V_{BIAS})	Ripple rejection for V_{BIAS} voltage	$V_{BIAS} = V_{OUT(NOM)} + 3$ V f = 120 Hz		58		
		$V_{BIAS} = V_{OUT(NOM)} + 3$ V $f = 1$ kHz		58		
e_n	Output noise density	$f = 120$ Hz		1		µV/√Hz
	Output noise voltage	BW = 10 Hz − 100 kHz, $V_{OUT} = 1.8$ V		150		μV_{RMS}
		BW = 300 Hz − 300 kHz, $V_{OUT} = 1.8$ V		90		
THERMAL PARAMETERS						
T_{SD}	Thermal shutdown junction temperature			160		°C
$T_{SD(HYS)}$	Thermal shutdown hysteresis			10		°C

6.6 Typical Characteristics

Unless otherwise specified: T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1 V, V_{BIAS} = 3 V, I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 10-µF ceramic, C_{BIAS} = 1-µF ceramic, C_{SS} = open.

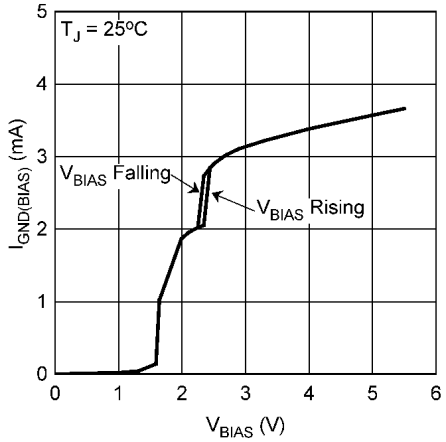


Figure 1. V_{BIAS} Ground Pin Current ($I_{GND(BIAS)}$) vs V_{BIAS}

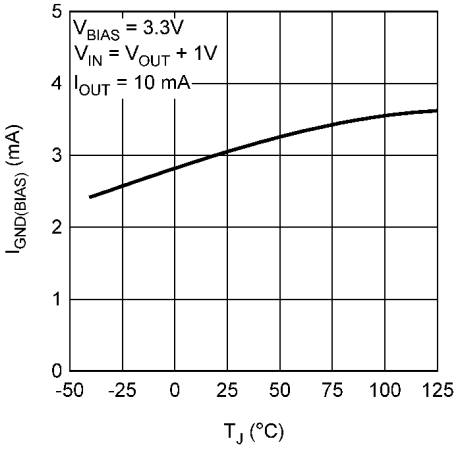


Figure 2. V_{BIAS} Ground Pin Current ($I_{GND(BIAS)}$) vs Temperature

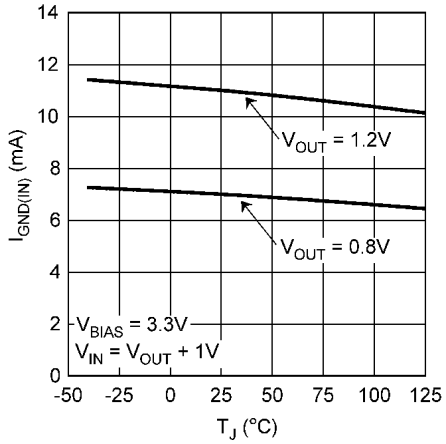


Figure 3. V_{IN} Ground Pin Current vs Temperature

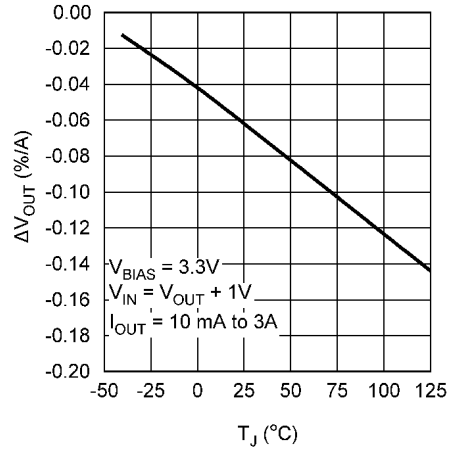


Figure 4. Load Regulation vs Temperature

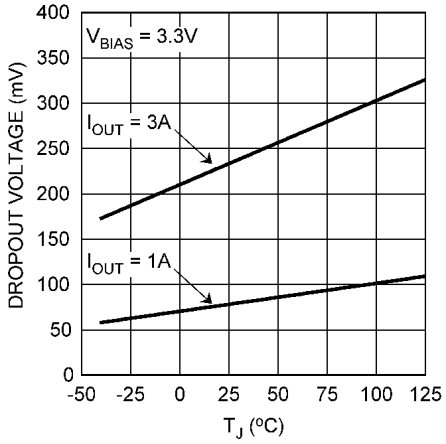


Figure 5. Dropout Voltage (V_{DO}) vs Temperature

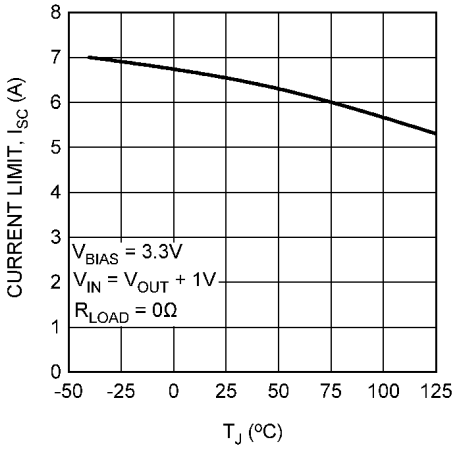


Figure 6. Output Current Limit (I_{SC}) vs Temperature

Typical Characteristics (continued)

Unless otherwise specified: T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1 V, V_{BIAS} = 3 V, I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 10-µF ceramic, C_{BIAS} = 1-µF ceramic, C_{SS} = open.

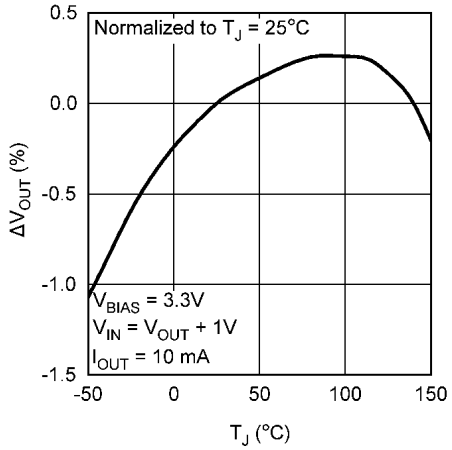


Figure 7. V_{OUT} vs Temperature

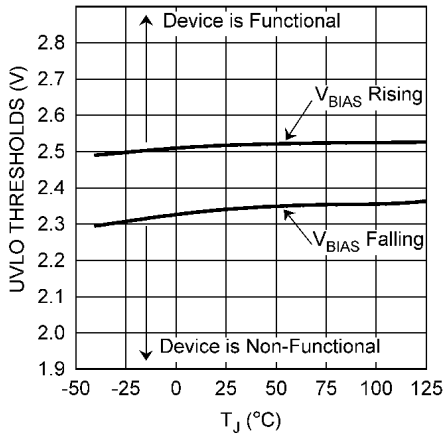


Figure 8. UVLO Thresholds vs Temperature

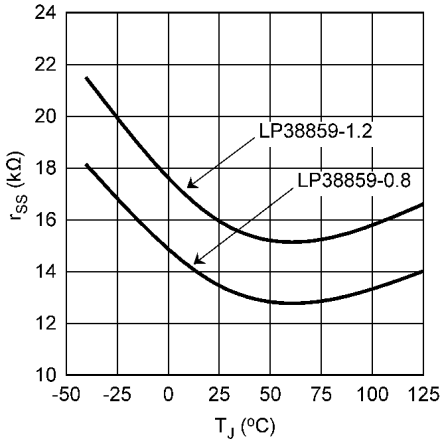


Figure 9. Soft-Start Resistor (R_{SS}) vs Temperature

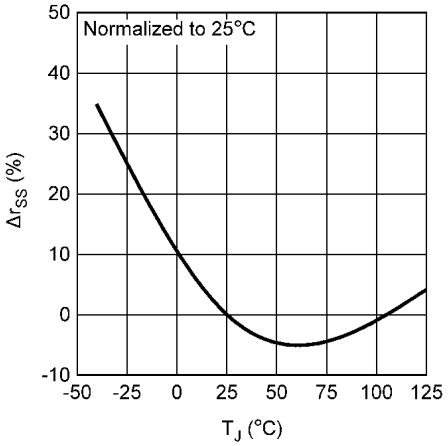


Figure 10. Soft-Start R_{SS} Variation vs Temperature

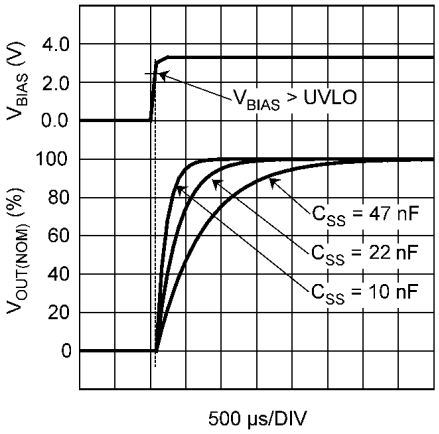


Figure 11. V_{OUT} vs C_{SS}

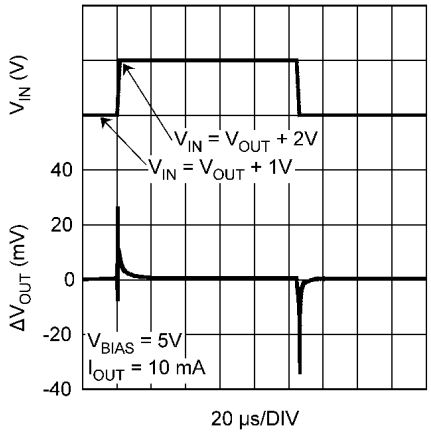


Figure 12. V_{IN} Line Transient Response

Typical Characteristics (continued)

Unless otherwise specified: T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1 V, V_{BIAS} = 3 V, I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 10-µF ceramic, C_{BIAS} = 1-µF ceramic, C_{SS} = open.

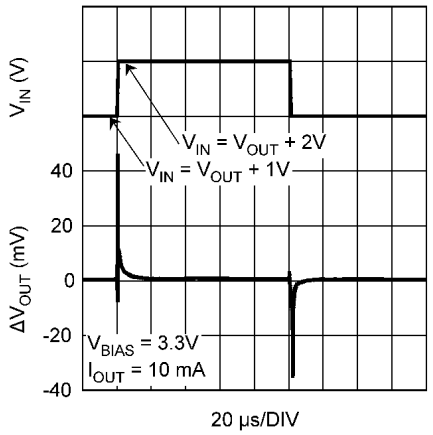


Figure 13. V_{IN} Line Transient Response

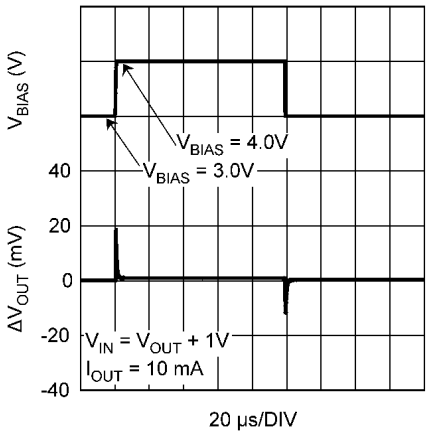


Figure 14. V_{BIAS} Line Transient Response

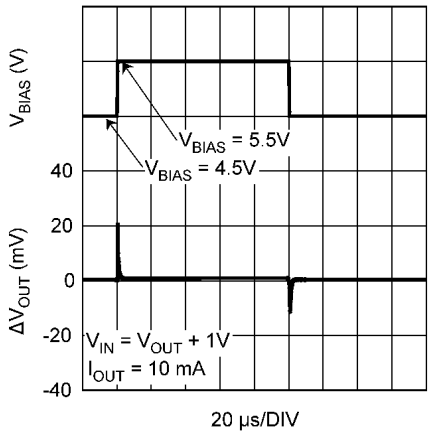


Figure 15. V_{BIAS} Line Transient Response

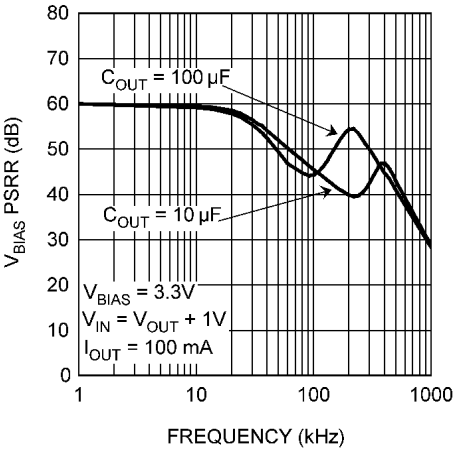


Figure 16. V_{BIAS} PSRR

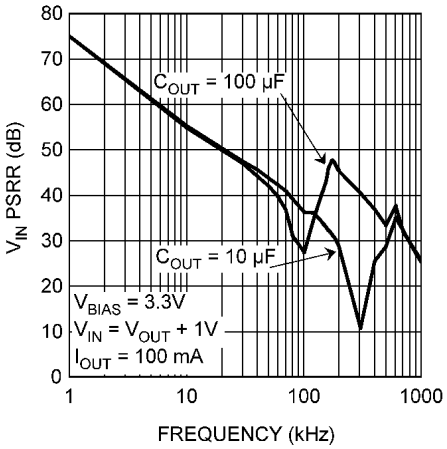


Figure 17. V_{IN} PSRR

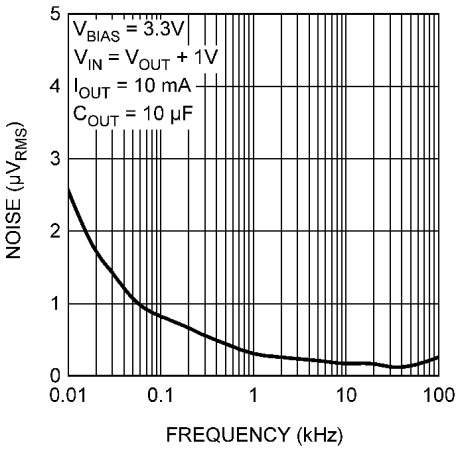


Figure 18. Output Noise

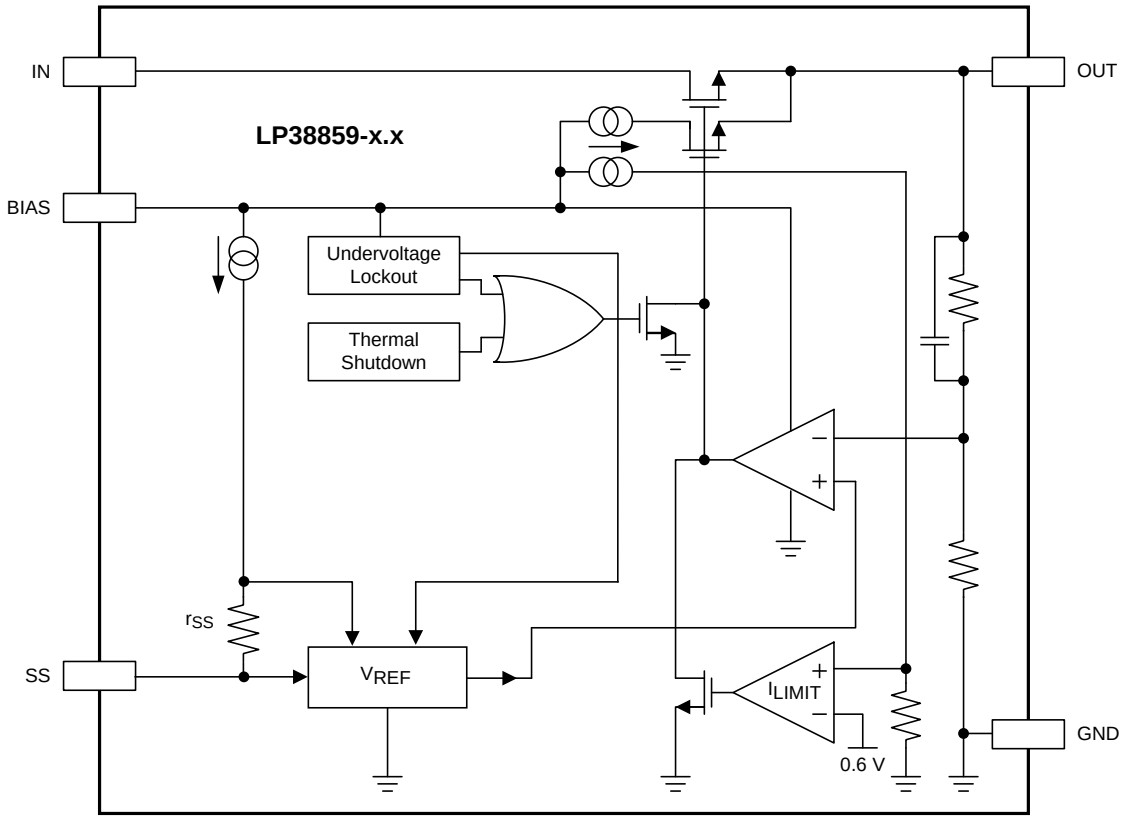
7 Detailed Description

7.1 Overview

The LP38559 is a fast-response, high-current, low-dropout regulator, available in output voltages are 0.8 V and 1.2 V. This part is capable of delivering 3-A continuous load current. Standard regulator features, such as overcurrent and over temperature protection, are also included. The LP38559 contains several features:

- Low dropout voltage, typical 240 mV at 3-A load.
- The bias voltage(V_{BIAS}) provides voltage to drive the gate of the N-MOS power transistor.
- The input voltage(V_{IN}) is the input voltage which supplies power to the load.
- Programmable soft-start time.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Voltage

The input voltage (V_{IN}) is the high current external voltage rail that is regulated down to a lower voltage, which is applied to the load. The input voltage must be at least V_{OUT} + V_{DO}, and no higher than whatever values is used for V_{BIAS}.

7.3.2 Bias Voltage

The bias voltage (V_{BIAS}) is a low current external voltage rail required to bias the control circuitry and provide gate drive for the N-FET pass transistor. The bias voltage must be in the range of 3 V to 5.5 V to ensure proper operation of the device.

Feature Description (continued)

7.3.3 Undervoltage Lockout

The bias voltage is monitored by a circuit which prevents the device from functioning when the bias voltage is below the undervoltage lockout (UVLO) threshold of approximately 2.45 V.

As the bias voltage rises above the UVLO threshold the device control circuitry becomes active. There is approximately 150 mV of hysteresis built into the UVLO threshold to provide noise immunity.

When the bias voltage is between the UVLO threshold and the minimum operating rating value of 3 V, the device is functional, but the operating parameters are not within the specified limits.

7.3.4 Supply Sequencing

There is no requirement for the order that V_{IN} or V_{BIAS} are applied or removed.

One practical limitation is that the soft-start circuit starts charging C_{SS} when V_{BIAS} rises above the UVLO threshold. If the application of V_{IN} is delayed beyond this point the benefits of soft start are compromised.

In any case, the output voltage cannot be specified until both V_{IN} and V_{BIAS} are within the range of specified operating values.

If used in a dual-supply system where the regulator output load is returned to a negative supply, the output pin must be diode clamped to ground. A Schottky diode is recommended for this diode clamp.

7.3.5 Reverse Voltage

A reverse voltage condition exists when the voltage at the output pin is higher than the voltage at the input pin. Typically this happens when V_{IN} is abruptly taken low and C_{OUT} continues to hold a sufficient charge such that the input to output voltage becomes reversed.

The NMOS pass element, by design, contains no body diode. This means that, as long as the gate of the pass element is not driven, there is no reverse current flow through the pass element during a reverse voltage event. The gate of the pass element is not driven when V_{BIAS} is below the UVLO threshold.

When V_{BIAS} is above the UVLO threshold, the control circuitry is active and attempts to regulate the output voltage. Because the input voltage is less than the output voltage the control circuit drives the gate of the pass element to the full V_{BIAS} potential when the output voltage begins to fall. In this condition, reverse current flows from the OUT pin to the IN pin , limited only by the $R_{DS(ON)}$ of the pass element and the output to input voltage differential. This condition is outside the specified operating range and must be avoided.

7.3.6 Soft-Start

The LP38859 incorporates a soft-start function that reduces the start-up current surge into the output capacitor (C_{OUT}) by allowing V_{OUT} to rise slowly to the final value. This is accomplished by controlling V_{REF} at the SS pin. The soft-start timing capacitor (C_{SS}) is internally held to ground until V_{BIAS} rises above the UVLO threshold.

V_{REF} rises at an RC rate defined by the internal resistance of the SS pin (r_{SS}), and the external capacitor connected to the SS pin. This allows the output voltage to rise in a controlled manner until steady-state regulation is achieved. Typically, five time constants are recommended to assure that the output voltage is sufficiently close to the final steady-state value. During the soft-start time the output current can rise to the built-in current limit.

$$\text{Soft-Start Time} = C_{SS} \times r_{SS} \times 5 \quad (1)$$

Because the V_{OUT} rise is exponential, not linear, the in-rush current peaks during the first time constant (τ), and V_{OUT} requires four additional time constants (4τ) to reach the final value (5τ) .

After achieving normal operation, if V_{BIAS} falsl below the ULVO threshold, the device output is disabled, and the soft-start capacitor (C_{SS}) discharge circuit becomes active. The C_{SS} discharge circuit remains active until V_{BIAS} falls to 500 mV (typical). When V_{BIAS} falls below 500 mV (typical), the C_{SS} discharge circuit ceases to function due to a lack of sufficient biasing to the control circuitry.

Feature Description (continued)

Because V_{REF} appears on the SS pin, any leakage through C_{SS} causes V_{REF} to fall, and thus affect V_{OUT}. A leakage of 50 nA (about 10 MΩ) through C_{SS} causes V_{OUT} to be approximately 0.1% lower than nominal, while a leakage of 500 nA (about 1 MΩ) causes V_{OUT} to be approximately 1% lower than nominal. Typical ceramic capacitors have a factor of 10× difference in leakage between 25°C and 85°C, so the maximum ambient temperature must be included in the capacitor selection process.

Typical C_{SS} values are in the range of 1 nF to 100 nF, providing typical soft-start times in the range of 70 µs to 7 ms (5τ). Values less than 1 nF can be used, but the soft-start effect is minimal. Values larger than 100 nF provide soft start, but may not be fully discharged if V_{BIAS} falls from the UVLO threshold to less than 500 mV in less than 100 µs.

Figure 19 shows the relationship between the C_{OUT} value and a typical C_{SS} value.

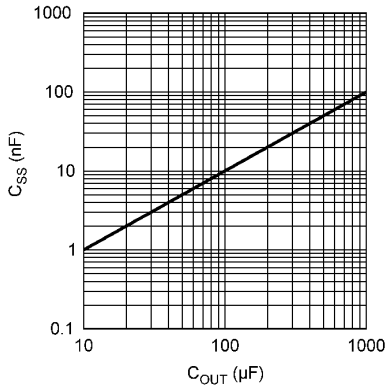


Figure 19. Typical C_{SS} vs C_{OUT} Values

The C_{SS} capacitor must be connected to a clean ground path back to the device ground pin. No components, other than C_{SS}, should be connected to the SS pin, as there could be adverse effects to V_{OUT}.

If the soft-start function is not needed, the SS pin must be left open, although some minimal capacitance value is always recommended.

7.4 Device Functional Modes

7.4.1 Operation with 3 V ≤ V_{BIAS} ≤ 5.5 V, $V_{OUT(TARGET)}$+ 0.3 V ≤ V_{IN} ≤ V_{BIAS}

The device operates if the bias voltage is equal to, or exceeds, 3 V, and input voltage is equal to, or exceeds, $V_{OUT(TARGET)}$ + 0.3 V. At bias voltages below the minimum V_{BIAS} requirement, the device does not operate correctly, and output voltage may not reach target value.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LP38859 can provide 3-A output current with 240-mV dropout voltage (typical). The bias voltage must be in the range of 3 V to 5.5 V to ensure proper operation of the device. The input voltage must be at least V_{OUT} + V_{DO}, and no higher than whatever value is used for V_{BIAS}. Minimal input and output capacitors are each 10 µF. The capacitor on the BIAS pin must be at least 1 µF.

8.2 Typical Application

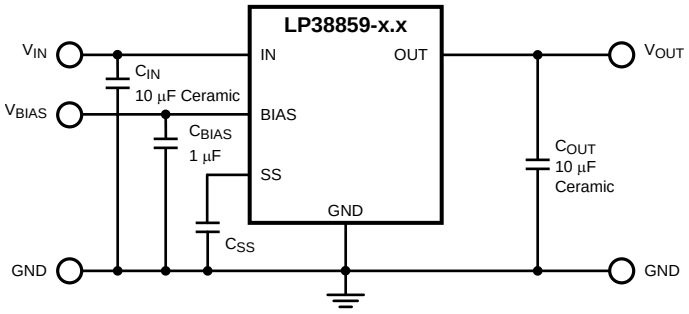


Figure 20. LP38859 Typical Application

8.2.1 Design Requirements

For typical high-accuracy LDO linear regulator applications, use the parameters listed in Table 1.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Bias voltage	3 V to 5.5 V
Input voltage	1.1 V to 5.5 V
Output voltages	0.8 V, 1.2 V
Output current	3 A (maximum)
Bias capacitor	1 µF (minimum)
Input capacitor	10 µF (minimum)
Output capacitor	10 uF (minimum)

8.2.2 Detailed Design Procedure

8.2.2.1 External Capacitors

To assure regulator stability, input and output capacitors are required as shown in the Figure 20.

8.2.2.1.1 Output Capacitor

A minimum output capacitance of 10 µF, ceramic, is required for stability. The amount of output capacitance can be increased without limit. The output capacitor must be located less than 1 cm from the OUT pin of the device and returned to the device GND pin with a clean analog ground.

Only high quality ceramic types such as X5R or X7R must be used, as the Z5U and Y5F types do not provide sufficient capacitance over temperature.

Tantalum capacitors also provide stable operation across the entire operating temperature range. However, the effects of ESR may provide variations in the output voltage during fast load transients. Using the minimum recommended 10-µF ceramic capacitor at the output allows unlimited capacitance, tantalum, and/or aluminum, to be added in parallel.

8.2.2.1.2 Input Capacitor

The input capacitor must be at least 10 µF, but can be increased without limit. Its purpose is to provide a low source impedance for the regulator input. A ceramic capacitor, X5R or X7R, is recommended.

Tantalum capacitors may also be used at the IN pin. There is no specific ESR limitation on the input capacitor (the lower, the better).

Aluminum electrolytic capacitors can be used, but are not recommended as their ESR increases very quickly at cold temperatures. They are not recommended for any application where the ambient temperature falls below 0°C.

8.2.2.1.3 Bias Capacitor

The capacitor on the BIAS pin must be at least 1 µF and can be any good-quality capacitor (ceramic is recommended).

8.2.2.2 Power Dissipation and Heat-Sinking

Additional copper area for heat-sinking may be required depending on the maximum device dissipation (P_D) and the maximum anticipated ambient temperature (T_A) for the device. Under all possible conditions, the junction temperature must be within the range specified under operating conditions.

The total power dissipation of the device is the sum of three different points of dissipation in the device.

The first part is the power that is dissipated in the NMOS pass element, and can be determined with the formula:

$$P_{D(PASS)} = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (2)$$

The second part is the power that is dissipated in the bias and control circuitry, and can be determined with the formula:

$$P_{D(BIAS)} = V_{BIAS} \times I_{GND(BIAS)}$$

where

- $I_{GND(BIAS)}$ is the portion of the operating ground current of the device that is related to V_{BIAS}. (3)

The third part is the power that is dissipated in portions of the output stage circuitry, and can be determined with the formula:

$$P_{D(IN)} = V_{IN} \times I_{GND(IN)}$$

where

- $I_{GND(IN)}$ is the portion of the operating ground current of the device that is related to V_{IN}. (4)

The total power dissipation is then:

$$P_D = P_{D(PASS)} + P_{D(BIAS)} + P_{D(IN)} \quad (5)$$

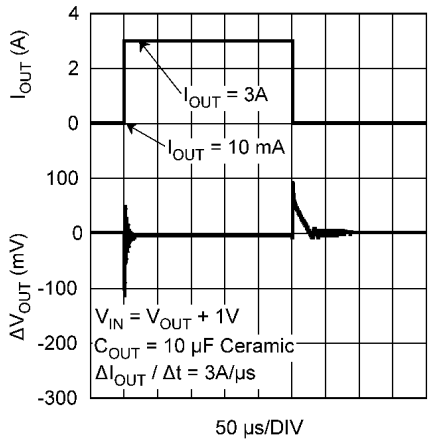
The maximum allowable junction temperature rise (ΔT_J) depends on the maximum anticipated ambient temperature (T_A) for the application, and the maximum allowable operating junction temperature ($T_{J(MAX)}$) .

$$\Delta T_J = T_{J(MAX)} – T_{A(MAX)} \quad (6)$$

The maximum allowable value for junction-to-ambient thermal resistance, $R_{\theta JA}$, can be calculated using Equation 7.

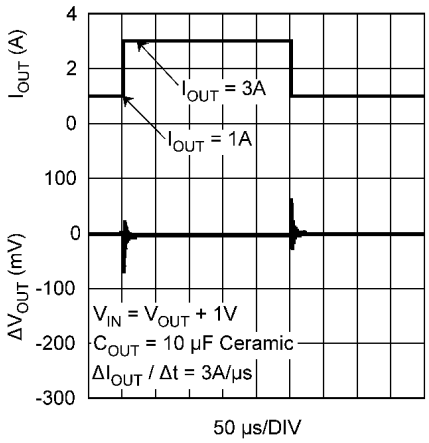
$$R_{\theta JA} \leq \Delta T_J / P_D \quad (7)$$

8.2.3 Application Curves



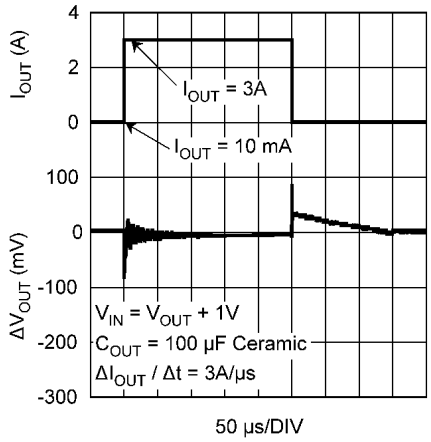
C_{OUT} = 10-µF ceramic

Figure 21. Load Transient Response



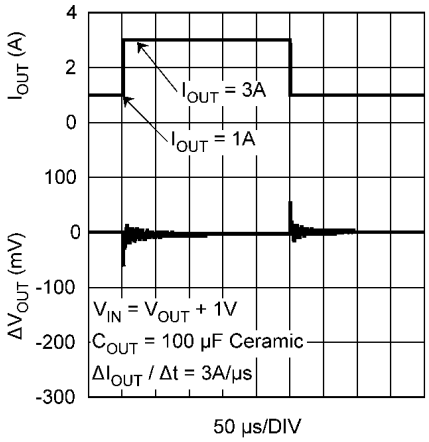
C_{OUT} = 10-µF ceramic

Figure 22. Load Transient Response



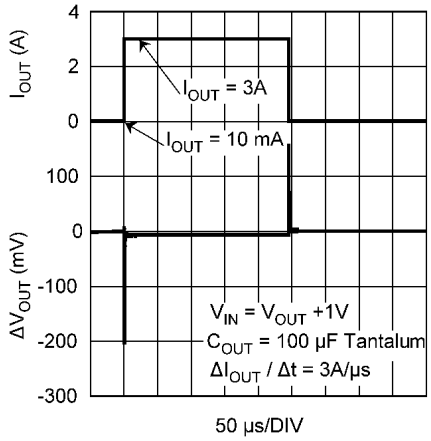
C_{OUT} = 100-µF ceramic

Figure 23. Load Transient Response



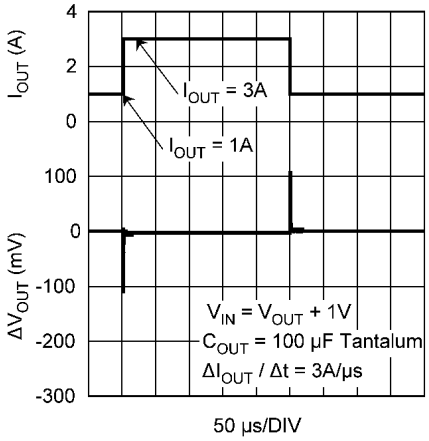
C_{OUT} = 100-µF ceramic

Figure 24. Load Transient Response



C_{OUT} = 100-µF tantalum

Figure 25. Load Transient Response



C_{OUT} = 100-µF tantalum

Figure 26. Load Transient Response

9 Power Supply Recommendations

The LP38859 device is designed to operate from an input voltage supply range from 3 V and 5.5 V. The input voltage range provides adequate headroom in order for the device to have a regulated output. This input supply must be well regulated. An input capacitor of at least 10 µF is required.

10 Layout

10.1 Layout Guidelines

The dynamic performance of the LP38859 is dependent on the layout of the PCB. PCB layout practices that are adequate for typical LDOs may degrade the PSRR, noise, or transient performance of the LP38859. Best performance is achieved by placing C_{IN} and C_{OUT} on the same side of the PCB as the LP38859, and as close as is practical to the package. The ground connections for C_{IN} and C_{OUT} must be back to the LP38859 ground pin using as wide and short of a copper trace as is practical.

Good PC layout practices must be used or instability can be induced because of ground loops and voltage drops. The input and output capacitors must be directly connected to the IN, OUT, and GND pins of the LP38859 using traces which do not have other currents flowing in them (Kelvin connect).

The best way to do this is to lay out C_{IN} and C_{OUT} near the device with short traces to the IN, OUT, and GND pins. The regulator ground pin must be connected to the external circuit ground so that the regulator and its capacitors have a single-point ground.

Stability problems have been seen in applications where vias to an internal ground plane were used at the ground points of the LP38859 device and the input and output capacitors. This was caused by varying ground potentials at these nodes resulting from current flowing through the ground plane. Using a single point ground technique for the regulator and its capacitors fixed the problem.

Because high current flows through the traces going into the IN pin and coming from the OUT pin, Kelvin connect the capacitor leads to these pins so there is no voltage drop in series with the input and output capacitors.

10.2 Layout Example

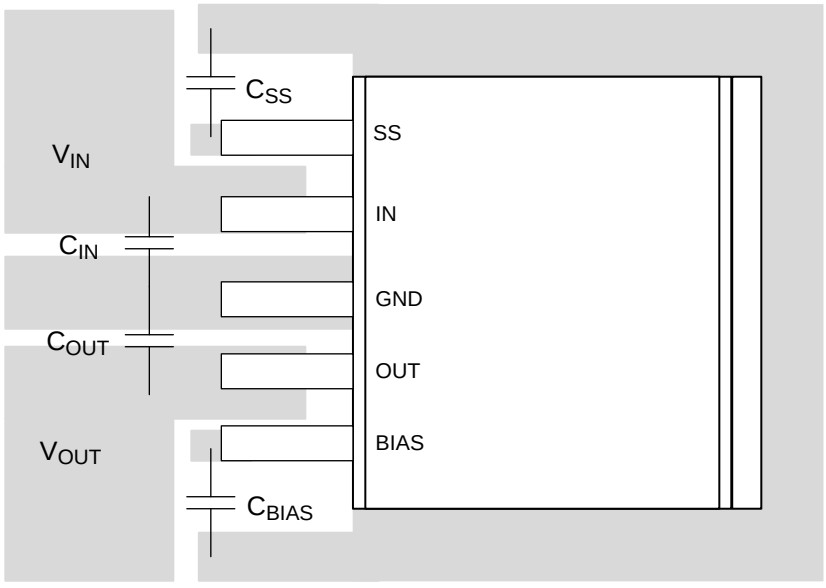


Figure 27. LP38859 Layout Example

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
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11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP38859S-1.2/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	-40 to 125	LP38859S -1.2	Samples
LP38859SX-1.2/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	-40 to 125	LP38859S -1.2	Samples
LP38859T-0.8/NOPB	ACTIVE	TO-220	NDH	5	45	RoHS & Green	SN	Level-1-NA-UNLIM	-40 to 125	LP38859T -0.8	Samples
LP38859T-1.2/NOPB	ACTIVE	TO-220	NDH	5	45	RoHS & Green	SN	Level-1-NA-UNLIM	-40 to 125	LP38859T -1.2	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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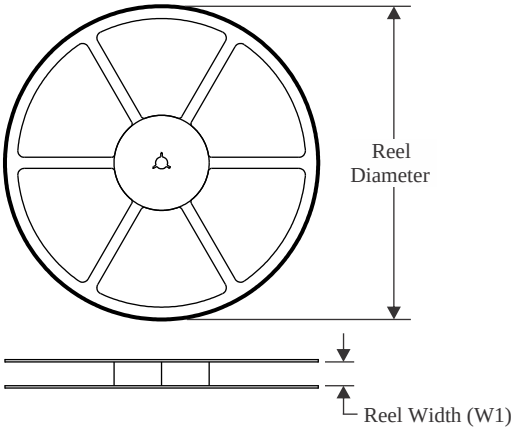
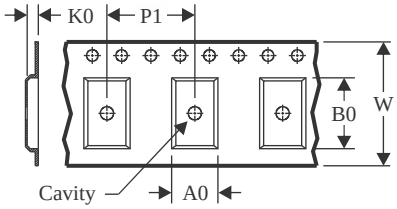
TAPE AND REEL INFORMATION

REEL DIMENSIONS

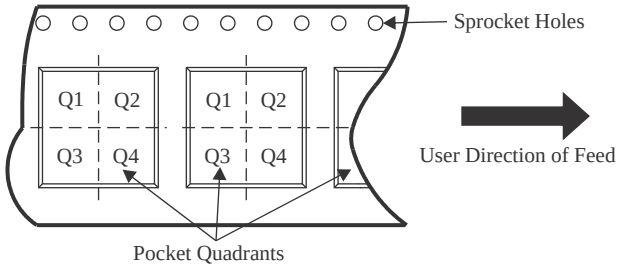


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

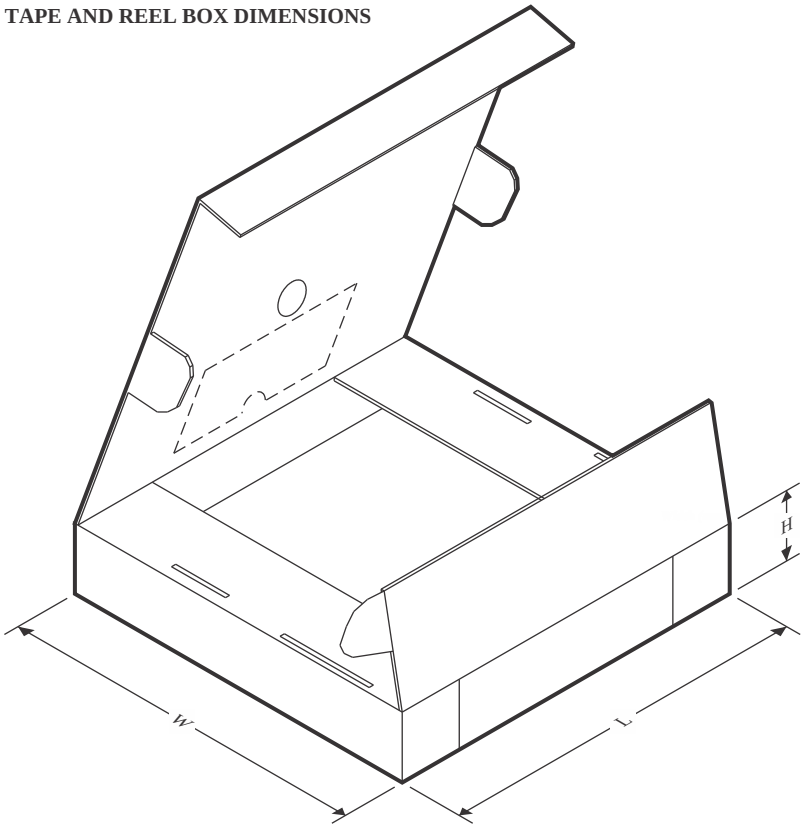
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP38859SX-1.2/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2

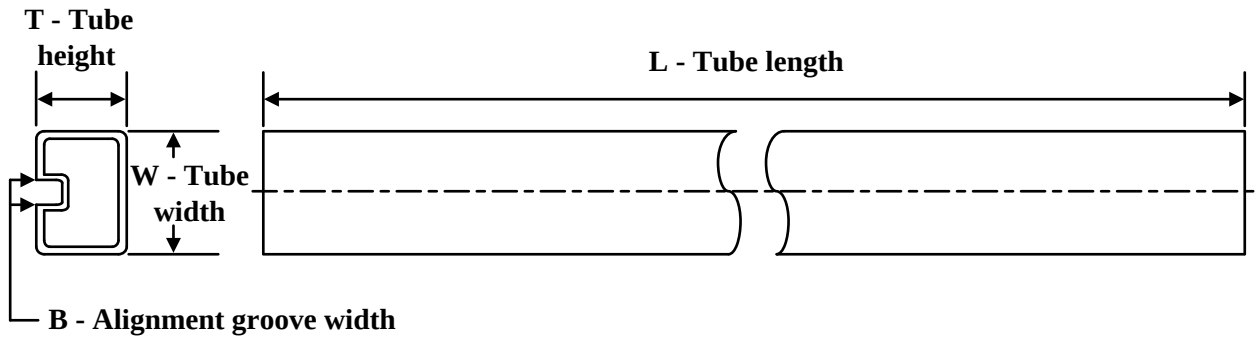
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP38859SX-1.2/NOPB	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0

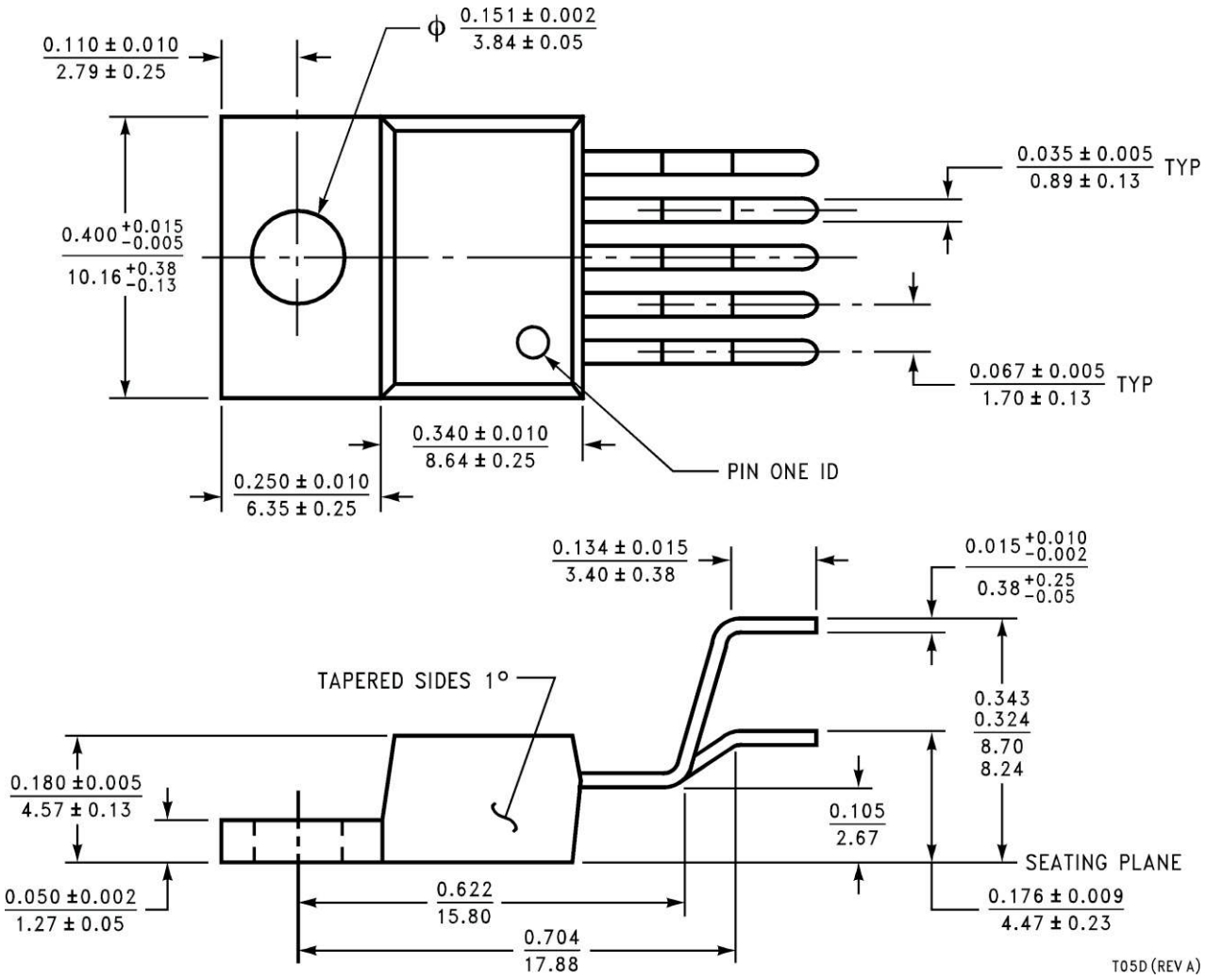
TUBE



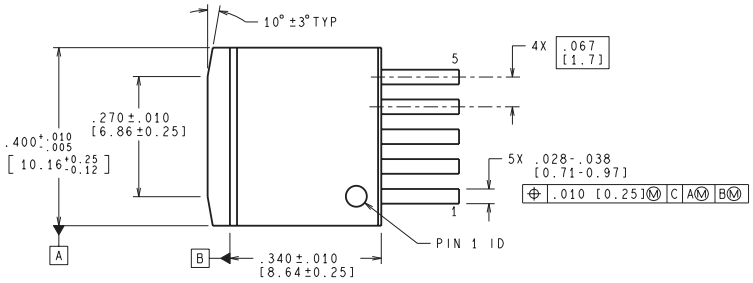
*All dimensions are nominal

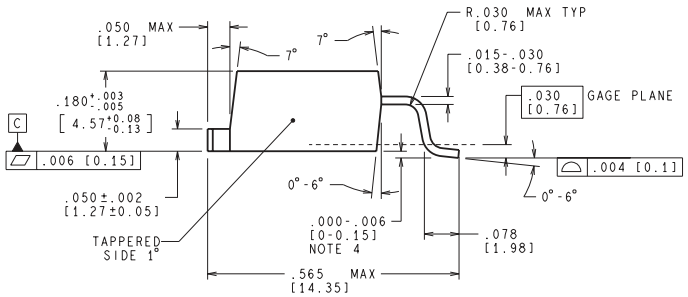
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LP38859S-1.2/NOPB	KTT	TO-263	5	45	502	25	8204.2	9.19
LP38859T-0.8/NOPB	NDH	TO-220	5	45	502	30	30048.2	10.74
LP38859T-1.2/NOPB	NDH	TO-220	5	45	502	30	30048.2	10.74

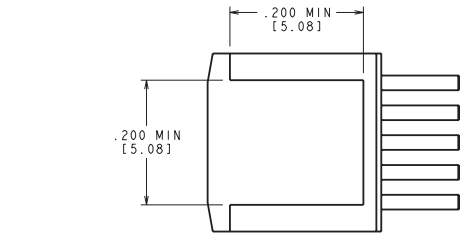
NDH0005D


0.110 ± 0.010
2.79 ± 0.25
ϕ 0.151 ± 0.002
3.84 ± 0.05
0.035 ± 0.005
0.89 ± 0.13 TYP
0.400 +0.015 −0.005
10.16 +0.38 −0.13
0.067 ± 0.005
1.70 ± 0.13 TYP
0.340 ± 0.010
8.64 ± 0.25
PIN ONE ID
0.250 ± 0.010
6.35 ± 0.25
0.134 ± 0.015
3.40 ± 0.38
0.015 +0.010 −0.002
0.38 +0.25 −0.05
TAPERED SIDES 1°
0.343
0.324
8.70
8.24
0.180 ±0.005
4.57 ± 0.13
0.105
2.67
SEATING PLANE
0.050 ±0.002
1.27 ± 0.05
0.622
15.80
0.176 ± 0.009
4.47 ± 0.23
0.704
17.88
T05D (REV A)

KTT0005B







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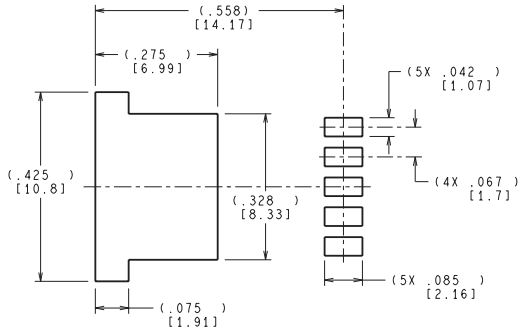

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