

CLOCKED FLIP-FLOP

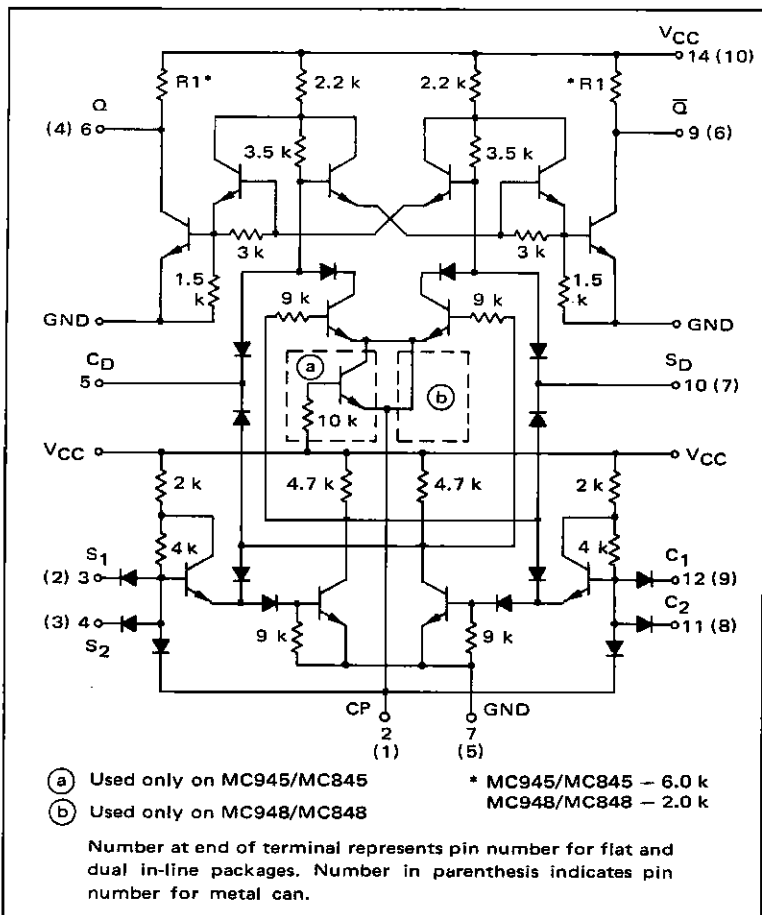
MDTL MC930/830 series **MOTOROLA**



ISSUE A

MC945 • MC845
MC948 • MC848

Add Suffix F for ceramic flat package (Case 607).
Suffix G for TO-100 metal package (Case 603-02).
Suffix L for ceramic dual in-line package (Case 632).
Suffix P for plastic dual in-line package (Case 646) MC830 series only.



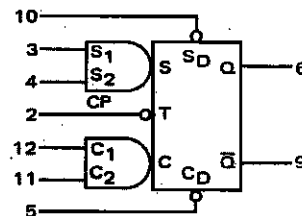
These clocked flip-flops consist of two directly coupled flip-flops, operating on the "master-slave" principle. The input information is stored in the "master" flip-flop when the clock voltage is high, and is transferred to the "slave" when the clock voltage is low.

This clocked flip-flop can be operated in either the R-S or J-K mode. For J-K operation the Q output is connected to a clear input, and the \bar{Q} output is connected to a set input. Asynchronous inputs, direct set (S_D) and direct clear (C_D), override the synchronous inputs. No matter what other inputs are applied to the flip-flop, the direct set and clear inputs prevail.

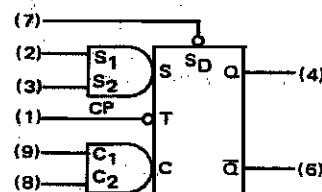
The outputs are buffered, thereby reducing the possibility of circuit disturbance from external line noise.

The output pullup resistor of the MC948/MC848 has been changed from that utilized in the MC945/MC845 in order to improve the propagation delay-versus-capacitance characteristics.

MC945F,L/MC845F,L,P
MC948F,L/MC848F,L,P



MC945G/MC845G
MC948G/MC848G



SYNCHRONOUS TRUTH TABLE

		t_n		t_{n+1}
S_1	S_2	C_1	C_2	Q
0	X	0	X	Q_n
0	X	X	0	Q_n
X	0	0	X	Q_n
X	0	X	0	Q_n
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	U

0 - Low State (more negative)
1 - High State (more positive)
X - State of the input does not affect the state of the circuit.
U - Indeterminate State

J-K TRUTH TABLE
(Connect S_2 to \bar{Q} , C_2 to Q)

		t_n	t_{n+1}
S_1	C_1	Q	
0	0	Q_n	
1	0	1	
0	1	0	
1	1	\bar{Q}_n	

ASYNCHRONOUS TRUTH TABLE

S_D	C_D	Q	\bar{Q}
1	1	NC	NC
0	1	1	0
1	0	0	1
0	0	1	1

Asynchronous inputs, direct set (S_D) and direct clear (C_D), override the synchronous inputs; they are independent of all other inputs.

Input Loading Factor:
S and C = 2/3
 $S_D, C_D, T = 2$

Output Loading Factor:
MC945 = 10
MC845 = 12
MC948 = 9
MC848 = 11

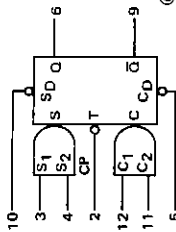
Total Power Dissipation:
MC945/MC845 = 60 mW typ/pkg
MC948/MC848 = 70 mW typ/pkg
Propagation Delay Time = 40 ns typ

See General Information section for packaging.

MC945 • MC845
MC948 • MC848

ELECTRICAL CHARACTERISTICS

NOTE: Although the test conditions and test limits are the same for devices in ALL available packages, the table shows pin connections for testing only the flat and dual in-line packaged devices. To test devices in the metal can, substitute pin numbers shown in the conversion table below.



PACKAGE	PIN NUMBERS												
	2	3	4	5	6	7	8	9	10	11	12	14	
Flat/Dual In-Line	-	2	3	4	5	6	7	8	9	10	11	12	-
Metal Can	-	1	2	3	4	5	6	7	8	9	10	-	-

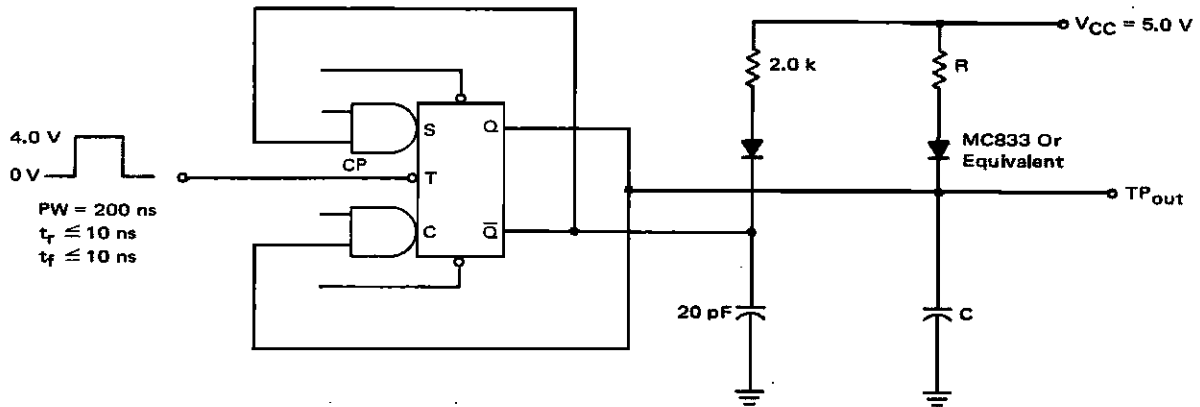
TEST VOLTAGE/CURRENT VALUES											
mA		Volts									
I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCI}	V_{CCH}	V_{max}	CP_a	CP_b
MC945	MC948	MC945	MC948	MC945	MC948	MC945	MC948	MC945	MC948	MC945	MC948
14.6	13.0	-0.12	-0.5	1.40	2.10	0	4.00	-	4.50	5.50	-
15.2	13.6	-0.12	-0.5	1.10	2.00	0	4.00	5.00	4.50	5.50	8.00
13.8	12.3	-0.12	-0.5	0.80	2.00	0	4.00	-	4.50	5.50	-
MC845	MC848	MC845	MC848	MC845	MC848	MC845	MC848	MC845	MC848	MC845	MC848
16.6	15.4	-0.12	-0.5	1.20	2.00	0.45	4.00	-	5.00	5.00	-
16.8	15.4	-0.12	-0.5	1.10	1.90	0.45	4.00	5.00	5.00	5.00	8.00
16.0	14.6	-0.12	-0.5	0.95	1.80	0.50	4.00	-	5.00	5.00	-

TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:

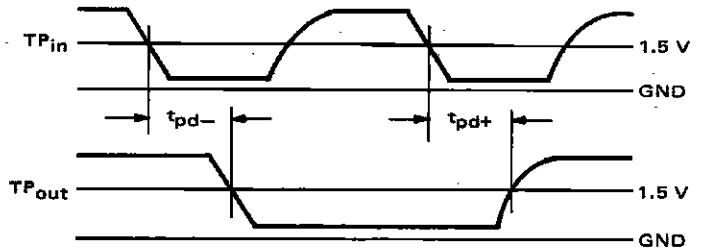
Characteristic	Symbol	Pin Under Test	MC945, MC948 TEST LIMITS						MC845, MC848 TEST LIMITS						Unit	Pulse In	Pulse Out	Pins
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max						
Output Voltage	V_{OL}	6	0.40	0.40	0.45	0.45	0.45	0.45	0.45	0.45	0.50	0.50	Vdc	6	9	14	3,7,7,12	
	V_{OH}	6	2.50	2.60	2.50	2.60	2.50	2.60	2.50	2.60	2.50	2.60	Vdc	6	9	7, 7, 3,4,7		
		9	-	-	-	-	-	-	-	-	-	-	Vdc	9	9	7, 7, 3,4,7		
Reverse Current	I_R	3	-	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	μ Adc	3	4	7,11,12		
		4	-	-	-	-	-	-	-	-	-	-	μ Adc	4	4	2,7		
		5	-	-	-	-	-	-	-	-	-	-	μ Adc	5	5	2,7		
Forward Current	I_{RCP}	2	-	20	20	20	20	20	20	20	20	20	mA	2	2	7,11,12		
	I_{FCP}	3	-1.07	-1.07	-1.07	-1.07	-1.07	-1.07	-1.07	-1.07	-1.07	-1.07	mA	3	4	7,11,12		
	I_{FS}	10	-	-	-	-	-	-	-	-	-	-	mA	10	10	7, 7, 3,4,7,11,12		
Power Drain Current	I_{PDH}	14	-	-	11	11	11	11	11	11	11	11	mAdc	14	14	7		
	I_{max}	14	-	-	14.5	14.5	14.5	14.5	14.5	14.5	14.5	14.5	mAdc	14	14	2,3,4,7,11,12		
	I_{max}	14	-	-	13.5	13.5	13.5	13.5	13.5	13.5	13.5	13.5	mAdc	14	14	7		
Switching Times	t_{pd+}	2,6	-	25	100	25	100	25	100	25	100	25	ns	2	6	7		
	t_{pd-}	2,6	-	15	55	15	55	15	55	15	55	15	ns	2	6	7		
	t_{pd-}	2,6	-	25	75	25	75	25	75	25	75	25	ns	2	6	7		

Pins not listed are left open.
 † CP_a = Clock Pulse a
 ‡ CP_b = Clock Pulse b
 See Clock Pulse Waveforms.

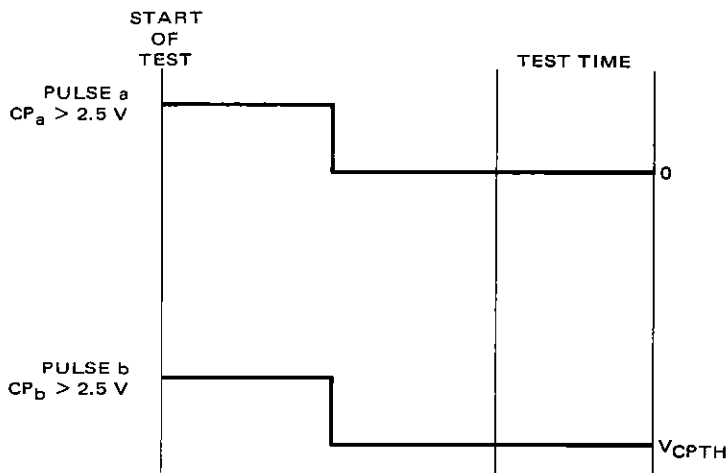
PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS



TEST	R	C
t_{pd+}	3.9 k ohms	30 pF
t_{pd-}	400 ohms	30 pF



CLOCK PULSE WAVEFORMS
($t_f < 1.0 \mu s$)



TEST CONDITIONS

	V _{CPTH}	
	MC945	MC948
-55°C	1.15 V	1.30 V
+25°C	0.95 V	1.15 V
+125°C	0.65 V	0.85 V
MC845 MC848		
0°C	1.00 V	1.20 V
+25°C	0.95 V	1.15 V
+75°C	0.65 V	0.85 V