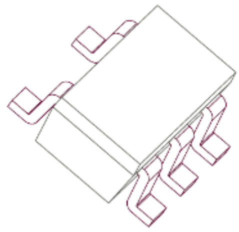
TOSHIBA CMOS Linear Integrated Circuit Silicon Monolithic

TC75S103F

Single Operational Amplifier
Low supply current

Features

- Input, Output Full Range type (Rail to Rail)
- Low supply current 100μA (Typ.) @V_{DD}=1.8V
- Low Input offset voltage 1.5mV (Max) @V_{DD}=1.8V
- Wide Operating Voltage Range 1.8V to 5.5V



Weight:
SMV (SOT-25)(SC-74A) :14 mg (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{DD} - V_{SS}	6	V
Differential input voltage	DV_{IN}	±6	V
Input voltage	V_{IN}	V_{DD} to V_{SS}	V
Output voltage	V_{OUT}	V_{SS} -0.3V to V_{DD} +0.3V ≤ V_{SS} + 6V	V
Output current	I_{OUT}	±25	mA
Power dissipation	P_D	200	mW
Operating temperature	T_{opr}	-40 to 105	°C
Storage temperature	T_{stg}	-55 to 150	°C

Note1: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ratings (Ta = -40 to 105°C)

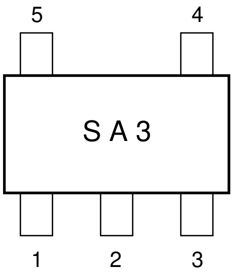
Characteristics	Symbol	Rating	Unit
Supply voltage	V_{DD} - V_{SS}	1.8 to 5.5	V

Note2: A higher load capacitance will increase the risk of voltage oscillation. Allow sufficient capacitance value when designing your circuit and using this product to prevent voltage oscillation.

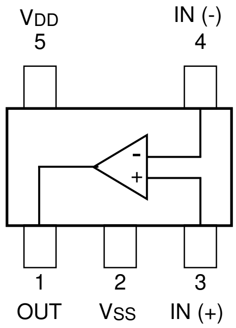
Note3: This device is sensitive to electrostatic discharge.
Please ensure equipment, operator and tools are adequately earthed when handling.

Start of commercial production
2020-09

Marking (top view)



Pin Assignment (top view)



Electrical Characteristics

DC Characteristics (V_{DD} = 1.8V, V_{SS} = GND, Ta = 25°C, V_{IN} = V_{DD}/2, unless otherwise noted.)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input offset voltage	V_{IO}	1	R_S = 1 kΩ, R_F = 100kΩ Ta = -40 to 105°C	-1.85	0.3	1.85	mV
			R_S = 1 kΩ, R_F = 100kΩ Ta = 25°C	-1.5	0.3	1.5	mV
Input offset voltage drift	V_{IO}drift	1	R_S = 1 kΩ, R_F = 100kΩ	-	1	-	μV/°C
Input offset current	I_{IO}	2	-	-	1	-	pA
Input bias current	I_I	2	-	-	1	-	pA
Common mode input voltage	CMV_{IN}	3	R_S = 1 kΩ, R_F = 100kΩ	0	-	V_{DD}	V
Voltage gain (open loop)	G_V	-	-	85	100	-	dB
Maximum output voltage	V_{OH}	4	R_L ≥ 100 kΩ	1.7	-	-	V
	V_{OL}	5	R_L ≥ 100 kΩ	-	-	0.1	
Common mode input signal rejection ratio	CMRR	3	V_{IN} = 0 to 1.8V	60	80	-	dB
Supply voltage rejection ratio	SVRR	1	V_{DD} = 1.8 to 5.0V	70	85	-	dB
Supply current	I_{DD}	6	-	-	100	165	μA
Source current	I_{source}	7	-	1.2	2	-	mA
Sink current	I_{sink}	8	-	1	2	-	mA

AC Characteristics (V_{DD} = 0.9 V, V_{SS} = -0.9 V, Ta = 25°C)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Unity Gain Cross Frequency	f_T	-	-	-	0.3	-	MHz
Phase margin	Φm	-	-	-	40	-	degrees
Slew Rate	SR	-	-	-	0.52	-	V/μs

DC Characteristics (V_{DD} = 3.3V, V_{SS} = GND, Ta = 25°C, V_{IN} = V_{DD}/2, unless otherwise noted.)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input offset voltage	V_{IO}	1	R_S = 1 kΩ, R_F = 100kΩ Ta = -40 to 105°C	-2.15	0.4	2.15	mV
			R_S = 1 kΩ, R_F = 100kΩ Ta = 25°C	-1.85	0.4	1.85	mV
Input offset voltage drift	V_{IO}drift	1	R_S = 1 kΩ, R_F = 100kΩ	-	2	-	μV/°C
Input offset current	I_{IO}	2	-	-	1	-	pA
Input bias current	I_I	2	-	-	1	-	pA
Common mode input voltage	CMV_{IN}	3	R_S = 1 kΩ, R_F = 100kΩ	0	-	V_{DD}	V
Voltage gain (open loop)	G_V	-	-	100	125	-	dB
Maximum output voltage	V_{OH}	4	R_L ≥ 100 kΩ	3.2	-	-	V
	V_{OL}	5	R_L ≥ 100 kΩ	-	-	0.1	
Common mode input signal rejection ratio	CMRR	3	V_{IN} = 0 to 3.3V	65	90	-	dB
Supply current	I_{DD}	6	-	-	100	165	μA
Source current	I_{source}	7	-	6	10	-	mA
Sink current	I_{sink}	8	-	6	10	-	mA

AC Characteristics (V_{DD} = 1.65 V, V_{SS} = -1.65 V, Ta = 25°C)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Unity Gain Cross Frequency	f_T	-	-	-	0.36	-	MHz
Phase margin	Φm	-	-	-	60	-	degrees
Slew Rate	SR	-	-	-	0.4	-	V/μs

DC Characteristics (V_{DD} = 5.0V, V_{SS} = GND, Ta = 25°C, V_{IN} = V_{DD}/2, unless otherwise noted.)

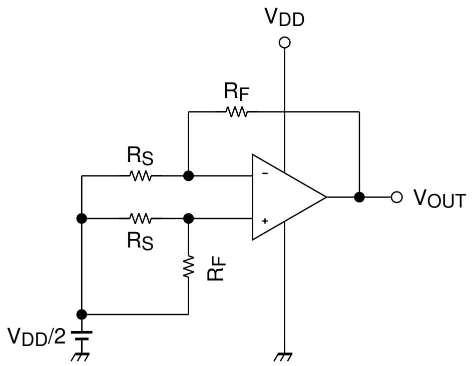
Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input offset voltage	V_{IO}	1	R_S = 1 kΩ, R_F = 100kΩ Ta = -40 to 105°C	-2.15	0.4	2.15	mV
			R_S = 1 kΩ, R_F = 100kΩ Ta = 25°C	-1.85	0.4	1.85	mV
Input offset voltage drift	V_{IO}drift	1	R_S = 1 kΩ, R_F = 100kΩ	-	2	-	µV/°C
Input offset current	I_{IO}	2	-	-	1	-	pA
Input bias current	I_I	2	-	-	1	-	pA
Common mode input voltage	CMV_{IN}	3	R_S = 1 kΩ, R_F = 100kΩ	0	-	V_{DD}	V
Voltage gain (open loop)	G_V	-	-	100	125	-	dB
Maximum output voltage	V_{OH}	4	$R_L \geq$ 100 kΩ	4.9	-	-	V
	V_{OL}	5	$R_L \geq$ 100 kΩ	-	-	0.1	
Common mode input signal rejection ratio	CMRR	3	V_{IN} = 0 to 5.0V	68	90	-	dB
Supply current	I_{DD}	6	-	-	115	190	µA
Source current	I_{source}	7	-	17	-	-	mA
Sink current	I_{sink}	8	-	17	-	-	mA

AC Characteristics (V_{DD} = 2.5 V, V_{SS} = -2.5 V, Ta = 25°C)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Unity Gain Cross Frequency	f_T	-	-	-	0.37	-	MHz
Phase margin	Φm	-	-	-	60	-	degrees
Slew Rate	SR	-	-	-	0.4	-	V/µs

Test Circuit

1. SVRR, VIO



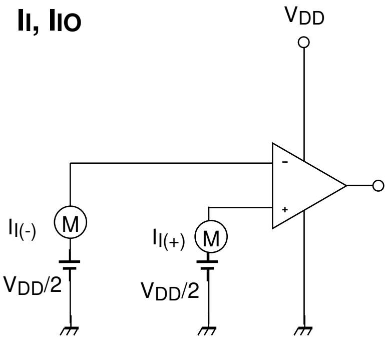
- SVRR
- For each of the two VDD values, measure the VOUT value, as indicated below, and calculate the value of SVRR using the equation shown.
  When VDD = 1.8 V, VDD = VDD1 and VOUT = VOUT1
  When VDD = 5.0 V, VDD = VDD2 and VOUT = VOUT2

$$SVRR=20\log\left[\left|\frac{V_{DD1}-V_{DD2}}{\left\{V_{OUT1}-\left(\frac{V_{DD1}}{2}\right)\right\}-\left\{V_{OUT2}-\left(\frac{V_{DD2}}{2}\right)\right\}}\right|\times\frac{R_F+R_S}{R_S}\right]$$

- VIO
  Measure the value of VOUT and calculate the value of VIO using the following equation.

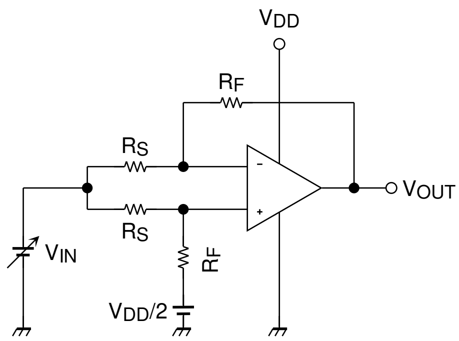
$$V_{IO}=\left(V_{OUT}-\frac{V_{DD}}{2}\right)\times\frac{R_S}{R_F+R_S}$$

2. II, IIO



- $I_I = (|I_{I(-)}| + |I_{I(+)}|) / 2$
- $I_{IO} = |I_{I(-)}| - |I_{I(+)}|$

3. CMRR, CMVIN

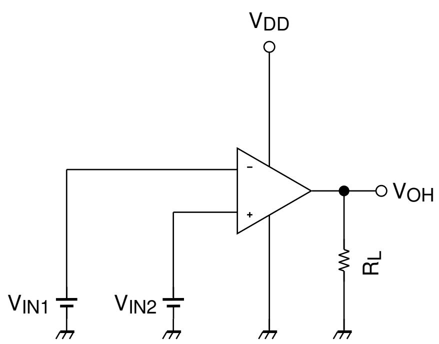


- CMRR
  Measure the VOUT value, as indicated below, and calculate the value of the CMRR using the equation shown.
  When VIN = 0 V, VIN = VIN1 and VOUT = VOUT1
  When VIN = 3.3 V, VIN = VIN2 and VOUT = VOUT2

$$CMRR=20\log\left(\left|\frac{V_{IN1}-V_{IN2}}{V_{OUT1}-V_{OUT2}}\right|\times\frac{R_F+R_S}{R_S}\right)$$

- CMVIN
  Input range within which the CMRR specification guarantees VOUT value (as varied by the VIN value).

4. VOH

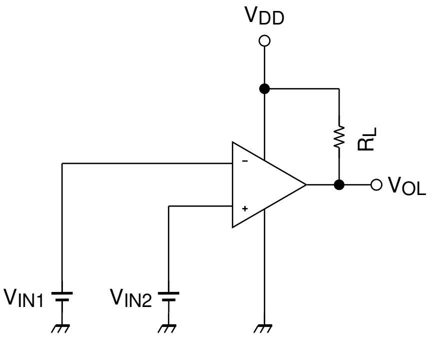


- VOH

$$V_{IN1}=\frac{V_{DD}}{2}-0.05V$$

$$V_{IN2}=\frac{V_{DD}}{2}+0.05V$$

5. V_{OL}

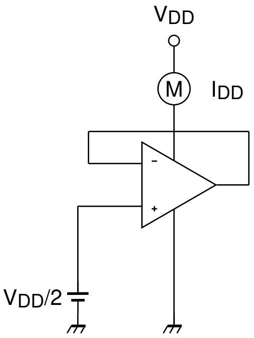


- V_{OL}

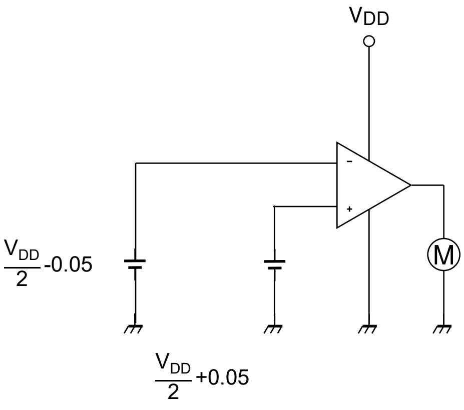
  $V_{IN1} = \frac{V_{DD}}{2} + 0.05V$

  $V_{IN2} = \frac{V_{DD}}{2} - 0.05V$

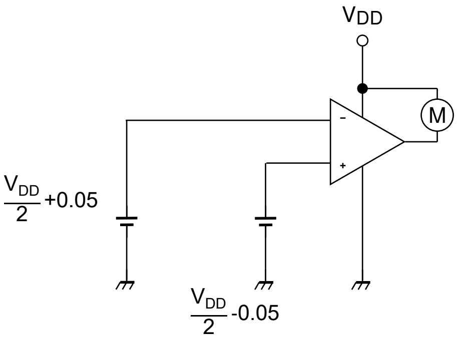
6. I_{DD}



7. I_{source}

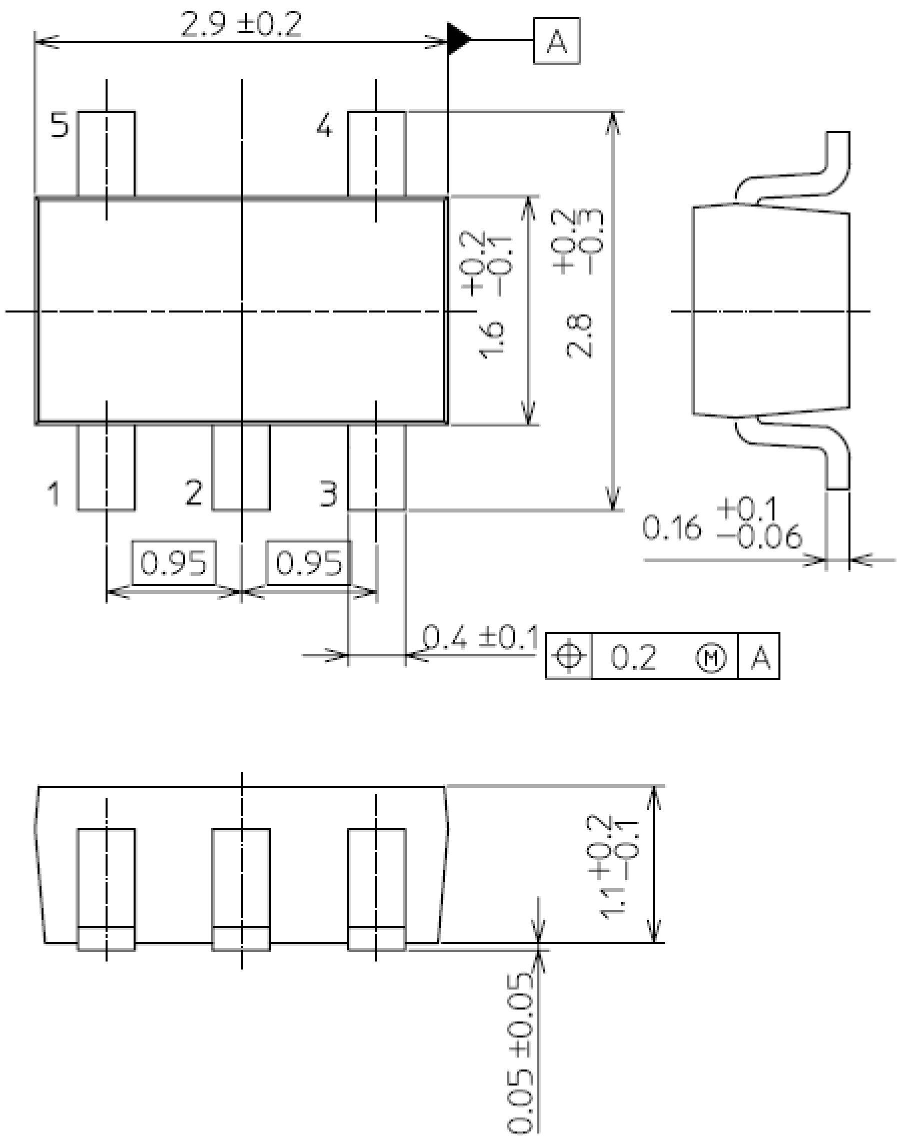


8. I_{sink}



Package Dimensions

SMV (SOT-25)(SC-74A) **Unit: mm**



Weight : 14 mg (typ.)

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