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DS21FT40
Four x Three 12 Channel E1 Framer

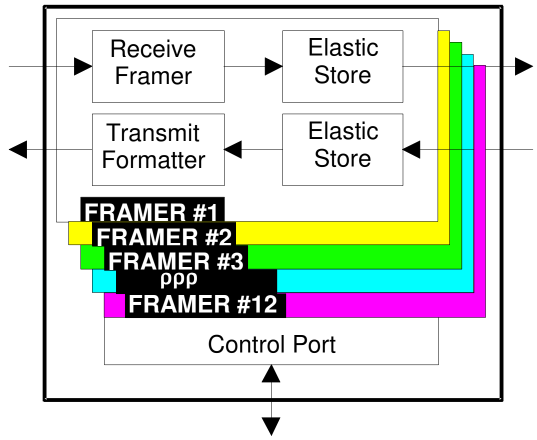
MULTI-CHIP MODULE FEATURES

- Twelve (12) completely independent E1 Framers in one small 27 mm x 27 mm Package
- Each Multi-Chip Module (MCM) Contains Three DS21Q44 Quad E1 Framer Die
- Each Quad Framer can be concatenated into a Single 8.192 MHz Backplane Data Stream
- 300–pin MCM 1.27 mm pitch BGA package (27 mm X 27 mm)
- Low Power 3.3V CMOS with 5V Tolerant Input & Outputs

FRAMER FEATURES

- All framers are fully independent; transmit and receive sections of each framer are fully independent
- Frames to FAS, CAS, CCS, and CRC4 formats
- Each framer contains dual two–frame elastic store slip buffers that can connect to asynchronous backplanes up to 8.192 MHz
- 8–bit parallel control port that can be used directly on either multiplexed or non–multiplexed buses (Intel or Motorola)
- Easy access to Si and Sa bits
- Extracts and inserts CAS signaling

FUNCTIONAL DIAGRAM



- Large counters for bipolar and code violations, CRC4 code word errors, FAS word errors, and E-bits
- Programmable output clocks for Fractional E1, per channel loopback, H0 and H12 applications
- Integral HDLC controller with 64-byte buffers. Configurable for Sa bits or DS0 operation
- Detects and generates AIS, remote alarm, and remote multiframe alarms
- IEEE 1149.1 support

DESCRIPTION

The DS21FT40 MCM offers a high density packaging arrangement for the DS21Q44 E1 Enhanced Quad Framer. Three DS21Q44 silicon die are packaged in a Multi-Chip Module (MCM) with the electrical connections as shown in Figure 1-1. The DS21FT40 is closely related to the DS21FT44. Most of the functions of the DS21FT44 are available on the DS21FT40. The differences are listed in Table 1-1. Table 2-1 lists all of the signals on the MCM.

The DS21Q44 E1 Framer is an enhanced version of the DS21Q43 Quad E1 Framer. Each DS21Q44 die contains four framers that are configured and read through a common microprocessor-compatible parallel port. Each framer consists of a receive framer, receive elastic store, transmit formatter and transmit elastic store. All four framers in the DS21Q44 are totally independent, they do not share a common framing synchronizer. Also, the transmit and receive sides of each framer are totally independent. The dual two-frame elastic stores contained in each of the four framers can be independently enabled and disabled as required. The device fully meets all of the latest E1 specifications including CCITT/ITU G.704, G.706, G.962, and I.431 as well as ETS 300 011 and ETS 300 233.

Functional Description

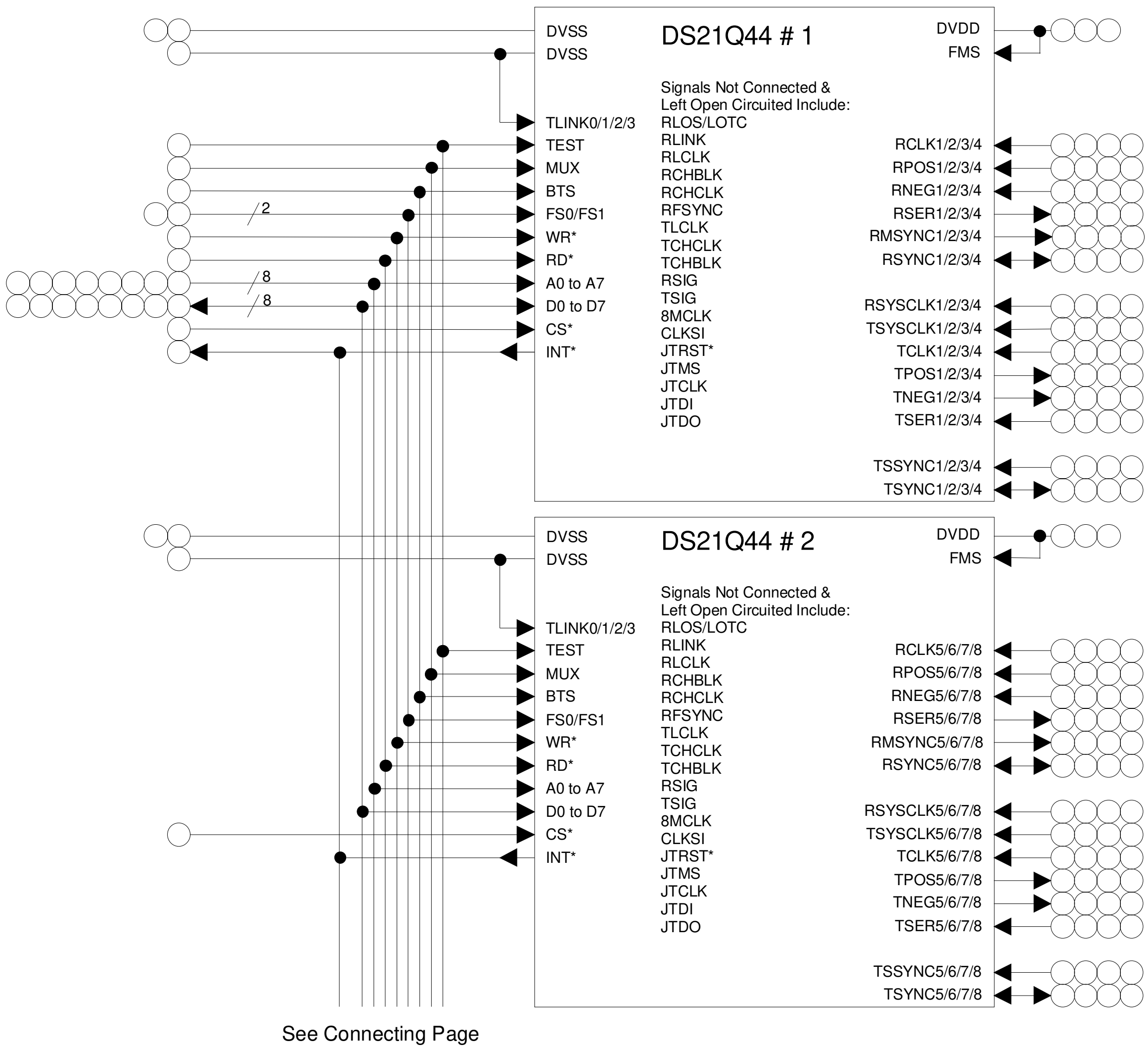
The receive side in each framer locates FAS frame and CRC and CAS multiframe boundaries as well as detects incoming alarms including, carrier loss, loss of synchronization, AIS and Remote Alarm. If needed, the receive side elastic store can be enabled in order to absorb the phase and frequency differences between the recovered E1 data stream and an asynchronous backplane clock which is provided at the RSYSCLK input. The clock applied at the RSYSCLK input can be either a 2.048 MHz clock or a 1.544 MHz clock. The RSYSCLK can be a burst clock with speeds up to 8.192 MHz.

The transmit side in each framer is totally independent from the receive side in both the clock requirements and characteristics. Data off of a backplane can be passed through a transmit side elastic store if necessary. The transmit formatter will provide the necessary frame/multiframe data overhead for E1 transmission.

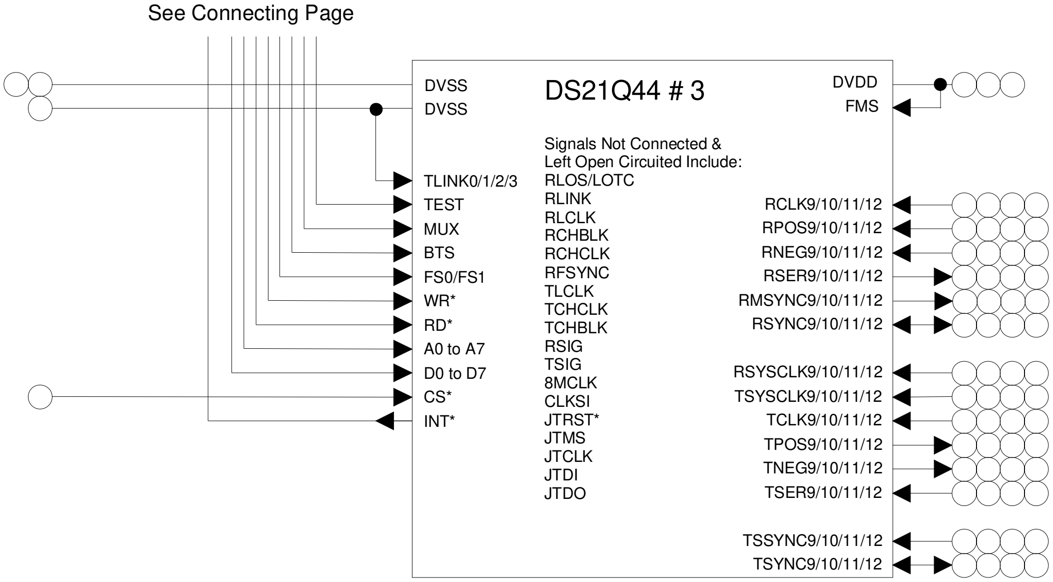
Reader's Note: This data sheet assumes a particular nomenclature of the E1 operating environment. In each 125 us frame, there are 32 8–bit timeslots numbered 0 to 31. Timeslot 0 is transmitted first and received first. These 32 timeslots are also referred to as channels with a numbering scheme of 1 to 32. Timeslot 0 is identical to channel 1, timeslot 1 is identical to Channel 2, and so on. Each timeslot (or channel) is made up of 8 bits which are numbered 1 to 8. Bit number 1 is the MSB and is transmitted first. Bit number 8 is the LSB and is transmitted last. Throughout this data sheet, the following abbreviations will be used:

FAS	Frame Alignment Signal
CAS	Channel Associated Signaling
MF	Multiframe
Si	International bits
CRC4	Cyclical Redundancy Check
CCS	Common Channel Signaling
Sa	Additional bits
E-bit	CRC4 Error Bits

DS21FT40 Schematic Figure 1-1



DS21FT40 Schematic Figure 1-1 (continued)



Changes in DS21FT40 compared to DS21FT44 Table 1-1

1. The SYSCLK pins have been separated into TSYSCLK and RSYSCLK pins.
2. RMSYNC pins have been added.
3. FMS tied to Vdd.
4. The following signals are not available:
   RSIG / TSIG / 8MCLK / CLKSI / JTRST* / JTMS / JTCLK / JTDI / JTDO

DS21FT40 ENHANCED 12-Channel E1 FRAMER Figure 1-2

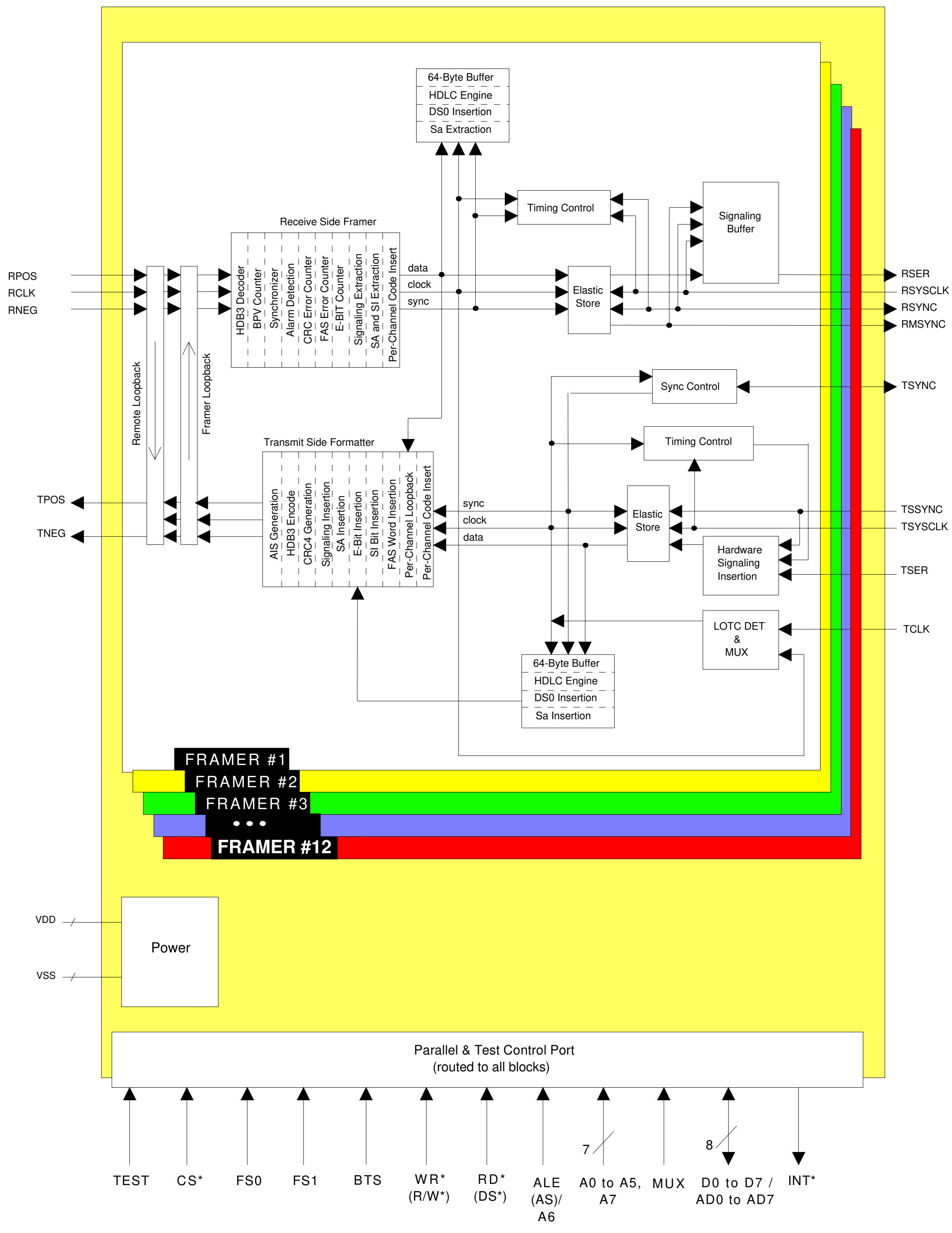


TABLE OF CONTENTS

DOCUMENT REVISION HISTORY

Revision	Notes
5-18-99	Initial Release
8-19-99	Concatenated DS21FT40 and DS21Q44 data sheets
8-26-99	Remove RCHBLK pins.
2-17-00	Corrected error in Figure 1-1 (removed RCHBLK pins).

1. DS21FT40 PIN DESCRIPTION

Pin Description Sorted by Pin Number Table 2-1

Lead	Symbols	I/O	Description
G20	A0	I	Address Bus Bit 0 (lsb).
H20	A1	I	Address Bus Bit 1.
G19	A2	I	Address Bus Bit 2.
H19	A3	I	Address Bus Bit 3.
G18	A4	I	Address Bus Bit 4.
H18	A5	I	Address Bus Bit 5.
G17	A6	I	Address Bus Bit 6.
H17	A7	I	Address Bus Bit 7 (msb).
W15	BTS	I	Bus Timing Select. 0 = Intel / 1 = Motorola.
T8	CS1*	I	Chip Select for Quad Framer 1.
Y4	CS2*	I	Chip Select for Quad Framer 2.
Y15	CS3*	I	Chip Select for Quad Framer 3.
L20	D0	I/O	Data Bus Bit 0 (lsb).
M20	D1	I/O	Data Bus Bit 1.
L19	D2	I/O	Data Bus Bit 2.
M19	D3	I/O	Data Bus Bit 3.
L18	D4	I/O	Data Bus Bit 4.
M18	D5	I/O	Data Bus Bit 5.
L17	D6	I/O	Data Bus Bit 6.
M17	D7	I/O	Data Bus Bit 7 (msb).
C7	DVDD1	–	Digital Positive Supply for Framer 1.
E4	DVDD1	–	Digital Positive Supply for Framer 1.
D2	DVDD1	–	Digital Positive Supply for Framer 1.
K3	DVDD2	–	Digital Positive Supply for Framer 2.
U7	DVDD2	–	Digital Positive Supply for Framer 2.
P2	DVDD2	–	Digital Positive Supply for Framer 2.
V19	DVDD3	–	Digital Positive Supply for Framer 3.
T12	DVDD3	–	Digital Positive Supply for Framer 3.
L16	DVDD3	–	Digital Positive Supply for Framer 3.
E9	DVSS1	–	Digital Signal Ground for Framer 1.
A6	DVSS1	–	Digital Signal Ground for Framer 1.
D5	DVSS1	–	Digital Signal Ground for Framer 1.
U3	DVSS2	–	Digital Signal Ground for Framer 2.
K4	DVSS2	–	Digital Signal Ground for Framer 2.
U8	DVSS2	–	Digital Signal Ground for Framer 2.
U4	DVSS3	–	Digital Signal Ground for Framer 3.
R16	DVSS3	–	Digital Signal Ground for Framer 3.
Y20	DVSS3	–	Digital Signal Ground for Framer 3.
Y14	FS0	I	Framer Select 0 for the Parallel Control Port.
W14	FS1	I	Framer Select 1 for the Parallel Control Port.
G16	INT*	O	Interrupt for all four Quad Framers.
P17	MUX	I	Bus Operation Select. 0 = non-multiplexed bus / 1 =

Lead	Symbols	I/O	Description
			multiplexed bus
A2	RCLK1	I	Receive Clock for Framer 1
K1	RCLK2	I	Receive Clock for Framer 2.
D10	RCLK3	I	Receive Clock for Framer 3.
B9	RCLK4	I	Receive Clock for Framer 4.
M3	RCLK5	I	Receive Clock for Framer 5.
V1	RCLK6	I	Receive Clock for Framer 6.
W6	RCLK7	I	Receive Clock for Framer 7.
J3	RCLK8	I	Receive Clock for Framer 8.
T9	RCLK9	I	Receive Clock for Framer 9.
W10	RCLK10	I	Receive Clock for Framer 10.
Y18	RCLK11	I	Receive Clock for Framer 11.
N17	RCLK12	I	Receive Clock for Framer 12.
E18	RD*	I	Read Input.
D3	RMSYNC1	O	Receive Multiframe Sync from Framer 1
G2	RMSYNC2	O	Receive Multiframe Sync from Framer 2
D4	RMSYNC3	O	Receive Multiframe Sync from Framer 3
D8	RMSYNC4	O	Receive Multiframe Sync from Framer 4
N2	RMSYNC5	O	Receive Multiframe Sync from Framer 5
V4	RMSYNC6	O	Receive Multiframe Sync from Framer 6
V6	RMSYNC7	O	Receive Multiframe Sync from Framer 7
K5	RMSYNC8	O	Receive Multiframe Sync from Framer 8
U10	RMSYNC9	O	Receive Multiframe Sync from Framer 9
Y11	RMSYNC10	O	Receive Multiframe Sync from Framer 10
W19	RMSYNC11	O	Receive Multiframe Sync from Framer 11
U20	RMSYNC12	O	Receive Multiframe Sync from Framer 12
B2	RNEG1	I	Receive Negative Data for Framer 1.
H2	RNEG2	I	Receive Negative Data for Framer 2.
D9	RNEG3	I	Receive Negative Data for Framer 3.
A9	RNEG4	I	Receive Negative Data for Framer 4.
M2	RNEG5	I	Receive Negative Data for Framer 5.
V3	RNEG6	I	Receive Negative Data for Framer 6.
V7	RNEG7	I	Receive Negative Data for Framer 7.
P3	RNEG8	I	Receive Negative Data for Framer 8.
U9	RNEG9	I	Receive Negative Data for Framer 9.
W11	RNEG10	I	Receive Negative Data for Framer 10.
W17	RNEG11	I	Receive Negative Data for Framer 11.
T20	RNEG12	I	Receive Negative Data for Framer 12.
A1	RPOS1	I	Receive Positive Data for Framer 1.
H1	RPOS2	I	Receive Positive Data for Framer 2.
H4	RPOS3	I	Receive Positive Data for Framer 3.
C9	RPOS4	I	Receive Positive Data for Framer 4.
M1	RPOS5	I	Receive Positive Data for Framer 5.
W2	RPOS6	I	Receive Positive Data for Framer 6.
V5	RPOS7	I	Receive Positive Data for Framer 7.

Lead	Symbols	I/O	Description
P4	RPOS8	I	Receive Positive Data for Framer 8.
T10	RPOS9	I	Receive Positive Data for Framer 9.
V11	RPOS10	I	Receive Positive Data for Framer 10.
Y19	RPOS11	I	Receive Positive Data for Framer 11.
R19	RPOS12	I	Receive Positive Data for Framer 12.
C1	RSER1	O	Receive Serial Data from Framer 1.
H3	RSER2	O	Receive Serial Data from Framer 2.
C6	RSER3	O	Receive Serial Data from Framer 3.
C8	RSER4	O	Receive Serial Data from Framer 4.
P1	RSER5	O	Receive Serial Data from Framer 5.
W4	RSER6	O	Receive Serial Data from Framer 6.
T7	RSER7	O	Receive Serial Data from Framer 7.
N4	RSER8	O	Receive Serial Data from Framer 8.
U11	RSER9	O	Receive Serial Data from Framer 9.
Y12	RSER10	O	Receive Serial Data from Framer 10.
V16	RSER11	O	Receive Serial Data from Framer 11.
T16	RSER12	O	Receive Serial Data from Framer 12.
B1	RSYNC1	I/O	Receive Frame/Multiframe Sync for Framer 1.
G1	RSYNC2	I/O	Receive Frame/Multiframe Sync for Framer 2.
D6	RSYNC3	I/O	Receive Frame/Multiframe Sync for Framer 3.
A7	RSYNC4	I/O	Receive Frame/Multiframe Sync for Framer 4.
N3	RSYNC5	I/O	Receive Frame/Multiframe Sync for Framer 5.
Y2	RSYNC6	I/O	Receive Frame/Multiframe Sync for Framer 6.
U5	RSYNC7	I/O	Receive Frame/Multiframe Sync for Framer 7.
J4	RSYNC8	I/O	Receive Frame/Multiframe Sync for Framer 8.
T11	RSYNC9	I/O	Receive Frame/Multiframe Sync for Framer 9.
V13	RSYNC10	I/O	Receive Frame/Multiframe Sync for Framer 10.
V15	RSYNC11	I/O	Receive Frame/Multiframe Sync for Framer 11.
P18	RSYNC12	I/O	Receive Frame/Multiframe Sync for Framer 12.
B5	RSYSCLK1	I	Receive System Clock for Framer 1.
E2	RSYSCLK2	I	Receive System Clock for Framer 2.
E5	RSYSCLK3	I	Receive System Clock for Framer 3.
B8	RSYSCLK4	I	Receive System Clock for Framer 4.
M4	RSYSCLK5	I	Receive System Clock for Framer 5.
T2	RSYSCLK6	I	Receive System Clock for Framer 6.
Y5	RSYSCLK7	I	Receive System Clock for Framer 7.
W3	RSYSCLK8	I	Receive System Clock for Framer 8.
T4	RSYSCLK9	I	Receive System Clock for Framer 9.
Y9	RSYSCLK10	I	Receive System Clock for Framer 10.
U12	RSYSCLK11	I	Receive System Clock for Framer 11.
R17	RSYSCLK12	I	Receive System Clock for Framer 12.
D1	TCLK1	I	Transmit Clock for Framer 1.
H5	TCLK2	I	Transmit Clock for Framer 2.
C5	TCLK3	I	Transmit Clock for Framer 3.
A5	TCLK4	I	Transmit Clock for Framer 4.

Lead	Symbols	I/O	Description
R1	TCLK5	I	Transmit Clock for Framer 5.
Y3	TCLK6	I	Transmit Clock for Framer 6.
T6	TCLK7	I	Transmit Clock for Framer 7.
K2	TCLK8	I	Transmit Clock for Framer 8.
U13	TCLK9	I	Transmit Clock for Framer 9.
Y13	TCLK10	I	Transmit Clock for Framer 10.
T18	TCLK11	I	Transmit Clock for Framer 11.
P16	TCLK12	I	Transmit Clock for Framer 12.
A13	TEST	I	Tri-State. 0 = do not tri-state / 1 = tri-state all outputs & I/O signals
C3	TNEG1	O	Transmit Negative Data from Framer 1.
J1	TNEG2	O	Transmit Negative Data from Framer 2.
F5	TNEG3	O	Transmit Negative Data from Framer 3.
A10	TNEG4	O	Transmit Negative Data from Framer 4.
L1	TNEG5	O	Transmit Negative Data from Framer 5.
V2	TNEG6	O	Transmit Negative Data from Framer 6.
V8	TNEG7	O	Transmit Negative Data from Framer 7.
P5	TNEG8	O	Transmit Negative Data from Framer 8.
U14	TNEG9	O	Transmit Negative Data from Framer 9.
V12	TNEG10	O	Transmit Negative Data from Framer 10.
W18	TNEG11	O	Transmit Negative Data from Framer 11.
T19	TNEG12	O	Transmit Negative Data from Framer 12.
B3	TPOS1	O	Transmit Positive Data from Framer 1.
J2	TPOS2	O	Transmit Positive Data from Framer 2.
J5	TPOS3	O	Transmit Positive Data from Framer 3.
B10	TPOS4	O	Transmit Positive Data from Framer 4.
L2	TPOS5	O	Transmit Positive Data from Framer 5.
W1	TPOS6	O	Transmit Positive Data from Framer 6.
W7	TPOS7	O	Transmit Positive Data from Framer 7.
R3	TPOS8	O	Transmit Positive Data from Framer 8.
T14	TPOS9	O	Transmit Positive Data from Framer 9.
Y10	TPOS10	O	Transmit Positive Data from Framer 10.
V18	TPOS11	O	Transmit Positive Data from Framer 11.
V20	TPOS12	O	Transmit Positive Data from Framer 12.
B4	TSER1	I	Transmit Serial Data for Framer 1.
E1	TSER2	I	Transmit Serial Data for Framer 2.
F3	TSER3	I	Transmit Serial Data for Framer 3.
D7	TSER4	I	Transmit Serial Data for Framer 4.
L5	TSER5	I	Transmit Serial Data for Framer 5.
T1	TSER6	I	Transmit Serial Data for Framer 6.
Y6	TSER7	I	Transmit Serial Data for Framer 7.
T3	TSER8	I	Transmit Serial Data for Framer 8.
M16	TSER9	I	Transmit Serial Data for Framer 9.
W9	TSER10	I	Transmit Serial Data for Framer 10.
W16	TSER11	I	Transmit Serial Data for Framer 11.

Lead	Symbols	I/O	Description
W20	TSER12	I	Transmit Serial Data for Framer 12.
A3	TSSYNC1	I	Transmit System Sync for Framer 1.
F2	TSSYNC2	I	Transmit System Sync for Framer 2.
G5	TSSYNC3	I	Transmit System Sync for Framer 3.
E8	TSSYNC4	I	Transmit System Sync for Framer 4.
L4	TSSYNC5	I	Transmit System Sync for Framer 5.
U1	TSSYNC6	I	Transmit System Sync for Framer 6.
Y7	TSSYNC7	I	Transmit System Sync for Framer 7.
R4	TSSYNC8	I	Transmit System Sync for Framer 8.
T15	TSSYNC9	I	Transmit System Sync for Framer 9.
W8	TSSYNC10	I	Transmit System Sync for Framer 10.
Y17	TSSYNC11	I	Transmit System Sync for Framer 11.
U19	TSSYNC12	I	Transmit System Sync for Framer 12.
E3	TSYNC1	I/O	Transmit Sync for Framer 1.
F4	TSYNC2	I/O	Transmit Sync for Framer 2.
E7	TSYNC3	I/O	Transmit Sync for Framer 3.
A4	TSYNC4	I/O	Transmit Sync for Framer 4.
R2	TSYNC5	I/O	Transmit Sync for Framer 5.
W5	TSYNC6	I/O	Transmit Sync for Framer 6.
T5	TSYNC7	I/O	Transmit Sync for Framer 7.
M5	TSYNC8	I/O	Transmit Sync for Framer 8.
T13	TSYNC9	I/O	Transmit Sync for Framer 9.
W13	TSYNC10	I/O	Transmit Sync for Framer 10.
U16	TSYNC11	I/O	Transmit Sync for Framer 11.
N16	TSYNC12	I/O	Transmit Sync for Framer 12.
C4	TSYSCLK1	I	Transmit System Clock for Framer 1.
F1	TSYSCLK2	I	Transmit System Clock for Framer 2.
G4	TSYSCLK3	I	Transmit System Clock for Framer 3.
C10	TSYSCLK4	I	Transmit System Clock for Framer 4.
L3	TSYSCLK5	I	Transmit System Clock for Framer 5.
U2	TSYSCLK6	I	Transmit System Clock for Framer 6.
V9	TSYSCLK7	I	Transmit System Clock for Framer 7.
R5	TSYSCLK8	I	Transmit System Clock for Framer 8.
U15	TSYSCLK9	I	Transmit System Clock for Framer 9.
V10	TSYSCLK10	I	Transmit System Clock for Framer 10.
U18	TSYSCLK11	I	Transmit System Clock for Framer 11.
R18	TSYSCLK12	I	Transmit System Clock for Framer 12.
Y16	WR*	I	Write Input.
A11	NC	–	No Connect
A12	NC	–	No Connect
A14	NC	–	No Connect
A15	NC	–	No Connect
A16	NC	–	No Connect
A17	NC	–	No Connect
A18	NC	–	No Connect

Lead	Symbols	I/O	Description
A19	NC	–	No Connect
A20	NC	–	No Connect
A8	NC	–	No Connect
B11	NC	–	No Connect
B12	NC	–	No Connect
B13	NC	–	No Connect
B14	NC	–	No Connect
B15	NC	–	No Connect
B16	NC	–	No Connect
B17	NC	–	No Connect
B18	NC	–	No Connect
B19	NC	–	No Connect
B20	NC	–	No Connect
B6	NC	–	No Connect
B7	NC	–	No Connect
C11	NC	–	No Connect
C12	NC	–	No Connect
C13	NC	–	No Connect
C14	NC	–	No Connect
C15	NC	–	No Connect
C16	NC	–	No Connect
C17	NC	–	No Connect
C18	NC	–	No Connect
C19	NC	–	No Connect
C2	NC	–	No Connect
C20	NC	–	No Connect
D11	NC	–	No Connect
D12	NC	–	No Connect
D13	NC	–	No Connect
D14	NC	–	No Connect
D15	NC	–	No Connect
D16	NC	–	No Connect
D17	NC	–	No Connect
D18	NC	–	No Connect
D19	NC	–	No Connect
D20	NC	–	No Connect
E10	NC	–	No Connect
E11	NC	–	No Connect
E12	NC	–	No Connect
E13	NC	–	No Connect
E14	NC	–	No Connect
E15	NC	–	No Connect
E16	NC	–	No Connect
E17	NC	–	No Connect
E19	NC	–	No Connect

Lead	Symbols	I/O	Description
E20	NC	–	No Connect
E6	NC	–	No Connect
F16	NC	–	No Connect
F17	NC	–	No Connect
F18	NC	–	No Connect
F19	NC	–	No Connect
F20	NC	–	No Connect
G3	NC	–	No Connect
H16	NC	–	No Connect
J16	NC	–	No Connect
J17	NC	–	No Connect
J18	NC	–	No Connect
J19	NC	–	No Connect
J20	NC	–	No Connect
K16	NC	–	No Connect
K17	NC	–	No Connect
K18	NC	–	No Connect
K19	NC	–	No Connect
K20	NC	–	No Connect
N1	NC	–	No Connect
N18	NC	–	No Connect
N19	NC	–	No Connect
N20	NC	–	No Connect
N5	NC	–	No Connect
P19	NC	–	No Connect
P20	NC	–	No Connect
R20	NC	–	No Connect
T17	NC	–	No Connect
U17	NC	–	No Connect
U6	NC	–	No Connect
V14	NC	–	No Connect
V17	NC	–	No Connect
W12	NC	–	No Connect
Y1	NC	–	No Connect
Y8	NC	–	No Connect

DS21FT40 PCB Land Pattern Figure 2-1

The diagram shown below is the lead pattern that will be placed on the target PCB. This is the same pattern that would be seen as viewed through the MCM from the top.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	rpos 1	rclk 1	ts sync1	tsync 4	tclk 4	dvss 1	rsync 4	nc	rneg 4	tneg 4	nc	nc	test	ns	ns	nc	nc	nc	nc	nc
B	rsync 1	rneg 1	tpos 1	tser 1	rsys clk 1	nc	nc	rsys clk 4	rclk 4	tpos 4	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
C	rser 1	nc	tneg 1	tsys clk 1	tclk 3	rser 3	dvdd 1	rser4	rpos 4	tsys clk 4	nc	nc	nc	nc	ns	nc	nc	nc	nc	nc
D	tclk 1	dvdd 1	rm sync 1	rm sync 3	dvss 1	rsync 3	tser 4	rm sync4	rneg 3	rclk 3	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
E	tser 2	rsys clk 2	tsync 1	dvdd 1	rsys clk 3	nc	tsync 3	ts sync 4	dvss 1	nc	nc	nc	nc	nc	nc	nc	nc	rd*	nc	nc
F	tsys clk 2	ts sync 2	tser 3	tsync 2	tneg 3											nc	nc	nc	nc	nc
G	rsync 2	rm sync 2	nc	tsys clk 3	ts sync 3											int*	A6	A4	A2	A0
H	rpos 2	rneg 2	rser 2	rpos 3	tclk 2											nc	A7	A5	A3	A1
J	tneg 2	tpos 2	rclk 8	rsync 8	tpos 3											nc	nc	nc	nc	nc
K	rclk 2	tclk 8	dvdd 2	dvss 2	rm sync 8											nc	nc	nc	nc	nc
L	tneg 5	tpos 5	tsys clk 5	ts sync 5	tser 5											dvdd 3	D6	D4	D2	D0
M	rpos 5	rneg 5	rclk 5	rsys clk 5	tsync 8											tser 9	D7	D5	D3	D1
N	nc	rm sync 5	rsync 5	rser 8	nc											tsync 12	rclk 12	nc	nc	nc
P	rser 5	dvdd 2	rneg 8	rpos 8	tneg 8											tclk 12	mux	rsync 12	nc	nc
R	tclk 5	tsync 5	tpos 8	ts sync 8	tsys clk 8											dvss 3	rsys clk 12	tsys clk 12	rpos 12	nc
T	tser 6	rsys clk 6	tser 8	rsys clk 9	tsync 7	tclk 7	rser 7	cs1*	rclk 9	rpos 9	rsync 9	dvdd 3	tsync 9	tpos 9	ts sync 9	rser 12	nc	tclk 11	tneg 12	rneg 12
U	ts sync 6	tsys clk 6	dvss 2	dvss 3	rsync 7	nc	dvdd 2	dvss 2	rneg 9	rm sync 9	rser 9	rsys clk 11	tclk 9	tneg 9	tsys clk 9	tsync 11	nc	tsys clk 11	ts sync 12	rm sync 12
V	rclk 6	tneg 6	rneg 6	rm sync 6	rpos 7	rm sync 7	rneg 7	tneg 7	tsys clk 7	tsys clk 10	rpos 10	tneg 10	rsync 10	nc	rsync 11	rser 11	nc	tpos 11	dvdd 3	tpos 12
W	tpos 6	rpos 6	rsys clk 8	rser 6	tsync 6	rclk 7	tpos 7	ts sync 10	tser 10	rclk 10	rneg 10	nc	tsync 10	fs1	bts	tser 11	rneg 11	tneg 11	rm sync 11	tser 12
Y	nc	rsync 6	tclk 6	cs2*	rsys clk 7	tser 7	ts sync 7	nc	rsys clk 10	tpos 10	rm sync 10	rser 10	tclk 10	fs0	cs3*	wr*	ts sync 11	rclk 11	rpos 11	dvss 3

2. DS21FT44 PIN FUNCTION DESCRIPTION

TRANSMIT SIDE PINS

Signal Name: TCLK
Signal Description: Transmit Clock
Signal Type: Input
A 2.048 MHz primary clock. Used to clock data through the transmit side formatter.

Signal Name: TSER
Signal Description: Transmit Serial Data
Signal Type: Input
Transmit NRZ serial data. Sampled on the falling edge of TCLK when the transmit side elastic store is disabled. Sampled on the falling edge of TSYSCLK when the transmit side elastic store is enabled.

Signal Name: TSYSCLK
Signal Description: Transmit System Clock
Signal Type: Input
1.544 MHz or 2.048 MHz clock. Only used when the transmit side elastic store function is enabled. Should be tied low in applications that do not use the transmit side elastic store. Can be burst at rates up to 8.192 MHz.

Signal Name: TSYNC
Signal Description: Transmit Sync
Signal Type: Input /Output
A pulse at this pin will establish either frame or multiframe boundaries for the transmit side. This pin can also be programmed to output either a frame or multiframe pulse. Always synchronous with TCLK.

Signal Name: TSSYNC
Signal Description: Transmit System Sync
Signal Type: Input
Only used when the transmit side elastic store is enabled. A pulse at this pin will establish either frame or multiframe boundaries for the transmit side. Should be tied low in applications that do not use the transmit side elastic store. Always synchronous with TSYSCLK.

Signal Name: TPOS
Signal Description: Transmit Positive Data Output
Signal Type: Output
Updated on the rising edge of TCLK with the bipolar data out of the transmit side formatter. Can be programmed to source NRZ data via the Output Data Format (TCR1.7) control bit.

Signal Name: TNEG
Signal Description: Transmit Negative Data Output
Signal Type: Output
Updated on the rising edge of TCLK with the bipolar data out of the transmit side formatter.

RECEIVE SIDE PINS

Signal Name: RCLK
Signal Description: Receive Clock Input
Signal Type: Input
2.048 MHz clock that is used to clock data through the receive side framer.

Signal Name: RSER
Signal Description: Receive Serial Data
Signal Type: Output
Received NRZ serial data. Updated on rising edges of RCLK when the receive side elastic store is disabled. Updated on the rising edges of RSYSCLK when the receive side elastic store is enabled.

Signal Name: RSYNC
Signal Description: Receive Sync
Signal Type: Input /Output
An extracted pulse, one RCLK wide, is output at this pin which identifies either frame or CAS/CRC multiframe boundaries. If the receive side elastic store is enabled, then this pin can be enabled to be an input at which a frame or multiframe boundary pulse synchronous with RSYSCLK is applied.

Signal Name: RMSYNC
Signal Description: Receive Multiframe Sync
Signal Type: Output
An extracted pulse, one RSYSCLK wide, is output at this pin which identifies multiframe boundaries. If the receive side elastic store is disabled, then this output will output multiframe boundaries associated with RCLK.

Signal Name: RSYSCLK
Signal Description: Receive System Clock
Signal Type: Input
1.544 MHz or 2.048 MHz clock. Only used when the elastic store function is enabled. Should be tied low in applications that do not use the elastic store. Can be burst at rates up to 8.192 MHz.

Signal Name: RPOS
Signal Description: Receive Positive Data Input
Signal Type: Input
Sampled on the falling edge of RCLK for data to be clocked through the receive side framer. RPOS and RNEG can be tied together for an NRZ interface. Connecting RPOS to RNEG disables the bipolar violation monitoring circuitry.

Signal Name: RNEG
Signal Description: Receive Negative Data Input
Signal Type: Input
Sampled on the falling edge of RCLK for data to be clocked through the receive side framer. RPOS and RNEG can be tied together for an NRZ interface. Connecting RPOS to RNEG disables the bipolar violation monitoring circuitry.

PARALLEL CONTROL PORT PINS

Signal Name: INT*
Signal Description: Interrupt
Signal Type: Output
Flags host controller during conditions and change of conditions defined in the Status Registers 1 and 2 and the FDL Status Register. Active low, open drain output.

Signal Name: MUX
Signal Description: Bus Operation
Signal Type: Input
Set low to select non–multiplexed bus operation. Set high to select multiplexed bus operation.

Signal Name: D0 TO D7 / AD0 TO AD7
Signal Description: Data Bus or Address/Data Bus
Signal Type: Input /Output
In non–multiplexed bus operation (MUX = 0), serves as the data bus. In multiplexed bus operation (MUX = 1), serves as a 8–bit multiplexed address / data bus.

Signal Name: A0 TO A5, A7
Signal Description: Address Bus
Signal Type: Input
In non–multiplexed bus operation (MUX = 0), serves as the address bus. In multiplexed bus operation (MUX = 1), these pins are not used and should be tied low.

Signal Name: ALE (AS) / A6
Signal Description: Address Latch Enable (Address Strobe) or A6
Signal Type: Input
In non–multiplexed bus operation (MUX = 0), serves as address bit 6. In multiplexed bus operation (MUX = 1), serves to demultiplex the bus on a positive–going edge.

Signal Name: BTS
Signal Description: Bus Type Select
Signal Type: Input
Strap high to select Motorola bus timing; strap low to select Intel bus timing. This pin controls the function of the RD*(DS*), ALE(AS), and WR*(R/W*) pins. If BTS = 1, then these pins assume the function listed in parenthesis ().

Signal Name: RD* (DS)
Signal Description: Read Input (Data Strobe)
Signal Type: Input
RD* is an active low signal and DS is an active high signal.

Signal Name: FS0 AND FS1
Signal Description: Framer Selects
Signal Type: Input
Selects which of the four framers is to be accessed for a specific DS21Q44 die.

Signal Name: CS1* TO CS3*
Signal Description: Chip Select
Signal Type: Input
Must be low to read or write to a specific DS21Q44 die. These are active low signals.

Signal Name: WR* (R/W*)
Signal Description: Write Input (Read/Write)
Signal Type: Input
WR* is an active low signal.

TEST ACCESS PORT PINS

Signal Name: TEST
Signal Description: 3–State Control
Signal Type: Input
Set high to 3–state all output and I/O pins (including the parallel control port). Set low for normal operation. Useful in board level testing.

SUPPLY PINS

Signal Name: VDD
Signal Description: Positive Supply
Signal Type: Supply
2.97 to 3.63 volts.

Signal Name: VSS
Signal Description: Signal Ground
Signal Type: Supply
0.0 volts.

3. DS21FT40 REGISTER MAP

Register Map for Each Quad Framer Sorted by Address Table 3-1

ADDRESS	R/W	REGISTER NAME	REGISTER ABBREVIATION
00	R	BPV or Code Violation Count 1	VCR1
01	R	BPV or Code Violation Count 2	VCR2
02	R	CRC4 Error Count 1 / FAS Error Count 1	CRCCR1
03	R	CRC4 Error Count 2	CRCCR2
04	R	E-Bit Count 1 / FAS Error Count 2	EBCR1
05	R	E-Bit Count 2	EBCR2
06	R/W	Status 1	SR1
07	R/W	Status 2	SR2
08	R/W	Receive Information	RIR
09	R/W	Test 2	TEST2 (set to 00h)
0A	–	Not used	(set to 00H)
0B	–	Not used	(set to 00H)
0C	–	Not used	(set to 00H)

ADDRESS	R/W	REGISTER NAME	REGISTER ABBREVIATION
0D	–	Not used	(set to 00H)
0E	–	Not used	(set to 00H)
0F	R	Device ID	IDR
10	R/W	Receive Control 1	RCR1
11	R/W	Receive Control 2	RCR2
12	R/W	Transmit Control 1	TCR1
13	R/W	Transmit Control 2	TCR2
14	R/W	Common Control 1	CCR1
15	R/W	Test 1	TEST1 (set to 00h)
16	R/W	Interrupt Mask 1	IMR1
17	R/W	Interrupt Mask 2	IMR2
18	–	Not used	(set to 00H)
19	–	Not used	(set to 00H)
1A	R/W	Common Control 2	CCR2
1B	R/W	Common Control 3	CCR3
1C	R/W	Transmit Sa Bit Control	TSaCR
1D	R/W	Common Control 6	CCR6
1E	R	Synchronizer Status	SSR
1F	R	Receive Non-Align Frame	RNAF
20	R/W	Transmit Align Frame	TAF
21	R/W	Transmit Non-Align Frame	TNAF
22	R/W	Transmit Channel Blocking 1 (Not applicable to DS21FT40 – write to 00H.)	TCBR1
23	R/W	Transmit Channel Blocking 2 (Not applicable to DS21FT40 – write to 00H.)	TCBR2
24	R/W	Transmit Channel Blocking 3 (Not applicable to DS21FT40 – write to 00H.)	TCBR3
25	R/W	Transmit Channel Blocking 4 (Not applicable to DS21FT40 – write to 00H.)	TCBR4
26	R/W	Transmit Idle 1	TIR1
27	R/W	Transmit Idle 2	TIR2
28	R/W	Transmit Idle 3	TIR3
29	R/W	Transmit Idle 4	TIR4
2A	R/W	Transmit Idle Definition	TIDR
2B	R/W	Receive Channel Blocking 1	RCBR1
2C	R/W	Receive Channel Blocking 2	RCBR2
2D	R/W	Receive Channel Blocking 3	RCBR3
2E	R/W	Receive Channel Blocking 4	RCBR4
2F	R	Receive Align Frame	RAF
30	R	Receive Signaling 1	RS1

ADDRESS	R/W	REGISTER NAME	REGISTER ABBREVIATION
31	R	Receive Signaling 2	RS2
32	R	Receive Signaling 3	RS3
33	R	Receive Signaling 4	RS4
34	R	Receive Signaling 5	RS5
35	R	Receive Signaling 6	RS6
36	R	Receive Signaling 7	RS7
37	R	Receive Signaling 8	RS8
38	R	Receive Signaling 9	RS9
39	R	Receive Signaling 10	RS10
3A	R	Receive Signaling 11	RS11
3B	R	Receive Signaling 12	RS12
3C	R	Receive Signaling 13	RS13
3D	R	Receive Signaling 14	RS14
3E	R	Receive Signaling 15	RS15
3F	R	Receive Signaling 16	RS16
40	R/W	Transmit Signaling 1	TS1
41	R/W	Transmit Signaling 2	TS2
42	R/W	Transmit Signaling 3	TS3
43	R/W	Transmit Signaling 4	TS4
44	R/W	Transmit Signaling 5	TS5
45	R/W	Transmit Signaling 6	TS6
46	R/W	Transmit Signaling 7	TS7
47	R/W	Transmit Signaling 8	TS8
48	R/W	Transmit Signaling 9	TS9
49	R/W	Transmit Signaling 10	TS10
4A	R/W	Transmit Signaling 11	TS11
4B	R/W	Transmit Signaling 12	TS12
4C	R/W	Transmit Signaling 13	TS13
4D	R/W	Transmit Signaling 14	TS14
4E	R/W	Transmit Signaling 15	TS15
4F	R/W	Transmit Signaling 16	TS16
50	R/W	Transmit Si Bits Align Frame	TSiAF
51	R/W	Transmit Si Bits Non-Align Frame	TSiNAF
52	R/W	Transmit Remote Alarm Bits	TRA
53	R/W	Transmit Sa4 Bits	TSa4
54	R/W	Transmit Sa5 Bits	TSa5
55	R/W	Transmit Sa6 Bits	TSa6
56	R/W	Transmit Sa7 Bits	TSa7
57	R/W	Transmit Sa8 Bits	TSa8
58	R	Receive Si bits Align Frame	RSiAF
59	R	Receive Si bits Non-Align Frame	RSiNAF
5A	R	Receive Remote Alarm Bits	RRA
5B	R	Receive Sa4 Bits	RSa4
5C	R	Receive Sa5 Bits	RSa5

ADDRESS	R/W	REGISTER NAME	REGISTER ABBREVIATION
5D	R	Receive Sa6 Bits	RSa6
5E	R	Receive Sa7 Bits	RSa7
5F	R	Receive Sa8 Bits	RSa8
60	R/W	Transmit Channel 1	TC1
61	R/W	Transmit Channel 2	TC2
62	R/W	Transmit Channel 3	TC3
63	R/W	Transmit Channel 4	TC4
64	R/W	Transmit Channel 5	TC5
65	R/W	Transmit Channel 6	TC6
66	R/W	Transmit Channel 7	TC7
67	R/W	Transmit Channel 8	TC8
68	R/W	Transmit Channel 9	TC9
69	R/W	Transmit Channel 10	TC10
6A	R/W	Transmit Channel 11	TC11
6B	R/W	Transmit Channel 12	TC12
6C	R/W	Transmit Channel 13	TC13
6D	R/W	Transmit Channel 14	TC14
6E	R/W	Transmit Channel 15	TC15
6F	R/W	Transmit Channel 16	TC16
70	R/W	Transmit Channel 17	TC17
71	R/W	Transmit Channel 18	TC18
72	R/W	Transmit Channel 19	TC19
73	R/W	Transmit Channel 20	TC20
74	R/W	Transmit Channel 21	TC21
75	R/W	Transmit Channel 22	TC22
76	R/W	Transmit Channel 23	TC23
77	R/W	Transmit Channel 24	TC24
78	R/W	Transmit Channel 25	TC25
79	R/W	Transmit Channel 26	TC26
7A	R/W	Transmit Channel 27	TC27
7B	R/W	Transmit Channel 28	TC28
7C	R/W	Transmit Channel 29	TC29
7D	R/W	Transmit Channel 30	TC30
7E	R/W	Transmit Channel 31	TC31
7F	R/W	Transmit Channel 32	TC32
80	R/W	Receive Channel 1	RC1
81	R/W	Receive Channel 2	RC2
82	R/W	Receive Channel 3	RC3
83	R/W	Receive Channel 4	RC4
84	R/W	Receive Channel 5	RC5
85	R/W	Receive Channel 6	RC6
86	R/W	Receive Channel 7	RC7
87	R/W	Receive Channel 8	RC8
88	R/W	Receive Channel 9	RC9

ADDRESS	R/W	REGISTER NAME	REGISTER ABBREVIATION
89	R/W	Receive Channel 10	RC10
8A	R/W	Receive Channel 11	RC11
8B	R/W	Receive Channel 12	RC12
8C	R/W	Receive Channel 13	RC13
8D	R/W	Receive Channel 14	RC14
8E	R/W	Receive Channel 15	RC15
8F	R/W	Receive Channel 16	RC16
90	R/W	Receive Channel 17	RC17
91	R/W	Receive Channel 18	RC18
92	R/W	Receive Channel 19	RC19
93	R/W	Receive Channel 20	RC20
94	R/W	Receive Channel 21	RC21
95	R/W	Receive Channel 22	RC22
96	R/W	Receive Channel 23	RC23
97	R/W	Receive Channel 24	RC24
98	R/W	Receive Channel 25	RC25
99	R/W	Receive Channel 26	RC26
9A	R/W	Receive Channel 27	RC27
9B	R/W	Receive Channel 28	RC28
9C	R/W	Receive Channel 29	RC29
9D	R/W	Receive Channel 30	RC30
9E	R/W	Receive Channel 31	RC31
9F	R/W	Receive Channel 32	RC32
A0	R/W	Transmit Channel Control 1	TCC1
A1	R/W	Transmit Channel Control 2	TCC2
A2	R/W	Transmit Channel Control 3	TCC3
A3	R/W	Transmit Channel Control 4	TCC4
A4	R/W	Receive Channel Control 1	RCC1
A5	R/W	Receive Channel Control 2	RCC2
A6	R/W	Receive Channel Control 3	RCC3
A7	R/W	Receive Channel Control 4	RCC4
A8	R/W	Common Control 4	CCR4
A9	R	Transmit DS0 Monitor	TDS0M
AA	R/W	Common Control 5	CCR5
AB	R	Receive DS0 Monitor	RDS0M
AC	R/W	Test 3	TEST3 (set to 00H)
AD	–	Not used	(set to 00H)
AE	–	Not used	(set to 00H)
AF	–	Not used	(set to 00H)
B0	R/W	HDLC Control Register	HCR
B1	R/W	HDLC Status Register	HSR
B2	R/W	HDLC Interrupt Mask Register	HIMR
B3	R/W	Receive HDLC Information Register	RHIR
B4	R/W	Receive HDLC FIFO Register	RHFR

ADDRESS	R/W	REGISTER NAME	REGISTER ABBREVIATION
B5	R/W	Interleave Bus Operation Register	IBO
B6	R/W	Transmit HDLC Information Register	THIR
B7	R/W	Transmit HDLC FIFO Register	THFR
B8	R/W	Receive HDLC DS0 Control Register 1	RDC1
B9	R/W	Receive HDLC DS0 Control Register 2	RDC2
BA	R/W	Transmit HDLC DS0 Control Register 1	TDC1
BB	R/W	Transmit HDLC DS0 Control Register 2	TDC2
BC	–	Not used	(set to 00H)
BD	–	Not used	(set to 00H)
BE	–	Not used	(set to 00H)
BF	–	Not used	(set to 00H)

NOTES:

1. Test Registers 1, 2, and 3 are used only by the factory; these registers must be cleared (set to all zeros) on power– up initialization to insure proper operation.
2. Register banks CxH, DxH, ExH, and FxH are not accessible.

4. PARALLEL PORT

The DS21FT40 is controlled via either a non–multiplexed (MUX = 0) or a multiplexed (MUX = 1) bus by an external microcontroller or microprocessor. The DS21FT40 can operate with either Intel or Motorola bus timing configurations. If the BTS pin is tied low, Intel timing will be selected; if tied high, Motorola timing will be selected. All Motorola bus signals are listed in parenthesis (). See the timing diagrams in the A.C. Electrical Characteristics in Section 17 for more details.

5. CONTROL, ID AND TEST REGISTERS

The operation of each framer within the DS21FT40 is configured via a set of ten control registers. Typically, the control registers are only accessed when the system is first powered up. Once a channel in the DS21FT40 has been initialized, the control registers will only need to be accessed when there is a change in the system configuration. There are two Receive Control Register (RCR1 and RCR2), two Transmit Control Registers (TCR1 and TCR2), and six Common Control Registers (CCR1 to CCR6). Each of the ten registers are described in this section.

There is a device Identification Register (IDR) at address 0Fh. The MSB of this read–only register is fixed to a one indicating that the DS21Q44 die is present. The lower 4 bits of the IDR are used to display the die revision of the chip.

Power–Up Sequence

The DS21FT40 does not automatically clear its register space on power–up. After the supplies are stable, each of the four framer's register space should be configured for operation by writing to all of the internal registers. This includes setting the Test and all unused registers to 00Hex.

This can be accomplished using a two-pass approach on each quad framer within the DS21FT40.

1. Clear each quad framer's register space by writing 00H to addresses 00H through 0BFH.
2. Program required registers to achieve desired operating mode.

Finally, after the TSYSCLK and RSYSCLK inputs are stable, the ESR bit should be toggled from a zero to a one (this step can be skipped if the elastic stores are disabled).

IDR: DEVICE IDENTIFICATION REGISTER (Address=0F Hex)

(MSB) (LSB)

T1E1	0	0	0	ID3	ID2	ID1	ID0

SYMBOLS	POSITION	NAME AND DESCRIPTION
T1E1	IDR.7	T1 or E1 Chip Determination Bit. 0=T1 chip 1=E1 chip
ID3	IDR.3	Chip Revision Bit 3. MSB of a decimal code that represents the chip revision.
ID2	IDR.1	Chip Revision Bit 2.
ID1	IDR.2	Chip Revision Bit 1.
ID0	IDR.0	Chip Revision Bit 0. LSB of a decimal code that represents the chip revision.

RCR1: RECEIVE CONTROL REGISTER 1 (Address=10 Hex)

(MSB) (LSB)

RSMF	RSM	RSIO	–	–	FRC	SYNCE	RESYNC

SYMBOLS	POSITION	NAME AND DESCRIPTION
RSMF	RCR1.7	RSYNC Multiframe Function. Only used if the RSYNC pin is programmed in the multiframe mode (RCR1.6=1). 0 = RSYNC outputs CAS multiframe boundaries 1 = RSYNC outputs CRC4 multiframe boundaries
RSM	RCR1.6	RSYNC Mode Select. 0 = frame mode (see the timing in Section 18) 1 = multiframe mode (see the timing in Section 18)
RSIO	RCR1.5	RSYNC I/O Select. (note: this bit must be set to zero when RCR2.1=0). 0 = RSYNC is an output (depends on RCR1.6) 1 = RSYNC is an input (only valid if elastic store enabled)
–	RCR1.4	Not Assigned. Should be set to zero when written.
–	RCR1.3	Not Assigned. Should be set to zero when written.

SYMBOLS	POSITION	NAME AND DESCRIPTION
FRC	RCR1.2	Frame Resync Criteria. 0 = resync if FAS received in error 3 consecutive times 1 = resync if FAS or bit 2 of non–FAS is received in error 3 consecutive times
SYNCE	RCR1.1	Sync Enable. 0 = auto resync enabled 1 = auto resync disabled
RESYNC	RCR1.0	Resync. When toggled from low to high, a resync is initiated. Must be cleared and set again for a subsequent resync.

SYNC/RESYNC CRITERIA Table 5–1

FRAME OR MULTIFRAME LEVEL	SYNC CRITERIA	RESYNC CRITERIA	ITU SPEC.
FAS	FAS present in frame N and N + 2, and FAS not present in frame N + 1	Three consecutive incorrect FAS received Alternate (RCR1.2=1) the above criteria is met or three consecutive incorrect bit 2 of non–FAS received	G.706 4.1.1 4.1.2
CRC4	Two valid MF alignment words found within 8 ms	915 or more CRC4 code words out of 1000 received in error	G.706 4.2 and 4.3.2
CAS	Valid MF alignment word found and previous timeslot 16 contains code other than all zeros	Two consecutive MF alignment words received in error	G.732 5.2

RCR2: RECEIVE CONTROL REGISTER 2 (Address=11 Hex)

(MSB) (LSB)

Sa8S	Sa7S	Sa6S	Sa5S	Sa4S	RBCS	RESE	–

SYMBOLS	POSITION	NAME AND DESCRIPTION
Sa8S	RCR2.7	Sa8 Bit Select. Not applicable for DS21FT40.
Sa7S	RCR2.6	Sa7 Bit Select. Not applicable for DS21FT40.
Sa6S	RCR2.5	Sa6 Bit Select. Not applicable for DS21FT40.
Sa5S	RCR2.4	Sa5 Bit Select. Not applicable for DS21FT40.
Sa4S	RCR2.3	Sa4 Bit Select. Not applicable for DS21FT40.

SYMBOLS	POSITION	NAME AND DESCRIPTION
RBCS	RCR2.2	Receive Side Backplane Clock Select. 0 = if RSYSCLK is 1.544 MHz 1 = if RSYSCLK is 2.048 MHz
RESE	RCR2.1	Receive Side Elastic Store Enable. 0 = elastic store is bypassed 1 = elastic store is enabled
–	RCR2.0	Not Assigned. Should be set to zero when written.

TCR1: TRANSMIT CONTROL REGISTER 1 (Address=12 Hex)

(MSB)							(LSB)
ODF	TFPT	T16S	TUA1	TSiS	TSA1	TSM	TSIO

SYMBOLS	POSITION	NAME AND DESCRIPTION
ODF	TCR1.7	Output Data Format. 0 = bipolar data at TPOS and TNEG 1 = NRZ data at TPOS; TNEG=0
TFPT	TCR1.6	Transmit Timeslot 0 Pass Through. 0 = FAS bits/Sa bits/Remote Alarm sourced internally from the TAF and TNAF registers 1 = FAS bits/Sa bits/Remote Alarm sourced from TSER
T16S	TCR1.5	Transmit Timeslot 16 Data Select. 0 = sample timeslot 16 at TSER pin 1 = source timeslot 16 from TS0 to TS15 registers
TUA1	TCR1.4	Transmit Unframed All Ones. 0 = transmit data normally 1 = transmit an unframed all one's code at TPOS and TNEG
TSiS	TCR1.3	Transmit International Bit Select. 0 = sample Si bits at TSER pin 1 = source Si bits from TAF and TNAF registers (in this mode, TCR1.6 must be set to 0)
TSA1	TCR1.2	Transmit Signaling All Ones. 0 = normal operation 1 = force timeslot 16 in every frame to all ones
TSM	CR1.1	TSYNC Mode Select. 0 = frame mode (see the timing in Section 16) 1 = CAS and CRC4 multiframe mode (see the timing in Section 16)
TSIO	TCR1.0	TSYNC I/O Select. 0 = TSYNC is an input 1 = TSYNC is an output

NOTE:

See Figure 16–15 for more details about how the Transmit Control Registers affect the operation of the DS21FT40.

TCR2: TRANSMIT CONTROL REGISTER 2 (Address=13 Hex)

(MSB)							(LSB)
Sa8S	Sa7S	Sa6S	Sa5S	Sa4S	ODM	AEBE	PF

SYMBOLS	POSITION	NAME AND DESCRIPTION
Sa8S	TCR2.7	Sa8 Bit Select. Not applicable for DS21FT40.
Sa7S	TCR2.6	Sa7 Bit Select. Not applicable for DS21FT40.
Sa6S	TCR2.5	Sa6 Bit Select. Not applicable for DS21FT40.
Sa5S	TCR2.4	Sa5 Bit Select. Not applicable for DS21FT40.
Sa4S	TCR2.3	Sa4 Bit Select. Not applicable for DS21FT40.
ODM	TCR2.2	Output Data Mode. 0 = pulses at TPOSO and TNEGO are one full TCLKO period wide 1 = pulses at TPOSO and TNEGO are 1/2 TCLKO period wide
AEBE	TCR2.1	Automatic E–Bit Enable. 0 = E–bits not automatically set in the transmit direction 1 = E–bits automatically set in the transmit direction
PF	TCR2.0	Function of RLOS/LOTC Pin. Not applicable for DS21FT40. Should be cleared to zero.

CCR1: COMMON CONTROL REGISTER 1 (Address=14 Hex)

(MSB)							(LSB)
FLB	THDB3	TG802	TCRC4	RSM	RHDB3	RG802	RCRC4

SYMBOLS	POSITION	NAME AND DESCRIPTION
FLB	CCR1.7	Framer Loopback. 0=loopback disabled 1=loopback enabled
THDB3	CCR1.6	Transmit HDB3 Enable. 0=HDB3 disabled 1=HDB3 enabled
TG802	CCR1.5	Transmit G.802 Enable. See Section 16 for details. Not applicable for DS21FT40. Should be cleared to zero.
TCRC4	CCR1.4	Transmit CRC4 Enable. 0=CRC4 disabled 1=CRC4 enabled
RSM	CCR1.3	Receive Signaling Mode Select. 0=CAS signaling mode 1=CCS signaling mode
RHDB3	CCR1.2	Receive HDB3 Enable. 0=HDB3 disabled 1=HDB3 enabled

SYMBOLS	POSITION	NAME AND DESCRIPTION
RG802	CCR1.1	Receive G.802 Enable. See Section 16 for details. Not applicable for DS21FT40. Should be cleared to zero.
RCRC4	CCR1.0	Receive CRC4 Enable. 0=CRC4 disabled 1=CRC4 enabled

FRAMER LOOPBACK

When CCR1.7 is set to a one, the framer will enter a Framer LoopBack (FLB) mode. See Figure 1–2 for more details. This loopback is useful in testing and debugging applications. In FLB, the framer will loop data from the transmit side back to the receive side. When FLB is enabled, the following will occur:

1. Data will be transmitted as normal at TPOS and TNEG.
2. Data input via RPOS and RNEG will be ignored.
3. The RCLK output will be replaced with the TCLK input.

CCR2: COMMON CONTROL REGISTER 2 (Address=1A Hex)

(MSB)							(LSB)
ECUS	VCRFS	AAIS	ARA	RSERC	LOTCMC	RFF	RFE

SYMBOLS	POSITION	NAME AND DESCRIPTION
ECUS	CCR2.7	Error Counter Update Select. See Section 7 for details. 0=update error counters once a second 1=update error counters every 62.5 ms (500 frames)
VCRFS	CCR2.6	VCR Function Select. See Section 7 for details. 0=count BiPolar Violations (BPVs) 1=count Code Violations (CVs)
AAIS	CCR2.5	Automatic AIS Generation. 0=disabled 1=enabled
ARA	CCR2.4	Automatic Remote Alarm Generation. 0=disabled 1=enabled
RSERC	CCR2.3	RSER Control. 0=allow RSER to output data as received under all conditions 1=force RSER to one under loss of frame alignment conditions
LOTCMC	CCR2.2	Loss of Transmit Clock Mux Control. Determines whether the transmit side formatter should switch to the ever present RCLK if the TCLK should fail to transition (see Figure 1–2). 0=do not switch to RCLK if TCLK stops 1=switch to RCLK if TCLK stops
RFF	CCR2.1	Receive Force Freeze. Freezes receive side signaling at RSER (if CCR3.3=1); will override Receive Freeze Enable (RFE). See Section 9 for details. 0=do not force a freeze event 1=force a freeze event

SYMBOLS	POSITION	NAME AND DESCRIPTION
RFE	CCR2.0	Receive Freeze Enable. See Section 9 for details. 0=no freezing of receive signaling data will occur 1=allow freezing of receive signaling data at RSER (if CCR3.3=1).

AUTOMATIC ALARM GENERATION

The DS21FT40 can be programmed to automatically transmit AIS or Remote Alarm. When automatic AIS generation is enabled (CCR2.5 = 1), the framer monitors the receive side to determine if any of the following conditions are present: loss of receive frame synchronization, AIS alarm (all one's) reception, or loss of receive carrier (or signal). If any one (or more) of the above conditions is present, then the framer will transmit an AIS alarm.

When automatic RAI generation is enabled (CCR2.4 = 1), the framer monitors the receive side to determine if any of the following conditions are present: loss of receive frame synchronization, AIS alarm (all one's) reception, loss of receive carrier or if CRC4 multiframe synchronization (if enabled) cannot be found within 128 ms of FAS synchronization. If any one (or more) of the above conditions is present, then the framer will transmit a RAI alarm. RAI generation conforms to ETS 300 011 specifications and a constant Remote Alarm will be transmitted if the framer cannot find CRC4 multiframe synchronization within 400 ms as per G.706.

It is an illegal state to have both CCR2.4 and CCR2.5 set to one at the same time.

CCR3: COMMON CONTROL REGISTER 3 (Address=1B Hex)

(MSB)							(LSB)
TESE	TCBFS	TIRFS	–	RSRE	THSE	TBCS	RCLA

SYMBOLS	POSITION	NAME AND DESCRIPTION
TESE	CCR3.7	Transmit Side Elastic Store Enable. 0=elastic store is bypassed 1=elastic store is enabled
TCBFS	CCR3.6	Transmit Channel Blocking Registers (TCBR) Function Select. 0=TCBRs define the operation of the TCHBLK output pin (not applicable for DS21FT40) 1=TCBRs define which signaling bits are to be inserted
TIRFS	CCR3.5	Transmit Idle Registers (TIR) Function Select. See Section 10 for details. 0=TIRs define in which channels to insert idle code 1=TIRs define in which channels to insert data from RSER (i.e., Per Channel Loopback function)
–	CCR3.4	Not Assigned. Should be set to zero when written.

SYMBOLS	POSITION	NAME AND DESCRIPTION
RSRE	CCR3.3	Receive Side Signaling Re–Insertion Enable. See Section 9 for details. 0=do not re–insert signaling bits into the data stream presented at the RSER pin 1=re–insert the signaling bits into data stream presented at the RSER pin
THSE	CCR3.2	Transmit Side Hardware Signaling Insertion Enable. Not applicable for DS21FT40. Should be cleared to zero.
TBCS	CCR3.1	Transmit Side Backplane Clock Select. 0=if TSYSCLK is 1.544 MHz 1=if TSYSCLK is 2.048 MHz
RCLA	CCR3.0	Receive Carrier Loss (RCL) Alternate Criteria. 0=RCL declared upon 255 consecutive zeros (125 us) 1=RCL declared upon 2048 consecutive zeros (1 ms)

CCR4: COMMON CONTROL REGISTER 4 (Address=A8 Hex)

(MSB) (LSB)

RLB	–	–	TCM4	TCM3	TCM2	TCM1	TCM0

SYMBOLS	POSITION	NAME AND DESCRIPTION
RLB	CCR4.7	Remote Loopback. 0 = loopback disabled 1 = loopback enabled
–	CCR4.6	Not Assigned. Should be set to zero when written.
–	CCR4.5	Not Assigned. Should be set to zero when written.
TCM4	CCR4.4	Transmit Channel Monitor Bit 4. MSB of a channel decode that deter-mines which transmit channel data will appear in the TDS0M register. See Section 8 for details.
TCM3	CCR4.3	Transmit Channel Monitor Bit 3.
TCM2	CCR4.2	Transmit Channel Monitor Bit 2.
TCM1	CCR4.1	Transmit Channel Monitor Bit 1.
TCM0	CCR4.0	Transmit Channel Monitor Bit 0. LSB of the channel decode.

CCR5: COMMON CONTROL REGISTER 5 (Address = AA Hex)

(MSB)							(LSB)
–	RESALGN	TESALGN	RCM4	RCM3	RCM2	RCM1	RCM0

SYMBOLS	POSITION	NAME AND DESCRIPTION
–	CCR5.7	Not Assigned. Should be set to zero when written
RESALGN	CCR5.6	Receive Elastic Store Align. Setting this bit from a zero to a one may force the receive elastic store's write/read pointers to a minimum separation of half a frame. No action will be taken if the pointer separation is already greater or equal to half a frame. If pointer separation is less then half a frame, the command will be executed and data will be disrupted. Should be toggled after RSYSCLK has been applied and is stable. Must be cleared and set again for a subsequent align. See Section 12 for details.
TESALGN	CCR5.5	Transmit Elastic Store Align. Setting this bit from a zero to a one may force the transmit elastic store's write/read pointers to a minimum separation of half a frame. No action will be taken if the pointer separation is already greater or equal to half a frame. If pointer separation is less then half a frame, the command will be executed and data will be disrupted. Should be toggled after TSYSCLK has been applied and is stable. Must be cleared and set again for a subsequent align. See Section 12 for details.
RCM4	CCR5.4	Receive Channel Monitor Bit 4. MSB of a channel decode that determines which receive channel data will appear in the RDS0M register. See Section 8 for details.
RCM3	CCR5.3	Receive Channel Monitor Bit 3.
RCM2	CCR5.2	Receive Channel Monitor Bit 2.
RCM1	CCR5.1	Receive Channel Monitor Bit 1.
RCM0	CCR5.0	Receive Channel Monitor Bit 0. LSB of the channel decode.

CCR6: COMMON CONTROL REGISTER 6 (Address=1D Hex)

(MSB)							(LSB)
–	–	–	–	–	TCLKSRC	RESR	TESR

SYMBOLS	POSITION	NAME AND DESCRIPTION
–	CCR6.7	Not Assigned. Should be set to zero when written
–	CCR6.6	Not Assigned. Should be set to zero when written
–	CCR6.5	Not Assigned. Should be set to zero when written
–	CCR6.4	Not Assigned. Should be set to zero when written
–	CCR6.3	Not Assigned. Should be set to zero when written

SYMBOLS	POSITION	NAME AND DESCRIPTION
TCLKSRC	CCR6.2	Transmit Clock Source Select. This function allows the user to internally select RCLK as the clock source for the transmit side formatter. 0 = Transmit side formatter clocked with signal applied at TCLK pin. LOTC Mux function is operational (TCR1.7) 1 = Transmit side formatter clocked with RCLK.
RESR	CCR6.1	Receive Elastic Store Reset. Setting this bit from a zero to a one will force the receive elastic store to a depth of one frame. Receive data is lost during the reset. Should be toggled after RSYSCLK has been applied and is stable. Do not leave this bit set high.
TESR	CCR6.0	Transmit Elastic Store Reset. Setting this bit from a zero to a one will force the transmit elastic store to a depth of one frame. Transmit data is lost during the reset. Should be toggled after TSYSCLK has been applied and is stable. Do not leave this bit set high.

6. STATUS AND INFORMATION REGISTERS

There is a set of seven registers per framer that contain information on the current real time status of a framer in the DS21FT40, Status Register 1 (SR1), Status Register 2 (SR2), Receive Information Register (RIR), Synchronizer status Register (SSR) and a set of three registers for the onboard HDLC controller. The specific details on the four registers pertaining to the HDLC controller are covered in Section 14 but they operate the same as the other status registers in the DS21FT40 and this operation is described below.

When a particular event has occurred (or is occurring), the appropriate bit in one of these four registers will be set to a one. All of the bits in SR1, SR2, and RIR1 registers operate in a latched fashion. The Synchronizer status Register contents are not latched. This means that if an event or an alarm occurs and a bit is set to a one in any of the registers, it will remain set until the user reads that bit. The bit will be cleared when it is read and it will not be set again until the event has occurred again (or in the case of the RSA1, RSA0, RDMA, RUA1, RRA, RCL, and RLOS alarms, the bit will remain set if the alarm is still present).

The user will always precede a read of any of the SR1, SR2 and RIR registers with a write. The byte written to the register will inform the framer which bits the user wishes to read and have cleared. The user will write a byte to one of these registers, with a one in the bit positions he or she wishes to read and a zero in the bit positions he or she does not wish to obtain the latest information on. When a one is written to a bit location, the read register will be updated with the latest information. When a zero is written to a bit position, the read register will not be updated and the previous value will be held. A write to the status and information registers will be immediately followed by a read of the same register. The read result should be logically AND'ed with the mask byte that was just written and this value should be written back into the same register to insure that bit does indeed clear. This second write step is necessary because the alarms and events in the status registers occur asynchronously in respect to their access via the parallel port. This write–read– write scheme allows an external microcontroller or microprocessor to individually poll certain bits without disturbing the other bits in the register. This operation is key in controlling the DS21FT40 with higher–order software languages.

The SSR register operates differently than the other three. It is a read only register and it reports the status of the synchronizer in real time. This register is not latched and it is not necessary to precede a read of this register with a write.

The SR1, SR2, and HSR registers have the unique ability to initiate a hardware interrupt via the INT* output pin. Each of the alarms and events in the SR1, SR2, and HSR can be either masked or unmasked from the interrupt pin via the Interrupt Mask Register 1 (IMR1), Interrupt Mask Register 2 (IMR2), and HDLC Interrupt Mask Register (HIMR) respectively. The HIMR register is covered in Section 14.

The interrupts caused by four of the alarms in SR1 (namely RUA1, RRA, RCL, and RLOS) act differently than the interrupts caused by other alarms and events in SR1 and SR2 (namely RSA1, RDMA, RSA0, RSLIP, RMF, RAF, TMF, SEC, TAF, LOTC, RCMF, and TSLIP). These four alarm interrupts will force the INT* pin low whenever the alarm changes state (i.e., the alarm goes active or inactive according to the set/clear criteria in Table 6-1). The INT* pin will be allowed to return high (if no other interrupts are present) when the user reads the alarm bit that caused the interrupt to occur. If the alarm is still present, the register bit will remain set.

The event caused interrupts will force the INT* pin low when the event occurs. The INT* pin will be allowed to return high (if no other interrupts are present) when the user reads the event bit that caused the interrupt to occur.

ISR: INTERRUPT STATUS REGISTER
(Any address from 0C0 Hex to 0FF Hex)

(MSB)							(LSB)
F3HDLC	F3SR	F2HDLC	F2SR	F1HDLC	F1SR	F0HDLC	F0SR

SYMBOLS	POSITION	NAME AND DESCRIPTION
F3HDLC	ISR.7	FRAMER 3 HDLC CONTROLLER INTERRUPT REQUEST. 0 = No interrupt request pending. 1 = Interrupt request pending.
F3SR	ISR.6	FRAMER 3 SR1 or SR2 INTERRUPT REQUEST. 0 = No interrupt request pending. 1 = Interrupt request pending.
F2HDLC	ISR.5	FRAMER 2 HDLC CONTROLLER INTERRUPT REQUEST. 0 = No interrupt request pending. 1 = Interrupt request pending.
F2SR	ISR.4	FRAMER 2 SR1 or SR2 INTERRUPT REQUEST. 0 = No interrupt request pending. 1 = Interrupt request pending.
F1HDLC	ISR.3	FRAMER 1 HDLC CONTROLLER INTERRUPT REQUEST. 0 = No interrupt request pending. 1 = Interrupt request pending.
F1SR	ISR.2	FRAMER 1 SR1 or SR2 INTERRUPT REQUEST. 0 = No interrupt request pending. 1 = Interrupt request pending.
F0HDLC	ISR.1	FRAMER 0 HDLC CONTROLLER INTERRUPT REQUEST. 0 = No interrupt request pending.

SYMBOLS	POSITION	NAME AND DESCRIPTION
		1 = Interrupt request pending.
F0SR	ISR.0	FRAMER 0 SR1 or SR2 INTERRUPT REQUEST. 0 = No interrupt request pending. 1 = Interrupt request pending.

RIR: RECEIVE INFORMATION REGISTER (Address=08 Hex)

(MSB)							(LSB)
TESF	TESE	–	RESF	RESE	CRCRC	FASRC	CASRC

SYMBOLS	POSITION	NAME AND DESCRIPTION
TESF	RIR.7	Transmit Side Elastic Store Full. Set when the transmit side elastic store buffer fills and a frame is deleted.
TESE	RIR.6	Transmit Side Elastic Store Empty. Set when the transmit side elastic store buffer empties and a frame is repeated.
–	RIR.5	Not Assigned. Could be any value.
RESF	RIR.4	Receive Side Elastic Store Full. Set when the receive side elastic store buffer fills and a frame is deleted.
RESE	RIR.3	Receive Side Elastic Store Empty. Set when the receive side elastic store buffer empties and a frame is repeated.
CRCRC	RIR.2	CRC Resync Criteria Met. Set when 915/1000 code words are received in error.
FASRC	RIR.1	FAS Resync Criteria Met. Set when 3 consecutive FAS words are received in error.
CASRC	RIR.0	CAS Resync Criteria Met. Set when 2 consecutive CAS MF alignment words are received in error.

SSR: SYNCHRONIZER STATUS REGISTER (Address=1E Hex)

(MSB)							(LSB)
CSC5	CSC4	CSC3	CSC2	CSC0	FASSA	CASSA	CRC4SA

SYMBOLS	POSITION	NAME AND DESCRIPTION
CSC5	SSR.7	CRC4 Sync Counter Bit 5. MSB of the 6–bit counter.
CSC4	SSR.6	CRC4 Sync Counter Bit 4.
CSC3	SSR.5	CRC4 Sync Counter Bit 3.
CSC2	SSR.4	CRC4 Sync Counter Bit 2.
CSC0	SSR.3	CRC4 Sync Counter Bit 0. LSB of the 6–bit counter. The next to LSB is not accessible.
FASSA	SSR.2	FAS Sync Active. Set while the synchronizer is searching for alignment at the FAS level.
CASSA	SSR.1	CAS MF Sync Active. Set while the synchronizer is searching for the CAS MF alignment word.
CRC4SA	SSR.0	CRC4 MF Sync Active. Set while the synchronizer is searching for the CRC4 MF alignment word.

CRC4 SYNC COUNTER

The CRC4 Sync Counter increments each time the 8 ms CRC4 multiframe search times out. The counter is cleared when the framer has successfully obtained synchronization at the CRC4 level. The counter can also be cleared by disabling the CRC4 mode (CCR1.0=0). This counter is useful for determining the amount of time the framer has been searching for synchronization at the CRC4 level. ITU G.706 suggests that if synchronization at the CRC4 level cannot be obtained within 400 ms, then the search should be abandoned and proper action taken. The CRC4 Sync Counter will rollover.

SR1: STATUS REGISTER 1 (Address=06 Hex)

(MSB)							(LSB)
RSA1	RDMA	RSA0	RSLIP	RUA1	RRA	RCL	RLOS

SYMBOLS	POSITION	NAME AND DESCRIPTION
RSA1	SR1.7	Receive Signaling All Ones / Signaling Change. Set when over a full MF, the content of timeslot 16 contains less than three zeros. This alarm is not disabled in the CCS signaling mode. A change in the contents of RS1 through RS16 from one multiframe to the next will cause RSA1 and RSA0 to be set.
RDMA	SR1.6	Receive Distant MF Alarm. Set when bit–6 of timeslot 16 in frame 0 has been set for two consecutive multiframes. This alarm is not disabled in the CCS signaling mode.
RSA0	SR1.5	Receive Signaling All Zeros / Signaling Change. Set when over a full MF, timeslot 16 contains all zeros. A change in the contents of RS1 through RS16 from one multiframe to the next will cause RSA1 and RSA0 to be set.
RSLIP	SR1.4	Receive Side Elastic Store Slip. Set when the elastic store has either repeated or deleted a frame of data.
RUA1	SR1.3	Receive Unframed All Ones. Set when an unframed all ones code is received at RPOS and RNEG.
RRA	SR1.2	Receive Remote Alarm. Set when a remote alarm is received at RPOS and RNEG.
RCL	SR1.1	Receive Carrier Loss. Set when 255 (or 2048 if CCR3.0=1) consecutive zeros have been detected at RPOS and RNEG.
RLOS	SR1.0	Receive Loss of Sync. Set when the device is not synchronized to the receive E1 stream.

ALARM CRITERIA Table 6-1

ALARM	SET CRITERIA	CLEAR CRITERIA	ITU SPEC.
RSA1 (receive signaling all ones)	over 16 consecutive frames (one full MF) timeslot 16 contains less than three zeros	over 16 consecutive frames (one full MF) timeslot 16 contains three or more zeros	G.732 4.2
RSA0 (receive signaling all zeros)	over 16 consecutive frames (one full MF) timeslot 16 contains all zeros	over 16 consecutive frames (one full MF) timeslot 16 contains at least a single one	G.732 5.2
RDMA (receive distant multiframe alarm)	bit 6 in timeslot 16 of frame 0 set to one for two consecutive MF	bit 6 in timeslot 16 of frame 0 set to zero for two consecutive MF	O.162 2.1.5
RUA1 (receive unframed all ones)	less than three zeros in two frames (512 bits)	more than two zeros in two frames (512 bits)	O.162 1.6.1.2
RRA (receive remote alarm)	bit 3 of non–align frame set to one for three consecutive occasions	bit 3 of non–align frame set to zero for three consecutive occasions	O.162 2.1.4
RCL (receive carrier loss)	255 (or 2048) consecutive zeros received	in 255 bit times, at least 32 ones are received	G.775 / G.962

SR2: STATUS REGISTER 2 (Address=07 Hex)

(MSB) (LSB)

RMF	RAF	TMF	SEC	TAF	LOTC	RCMF	TSLIP

SYMBOLS	POSITION	NAME AND DESCRIPTION
RMF	SR2.7	Receive CAS Multiframe. Set every 2 ms (regardless if CAS signaling is enabled or not) on receive multiframe boundaries. Used to alert the host that signaling data is available.
RAF	SR2.6	Receive Align Frame. Set every 250 s at the beginning of align frames. Used to alert the host that Si and Sa bits are available in the RAF and RNAF registers.
TMF	SR2.5	Transmit Multiframe. Set every 2 ms (regardless if CRC4 is enabled) on transmit multiframe boundaries. Used to alert the host that signaling data needs to be updated.
SEC	SR2.4	One Second Timer. Set on increments of one second based on RCLK. If CCR2.7=1, then this bit will be set every 62.5 ms instead of once a second.
TAF	SR2.3	Transmit Align Frame. Set every 250 s at the beginning of align frames. Used to alert the host that the TAF and TNAF registers need to be updated.

SYMBOLS	POSITION	NAME AND DESCRIPTION
LOTC	SR2.2	Loss of Transmit Clock. Set when the TCLK pin has not transitioned for one channel time (or 3.9 s).
RCMF	SR2.1	Receive CRC4 Multiframe. Set on CRC4 multiframe boundaries; will continue to be set every 2 ms on an arbitrary boundary if CRC4 is disabled.
TSLIP	SR2.0	Transmit Elastic Store Slip. Set when the elastic store has either repeated or deleted a frame of data.

IMR1: INTERRUPT MASK REGISTER 1 (Address=16 Hex)

(MSB)							(LSB)
RSA1	RDMA	RSA0	RSLIP	RUA1	RRA	RCL	RLOS

SYMBOLS	POSITION	NAME AND DESCRIPTION
RSA1	IMR1.7	Receive Signaling All Ones / Signaling Change. 0=interrupt masked 1=interrupt enabled
RDMA	IMR1.6	Receive Distant MF Alarm. 0=interrupt masked 1=interrupt enabled
RSA0	IMR1.5	Receive Signaling All Zeros / Signaling Change. 0=interrupt masked 1=interrupt enabled
RSLIP	IMR1.4	Receive Elastic Store Slip Occurrence. 0=interrupt masked 1=interrupt enabled
RUA1	IMR1.3	Receive Unframed All Ones. 0=interrupt masked 1=interrupt enabled
RRA	IMR1.2	Receive Remote Alarm. 0=interrupt masked 1=interrupt enabled
RCL	IMR1.1	Receive Carrier Loss. 0=interrupt masked 1=interrupt enabled
RLOS	IMR1.0	Receive Loss of Sync. 0=interrupt masked 1=interrupt enabled

IMR2: INTERRUPT MASK REGISTER 2 (Address=17 Hex)

(MSB)							(LSB)
RMF	RAF	TMF	SEC	TAF	LOTC	RCMF	TSLIP

SYMBOLS	POSITION	NAME AND DESCRIPTION
RMF	IMR2.7	Receive CAS Multiframe. 0=interrupt masked 1=interrupt enabled
RAF	IMR2.6	Receive Align Frame. 0=interrupt masked 1=interrupt enabled
TMF	IMR2.5	Transmit Multiframe. 0=interrupt masked 1=interrupt enabled
SEC	IMR2.4	One Second Timer. 0=interrupt masked 1=interrupt enabled
TAF	IMR2.3	Transmit Align Frame. 0=interrupt masked 1=interrupt enabled
LOTC	IMR2.2	Loss Of Transmit Clock. 0=interrupt masked 1=interrupt enabled
RCMF	IMR2.1	Receive CRC4 Multiframe. 0=interrupt masked 1=interrupt enabled
TSLIP	IMR2.0	Transmit Side Elastic Store Slip Occurrence. 0=interrupt masked 1=interrupt enabled

7. ERROR COUNT REGISTERS

There are a set of four counters in each framer that record bipolar or code violations, errors in the CRC4 SMF code words, E bits as reported by the far end, and word errors in the FAS. Each of these four counters are automatically updated on either one second boundaries (CCR2.7=0) or every 62.5 ms (CCR2.7=1) as determined by the timer in Status Register 2 (SR2.4). Hence, these registers contain performance data from either the previous second or the previous 62.5 ms. The user can use the interrupt from the one second timer to determine when to read these registers. The user has a full second (or 62.5 ms) to read the counters before the data is lost. All four counters will saturate at their respective maximum counts and they will not rollover.

BPV or Code Violation Counter

Violation Count Register 1 (VCR1) is the most significant word and VCR2 is the least significant word of a 16–bit counter that records either BiPolar Violations (BPVs) or Code Violations (CVs). If CCR2.6=0, then the VCR counts bipolar violations. Bipolar violations are defined as consecutive marks of the same polarity. In this mode, if the HDB3 mode is set for the receive side via CCR1.2, then HDB3 code words are not counted as BPVs. If CCR2.6=1, then the VCR counts code violations as defined in ITU O.161. Code violations are defined as consecutive bipolar violations of the same polarity. In most applications, the framer should be programmed to count BPVs when receiving AMI code and to count CVs when receiving HDB3 code. This counter increments at all times and is not disabled by loss of sync conditions. The counter saturates at 65,535 and will not rollover. The bit error rate on a E1 line would have to be greater than 10** –2 before the VCR would saturate.

VCR1: UPPER BIPOLAR VIOLATION COUNT REGISTER 1 (Address=00 Hex)
VCR2: LOWER BIPOLAR VIOLATION COUNT REGISTER 2 (Address=01 Hex)

(MSB)							(LSB)	
V15	V14	V13	V12	V11	V10	V9	V8	VCR1
V7	V6	V5	V4	V3	V2	V1	V0	VCR2

SYMBOLS	POSITION	NAME AND DESCRIPTION
V15	VCR1.7	MSB of the 16–bit code violation count
V0	VCR2.0	LSB of the 10–bit code violation count

CRC4 Error Counter CRC4 Count Register 1 (CRCCR1) is the most significant word and CRCCR2 is the least significant word of a 10–bit counter that records word errors in the Cyclic Redundancy Check 4 (CRC4). Since the maximum CRC4 count in a one second period is 1000, this counter cannot saturate. The counter is disabled during loss of sync at either the FAS or CRC4 level; it will continue to count if loss of multiframe sync occurs at the CAS level.

CRCCR1: CRC4 COUNT REGISTER 1 (Address=02 Hex)
CRCCR2: CRC4 COUNT REGISTER 2 (Address=03 Hex)

(MSB)							(LSB)	
(note 1)	(note 1)	(note 1)	(note 1)	(note 1)	(note 1)	CRC9	CRC8	CRCCR1
CRC7	CRC6	CRC5	CRC4	CRC3	CRC2	CRC1	CRC0	CRCCR2

SYMBOLS	POSITION	NAME AND DESCRIPTION
CRC9	CRCCR1.1	MSB of the 10–Bit CRC4 error count
CRC0	CRCCR2.0	LSB of the 10–Bit CRC4 error count

NOTE:

1. The upper 6 bits of CRCCR1 at address 02 are the most significant bits of the 12–bit FAS error counter.

E–Bit Counter

E–bit Count Register 1 (EBCR1) is the most significant word and EBCR2 is the least significant word of a 10–bit counter that records Far End Block Errors (FEBE) as reported in the first bit of frames 13 and 15 on E1 lines running with CRC4 multiframe. These count registers will increment once each time the received E–bit is set to zero. Since the maximum E–bit count in a one second period is 1000, this counter cannot saturate. The counter is disabled during loss of sync at either the FAS or CRC4 level; it will continue to count if loss of multiframe sync occurs at the CAS level.

EBCR1: E–BIT COUNT REGISTER 1 (Address=04 Hex)
EBCR2: E–BIT COUNT REGISTER 2 (Address=05 Hex)

(MSB)							(LSB)	
(note 1)	(note 1)	(note 1)	(note 1)	(note 1)	(note 1)	EB9	EB8	EBCR1
EB7	EB6	EB5	EB4	EB3	EB2	EB1	EB0	EBCR2

SYMBOLS	POSITION	NAME AND DESCRIPTION
EB9	EBCR1.1	MSB of the 10–Bit E–Bit Error Count
EB0	EBCR2.0	LSB of the 10–Bit E–Bit Error Count

NOTE:
The upper 6 bits of EBCR1 at address 04 are the least significant bits of the 12–bit FAS error counter.

FAS Error Counter
FAS Count Register 1 (FASCR1) is the most significant word and FASCR2 is the least significant word of a 12–bit counter that records word errors in the Frame Alignment Signal in timeslot 0. This counter is disabled when RLOS is high. FAS errors will not be counted when the framer is searching for FAS alignment and/or synchronization at either the CAS or CRC4 multiframe level. Since the maximum FAS word error count in a one second period is 4000, this counter cannot saturate.

FASCR1: FAS ERROR COUNT REGISTER 1 (Address=02 Hex)
FASCR2: FAS ERROR COUNT REGISTER 2 (Address=04 Hex)

(MSB)							(LSB)	
FAS11	FAS10	FAS9	FAS8	FAS7	FAS6	(note 2)	(note 2)	FASCR1
FAS5	FAS4	FAS3	FAS2	FAS1	FAS0	(note 1)	(note 1)	FASCR2

SYMBOLS	POSITION	NAME AND DESCRIPTION
FAS11	FASCR1.7	MSB of the 12–Bit FAS Error Count
FAS0	FASCR2.2	LSB of the 12–Bit FAS Error Count

NOTES:
1. The lower 2 bits of FASCR1 at address 02 are the most significant bits of the 10–bit CRC4 error counter.
2. The lower 2 bits of FASCR2 at address 04 are the most significant bits of the 10–bit E–Bit counter.

8. DS0 MONITORING FUNCTION
Each framer in the DS21FT40 has the ability to monitor one DS0 64Kbps channel in the transmit direction and one DS0 channel in the receive direction at the same time. In the transmit direction the user will determine which channel is to be monitored by properly setting the TCM0 to TCM4 bits in the CCR4 register. In the receive direction, the RCM0 to RCM4 bits in the CCR5 register need to be properly set. The DS0 channel pointed to by the TCM0 to TCM4 bits will appear in the Transmit DS0 Monitor (TDS0M) register and the DS0 channel pointed to by the RCM0 to RCM4 bits will appear in the Receive DS0 (RDS0M) register. The TCM4 to TCM0 and RCM4 to RCM0 bits should be programmed with the decimal decode of the appropriate E1 channel. For example, if DS0 channel 6 (timeslot 5) in the transmit

direction and DS0 channel 15 (timeslot 14) in the receive direction needed to be monitored, then the following values would be programmed into CCR4 and CCR5:

TCM4 = 0 RCM4 = 0
TCM3 = 0 RCM3 = 1
TCM2 = 1 RCM2 = 1
TCM1 = 0 RCM1 = 1
TCM0 = 1 RCM0 = 0

CCR4: COMMON CONTROL REGISTER 4 (Address=A8 Hex)

[Repeated here from section 5 for convenience]

(MSB) (LSB)

RLB	–	–	TCM4	TCM3	TCM2	TCM1	TCM0

SYMBOLS	POSITION	NAME AND DESCRIPTION
RLB	CCR4.7	Remote Loopback. 0 = loopback disabled 1 = loopback enabled
–	CCR4.6	Not Assigned. Should be set to zero when written.
–	CCR4.5	Not Assigned. Should be set to zero when written.
TCM4	CCR4.4	Transmit Channel Monitor Bit 4. MSB of a channel decode that deter-mines which transmit channel data will appear in the TDS0M register. See Section 8 or details.
TCM3	CCR4.3	Transmit Channel Monitor Bit 3.
TCM2	CCR4.2	Transmit Channel Monitor Bit 2.
TCM1	CCR4.1	Transmit Channel Monitor Bit 1.
TCM0	CCR4.0	Transmit Channel Monitor Bit 0. LSB of the channel decode.

TDS0M: TRANSMIT DS0 MONITOR REGISTER (Address=A9 Hex)

(MSB) (LSB)

B1	B2	B3	B4	B5	B6	B7	B8

SYMBOLS	POSITION	NAME AND DESCRIPTION
B1	TDS0M.7	Transmit DS0 Channel Bit 1. MSB of the DS0 channel (first bit to be transmitted).
B2	TDS0M.6	Transmit DS0 Channel Bit 2.
B3	TDS0M.5	Transmit DS0 Channel Bit 3.
B4	TDS0M.4	Transmit DS0 Channel Bit 4.
B5	TDS0M.3	Transmit DS0 Channel Bit 5.
B6	TDS0M.2	Transmit DS0 Channel Bit 6.
B7	TDS0M.1	Transmit DS0 Channel Bit 7.
B8	TDS0M.0	Transmit DS0 Channel Bit 8. LSB of the DS0 channel (last bit to be transmitted).

CCR5: COMMON CONTROL REGISTER 5 (Address=AA Hex)

[Repeated here from section 5 for convenience]

(MSB)							(LSB)
–	RESALGN	TESALGN	RCM4	RCM3	RCM2	RCM1	RCM0

SYMBOLS	POSITION	NAME AND DESCRIPTION
–	CCR5.7	Not Assigned. Should be set to zero when written
RESALGN	CCR5.6	Receive Elastic Store Align. Setting this bit from a zero to a one may force the receive elastic store's write/read pointers to a minimum separation of half a frame. No action will be taken if the pointer separation is already greater or equal to half a frame. If pointer separation is less then half a frame, the command will be executed and data will be disrupted. Should be toggled after RSYSCLK has been applied and is stable. Must be cleared and set again for a subsequent align. See Section 12 for details.
TESALGN	CCR5.5	Transmit Elastic Store Align. Setting this bit from a zero to a one may force the transmit elastic store's write/read pointers to a minimum separation of half a frame. No action will be taken if the pointer separation is already greater or equal to half a frame. If pointer separation is less then half a frame, the command will be executed and data will be disrupted. Should be toggled after TSYSCLK has been applied and is stable. Must be cleared and set again for a subsequent align. See Section 12 for details.
RCM4	CCR5.4	Receive Channel Monitor Bit 4. MSB of a channel decode that determines which receive channel data will appear in the RDS0M register. See Section 8 for details.
RCM3	CCR5.3	Receive Channel Monitor Bit 3.
RCM2	CCR5.2	Receive Channel Monitor Bit 2.
RCM1	CCR5.1	Receive Channel Monitor Bit 1.
RCM0	CCR5.0	Receive Channel Monitor Bit 0. LSB of the channel decode.

RDS0M: RECEIVE DS0 MONITOR REGISTER (Address = AB Hex)

(MSB) (LSB)

B1	B2	B3	B4	B5	B6	B7	B8

SYMBOLS	POSITION	NAME AND DESCRIPTION
B1	RDS0M.7	Receive DS0 Channel Bit 1. MSB of the DS0 channel (first bit to be received).
B2	RDS0M.6	Receive DS0 Channel Bit 2.
B3	RDS0M.5	Receive DS0 Channel Bit 3.
B4	RDS0M.4	Receive DS0 Channel Bit 4.
B5	RDS0M.3	Receive DS0 Channel Bit 5.
B6	RDS0M.2	Receive DS0 Channel Bit 6.
B7	RDS0M.1	Receive DS0 Channel Bit 7.
B8	RDS0M.0	Receive DS0 Channel Bit 8. LSB of the DS0 channel (last bit to be received).

9. SIGNALING OPERATION

Each framer in the DS21FT40 contains provisions for both processor based (i.e., software based) signaling bit access and for hardware based access. Both the processor based access and the hardware based access can be used simultaneously if necessary. The processor based signaling is covered in Section 9.1 and the hardware based signaling is covered in Section 9.2.

9.1 PROCESSOR BASED SIGNALING

The Channel Associated Signaling (CAS) bits embedded in the E1 stream can be extracted from the receive stream and inserted into the transmit stream by the framer. Each of the 30 voice channels has four signaling bits (A/B/C/D) associated with it. The numbers in parenthesis () are the voice channel associated with a particular signaling bit. The voice channel numbers have been assigned as described in the ITU documents. Please note that this is different than the channel numbering scheme (1 to 32) that is used in the rest of the data sheet. For example, voice channel 1 is associated with timeslot 1 (Channel 2) and voice Channel 30 is associated with timeslot 31 (Channel 32). There is a set of 16 registers for the receive side (RS1 to RS16) and 16 registers on the transmit side (TS1 to TS16). The signaling registers are detailed below.

RS1 TO RS16: RECEIVE SIGNALING REGISTERS (Address=30 to 3F Hex)

(MSB) (LSB)

0	0	0	0	X	Y	X	X	RS1 (30)
A(1)	B(1)	C(1)	D(1)	A(16)	B(16)	C(16)	D(16)	RS2 (31)
A(2)	B(2)	C(2)	D(2)	A(17)	B(17)	C(17)	D(17)	RS3 (32)
A(3)	B(3)	C(3)	D(3)	A(18)	B(18)	C(18)	D(18)	RS3 (33)
A(4)	B(4)	C(4)	D(4)	A(19)	B(19)	C(19)	D(19)	RS5 (34)
A(5)	B(5)	C(5)	D(5)	A(20)	B(20)	C(20)	D(20)	RS6 (35)
A(6)	B(6)	C(6)	D(6)	A(21)	B(21)	C(21)	D(21)	RS7 (36)
A(7)	B(7)	B(7)	B(7)	B(22)	B(22)	B(22)	B(22)	RS8 (37)
A(8)	B(8)	C(8)	D(8)	A(23)	B(23)	C(23)	D(23)	RS9 (38)
A(9)	B(9)	C(9)	D(9)	A(24)	B(24)	C(24)	D(24)	RS10 (39)
A(10)	B(10)	C(10)	D(10)	A(25)	B(25)	C(25)	D(25)	RS11 (3A)
A(11)	B(11)	C(11)	D(11)	A(26)	B(26)	C(26)	D(26)	RS12 (3B)
A(12)	B(12)	C(12)	D(12)	A(27)	B(27)	C(27)	D(27)	RS13 (3C)
A(13)	B(13)	C(13)	D(13)	A(28)	B(28)	C(28)	D(28)	RS14 (3D)
A(14)	B(14)	C(14)	D(14)	A(29)	B(29)	C(29)	D(29)	RS15 (3E)
A(15)	B(15)	C(15)	D(15)	A(30)	B(30)	C(30)	D(30)	RS16 (3F)

SYMBOLS	POSITION	NAME AND DESCRIPTION
X	RS1.0/1/3	Spare Bits.
Y	RS1.2	Remote Alarm Bit (integrated and reported in SR1.6).
A(1)	RS2.7	Signaling Bit A for Channel 1
D(30)	RS16.0	Signaling Bit D for Channel 30.

Each Receive Signaling Register (RS1 to RS16) reports the incoming signaling from two timeslots. The bits in the Receive Signaling Registers are updated on multiframe boundaries so the user can utilize the Receive Multiframe Interrupt in the Receive Status Register 2 (SR2.7) to know when to retrieve the signaling bits. The user has a full 2 ms to retrieve the signaling bits before the data is lost. The RS registers are updated under all conditions. Their validity should be qualified by checking for synchronization at the CAS level. In CCS signaling mode, RS1 to RS16 can also be used to extract signaling information. Via the SR2.7 bit, the user will be informed when the signaling registers have been loaded with data. The user has 2 ms to retrieve the data before it is lost. The signaling data reported in RS1 to RS16 is also available at the RSER pin.

Three status bits in Status Register 1 (SR1) monitor the contents of registers RS1 through RS16. Status monitored includes all zeros detection, all ones detection and a change in register contents. The Receive Signaling All Zeros status bit (SR1.5) is set when over a full multi-frame, RS1 through RS16 contain all zeros. The Receive Signaling All Ones status bit (SR1.7) is set when over a full multi-frame, RS1 through RS16 contain less than three zeros. A change in the contents of RS1 through RS16 from one multiframe to the next will cause RSA1 (SR1.7) and RSA0 (SR1.5) status bits to be set at the same time.

The user can enable the INT* pin to toggle low upon detection of a change in signaling by setting either the IMR1.7 or IMR1.5 bit. Once a signaling change has been detected, the user has at least 1.75 ms to read the data out of the RS1 to RS16 registers before the data will be lost.

TS1 TO TS16: TRANSMIT SIGNALING REGISTERS (Address=40 to 4F Hex)

(MSB)							(LSB)	
0	0	0	0	X	Y	X	X	TS1 (40)
A(1)	B(1)	C(1)	D(1)	A(16)	B(16)	C(16)	D(16)	TS2 (41)
A(2)	B(2)	C(2)	D(2)	A(17)	B(17)	C(17)	D(17)	TS3 (42)
A(3)	B(3)	C(3)	D(3)	A(18)	B(18)	C(18)	D(18)	TS4 (43)
A(4)	B(4)	C(4)	D(4)	A(19)	B(19)	C(19)	D(19)	TS5 (44)
A(5)	B(5)	C(5)	D(5)	A(20)	B(20)	C(20)	D(20)	TS6 (45)
A(6)	B(6)	C(6)	D(6)	A(21)	B(21)	C(21)	D(21)	TS7 (46)
A(7)	B(7)	B(7)	B(7)	B(22)	B(22)	B(22)	B(22)	TS8 (47)
A(8)	B(8)	C(8)	D(8)	A(23)	B(23)	C(23)	D(23)	TS9 (48)
A(9)	B(9)	C(9)	D(9)	A(24)	B(24)	C(24)	D(24)	TS10 (49)
A(10)	B(10)	C(10)	D(10)	A(25)	B(25)	C(25)	D(25)	TS11 (4A)
A(11)	B(11)	C(11)	D(11)	A(26)	B(26)	C(26)	D(26)	TS12 (4B)
A(12)	B(12)	C(12)	D(12)	A(27)	B(27)	C(27)	D(27)	TS13 (4C)
A(13)	B(13)	C(13)	D(13)	A(28)	B(28)	C(28)	D(28)	TS14 (4D)
A(14)	B(14)	C(14)	D(14)	A(29)	B(29)	C(29)	D(29)	TS15 (4E)
A(15)	B(15)	C(15)	D(15)	A(30)	B(30)	C(30)	D(30)	TS16 (4F)

SYMBOLS	POSITION	NAME AND DESCRIPTION
X	TS1.0/1/3	Spare Bits.
Y	TS1.2	Remote Alarm Bit (integrated and reported in SR1.6).
A(1)	TS2.7	Signaling Bit A for Channel 1
D(30)	TS16.0	Signaling Bit D for Channel 30.

Each Transmit Signaling Register (TS1 to TS16) contains the CAS bits for two timeslots that will be inserted into the outgoing stream if enabled to do so via TCR1.5. On multiframe boundaries, the framer will load the values present in the Transmit Signaling Register into an outgoing signaling shift register that is internal to the device. The user can utilize the Transmit Multiframe bit in Status Register 2 (SR2.5) to know when to update the signaling bits. The bit will be set every 2 ms and the user has 2 ms to update the TSR’s before the old data will be retransmitted. ITU specifications recommend that the ABCD signaling not be set to all zeros because they will emulate a CAS multiframe alignment word.

The TS1 register is special because it contains the CAS multiframe alignment word in its upper nibble. The upper nibble must always be set to 0000 or else the terminal at the far end will lose multiframe synchronization. If the user wishes to transmit a multiframe alarm to the far end, then the TS1.2 bit should be set to a one. If no alarm is to be transmitted, then the TS1.2 bit should be cleared. The three remaining bits in TS1 are the spare bits. If they are not used, they should be set to one. In CCS signaling mode, TS1 to TS16 can also be used to insert signaling information. Via the SR2.5 bit, the user will be informed when the signaling registers need to be loaded with data. The user has 2 ms to load the data before the old data will be retransmitted.

Via the CCR3.6 bit, the user has the option to use the Transmit Channel Blocking Registers (TCBRs) to determine on a channel by channel basis, which signaling bits are to be inserted via the TSRs (the corresponding bit in the TCBRs=1) and which are to be sourced from the TSER pin. See the Transmit Data Flow diagram in Section 16 for more details.

TCBR1/TCBR2/TCBR3/TCBR4: DEFINITION WHEN CCR3.6=1

(MSB)							(LSB)	
CH20	CH4	CH19	CH3	CH18	CH2	CH17*	CH1*	TCBR1(22)
CH24	CH8	CH23	CH7	CH22	CH6	CH21	CH5	TCBR2(23)
CH28	CH12	CH27	CH11	CH26	CH10	CH25	CH9	TCBR3(24)
CH32	CH16	CH31	CH15	CH30	CH14	CH29	CH13	TCBR4(25)

*=CH1 and CH17 should be set to one to allow the internal TS1 register to create the CAS Multiframe Alignment Word and Spare/Remote Alarm bits.

9.2 HARDWARE BASED SIGNALING

Receive Side

Hardware signaling is supported through a mode called signaling re-insertion which is invoked by setting the RSRE control bit high (CCR3.3=1). In this mode, the user will provide a multiframe sync at the RSYNC pin and the signaling data will be re-aligned at the RSER output according to this applied multiframe boundary. In this mode, the elastic store must be enabled and the backplane clock must be 2.048 MHz.

The signaling data in the two multiframe buffer will be frozen in a known good state upon either a loss of synchronization (OOF event), carrier loss, or frame slip. To allow this freeze action to occur, the RFE control bit (CCR2.0) should be set high. The user can force a freeze by setting the RFF control bit (CCR2.1) high. Setting the RFF bit high causes the same freezing action as if a loss of synchronization, carrier loss, or slip has occurred.

The 2 multiframe buffer provides an approximate 1 multiframe delay in the signaling bits provided at the RSER pin (if RSRE=1 via CCR3.3). When freezing is enabled (RFE=1), the signaling data will be held in the last known good state until the corrupting error condition subsides. When the error condition subsides, the signaling data will be held in the old state for an additional 3 ms to 5 ms before being allowed to be updated with new signaling data.

10. PER–CHANNEL CODE GENERATION AND LOOPBACK

Each framer in the DS21FT40 can replace data on a channel–by–channel basis in both the transmit and receive directions. The transmit direction is from the backplane to the E1 line and is covered in Section 10.1. The receive direction is from the E1 line to the backplane and is covered in Section 10.2.

10.1 TRANSMIT SIDE CODE GENERATION

In the transmit direction there are two methods by which channel data from the backplane can be overwritten with data generated by the framer. The first method which is covered in Section 10.1.1 was a feature contained in the original DS21Q43 while the second method which is covered in Section 10.1.2 is a new feature of the DS21Q44.

10.1.1 Simple Idle Code Insertion and Per–Channel Loopback

The first method involves using the Transmit Idle Registers (TIR1/2/3/4) to determine which of the 32 E1 channels should be overwritten with the code placed in the Transmit Idle Definition Register (TIDR).

This method allows the same 8–bit code to be placed into any of the 32 E1 channels. If this method is used, then the CCR3.5 control bit must be set to zero.

Each of the bit position in the Transmit Idle Registers (TIR1/TIR2/TIR3/TIR4) represent a DS0 channel in the outgoing frame. When these bits are set to a one, the corresponding channel will transmit the Idle Code contained in the Transmit Idle Definition Register (TIDR).

The Transmit Idle Registers (TIRs) have an alternate function that allows them to define a Per–Channel LoopBack (PCLB). If the TIRFS control bit (CCR3.5) is set to one, then the TIRs will determine which channels (if any) from the backplane should be replaced with the data from the receive side or in other words, off of the E1 line. If this mode is enabled, then transmit and receive clocks and frame syncs must be synchronized.

TIR1/TIR2/TIR3: TRANSMIT IDLE REGISTERS (Address=26 to 29 Hex)

[Also used for Per–Channel Loopback]

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TIR1 (26)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TIR2 (27)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TIR3 (28)
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	TIR4 (29)

SYMBOLS	POSITIONS	NAME AND DESCRIPTION
CH1 - 32	TIR1.0 - 4.7	Transmit Idle Code Insertion Control Bits. 0 = do not insert the Idle Code in the TIDR into this channel 1 = insert the Idle Code in the TIDR into this channel

NOTE:

If CCR3.5=1, then a zero in the TIRs implies that channel data is to be sourced from TSER and a one implies that channel data is to be sourced from the output of the receive side framer (i.e., Per–Channel Loopback; see Figure 1–2).

TIDR: TRANSMIT IDLE DEFINITION REGISTER (Address=2A Hex)

(MSB)							(LSB)
TIDR7	TIDR6	TIDR5	TIDR4	TIDR3	TIDR2	TIDR1	TIDR0

SYMBOLS	POSITION	NAME AND DESCRIPTION
TIDR7	TIDR.7	MSB of the Idle Code (this bit is transmitted first)
TIDR0	TIDR.0	LSB of the Idle Code (this bit is transmitted last)

10.1.2 Per–Channel Code Insertion

The second method involves using the Transmit Channel Control Registers (TCC1/2/3/4) to determine which of the 32 E1 channels should be overwritten with the code placed in the Transmit Channel Registers (TC1 to TC32). This method is more flexible than the first in that it allows a different 8–bit code to be placed into each of the 32 E1 channels.

TC1 TO TC32: TRANSMIT CHANNEL REGISTERS (Address=60 to 7F Hex)

(for brevity, only channel one is shown; see Table 3-1 for other register address)

(MSB)							(LSB)	
C7	C6	C5	C4	C3	C2	C1	C0	TC1 (60)

SYMBOLS	POSITION	NAME AND DESCRIPTION
C7	TC1.7	MSB of the Code (this bit is transmitted first)
C0	TC1.0	LSB of the Code (this bit is transmitted last)

TCC1/TCC2/TCC3/TCC4: TRANSMIT CHANNEL CONTROL REGISTER (Address=A0 to A3 Hex)

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TCC1 (A0)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TCC2 (A1)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TCC3 (A2)
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	TCC4 (A3)

SYMBOLS	POSITION	NAME AND DESCRIPTION
CH1 - 32	TCC1.0 - 4.7	Transmit Code Insertion Control Bits 0 = do not insert data from the TC register into the transmit data stream 1 = insert data from the TC register into the transmit data stream

10.2 RECEIVE SIDE CODE GENERATION

On the receive side, the Receive Channel Control Registers (RCC1/2/3/4) are used to determine which of the 32 E1 channels off of the E1 line and going to the backplane should be overwritten with the code placed in the Receive Channel Registers (RC1 to RC32). This method allows a different 8–bit code to be placed into each of the 32 E1 channels.

RC1 TO RC32: RECEIVE CHANNEL REGISTERS (Address=80 to 9F Hex)

(for brevity, only channel one is shown; see Table 3-1 for other register address)

(MSB)							(LSB)	
C7	C6	C5	C4	C3	C2	C1	C0	RC1 (80)

SYMBOLS	POSITION	NAME AND DESCRIPTION
C7	RC1.7	MSB of the Code (this bit is sent first to the backplane)
C0	RC1.0	LSB of the Code (this bit is sent last to the backplane)

RCC1/RCC2/RCC3/RCC4: RECEIVE CHANNEL CONTROL REGISTER

(Address = A4 to A7 Hex)

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	RCC1 (A4)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	RCC2 (A5)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	RCC3 (A6)
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	RCC4 (A7)

SYMBOLS	POSITION	NAME AND DESCRIPTION
CH1 - 32	RCC1.0 - 4.7	Receive Code Insertion Control Bits 0 = do not insert data from the RC register into the receive data stream 1 = insert data from the RC register into the receive data stream

11. CLOCK BLOCKING REGISTERS

The Receive Channel blocking Registers (RCBR1 / RCBR2 / RCBR3 / RCBR4) and the Transmit Channel Blocking Registers (TCBR1 / TCBR2 / TCBR3 / TCBR4) control RCHBLK and TCHBLK pins on the DS21Q44 die, respectively. The RCHBLK and TCHBLK pins are not bonded out on the DS21FT40 module. However, the Transmit Channel Blocking Registers have an alternate function that is supported by the module. Via the CCR3.6 bit, the user has the option to use the TCBRs to determine on a channel by channel basis, which signaling bits are to be inserted via the TSRs and which are to be sourced from the TSER. If CCR3.6=1, then a zero in the TCBRs implies that signaling data is to be sourced from and a one implies that signaling data for that channel is to be sourced from the Transmit Signaling (TS) registers. See definition below. See the timing in Section 16 for an example. The Receive Channel Blocking Registers provide no function for the DS21FT40 and should be cleared to zero.

TCBR1/TCBR2/TCBR3/TCBR4: DEFINITION WHEN CCR3.6=1

(MSB)							(LSB)	
CH20	CH4	CH19	CH3	CH18	CH2	CH17*	CH1*	TCBR1 (22)
CH24	CH8	CH23	CH7	CH22	CH6	CH21	CH5	TCBR2 (23)
CH28	CH12	CH27	CH11	CH26	CH10	CH25	CH9	TCBR3 (24)
CH32	CH16	CH31	CH15	CH30	CH14	CH29	CH13	TCBR4 (25)

*=CH1 and CH17 should be set to one to allow the internal TS1 register to create the CAS Multiframe Alignment Word and Spare/Remote Alarm bits.

12. ELASTIC STORES OPERATION

Each framer in the DS21FT40 contains dual two–frame (512 bits) elastic stores, one for the receive direction, and one for the transmit direction. These elastic stores have two main purposes. First, they can be used to rate convert the E1 data stream to 1.544 Mbps (or a multiple of 1.544 Mbps) which is the T1 rate. Secondly, they can be used to absorb the differences in frequency and phase between the E1 data stream and an asynchronous (i.e., not frequency locked) backplane clock which can be 1.544 MHz or 2.048 MHz. The backplane clock can burst at rates up to 8.192 MHz. Both elastic stores contain full controlled slip capability which is necessary for this second purpose. Both elastic stores within a framer are fully independent and no restrictions apply to the sourcing of the various clocks that are applied to them. The transmit side elastic store can be enabled whether the receive elastic store is enabled or disabled and vice versa. Also, each elastic store can interface to either a 1.544 MHz or 2.048 MHz backplane without regard to the backplane rate the other elastic store is interfacing.

Two mechanisms are available to the user for resetting the elastic stores. The Elastic Store Reset (CCR6.0 & CCR6.1) function forces the elastic stores to a depth of one frame unconditionally. Data is lost during the reset. The second method, the Elastic Store Align (CCR5.5 & CCR5.6) forces the elastic store depth to a minimum depth of half a frame only if the current pointer separation is already less then half a frame. If a realignment occurs data is lost. In both mechanisms, independent resets are provided for both the receive and transmit elastic stores.

12.1 RECEIVE SIDE

If the receive side elastic store is enabled (RCR2.1=1), then the user must provide either a 1.544 MHz (RCR2.2 =0) or 2.048 MHz (RCR2.2=1) clock at the RSYSCLK pin. The user has the option of either providing a frame/multiframe sync at the RSYNC pin (RCR1.5=1) or having the RSYNC pin provide a pulse on frame/multiframe boundaries (RCR1.5=0). If the user wishes to obtain pulses at the frame boundary, then RCR1.6 must be set to zero and if the user wishes to have pulses occur at the multiframe boundary, then RCR1.6 must be set to one. If the elastic store is enabled, then either CAS (RCR1.7=0) or CRC4 (RCR1.7=1) multiframe boundaries will be indicated via the RMSYNC output. If the user selects to apply a 1.544 MHz clock to the RSYSCLK pin, then every fourth channel of the received E1 data will be deleted and a F–bit position (which will be forced to one) will be inserted. Hence Channels 1, 5, 9, 13, 17, 21, 25, and 29 (timeslots 0, 4, 8, 12, 16, 20, 24, and 28) will be deleted from the received E1 data stream). See Section 16 for timing details. If the 512–bit elastic buffer either fills or empties, a controlled slip will occur. If the buffer empties, then a full frame of data (256–bits) will be repeated at RSER and the SR1.4 and RIR.3 bits will be set to a one. If the buffer fills, then a full frame of data will be deleted and the SR1.4 and RIR.4 bits will be set to a one.

12.2 TRANSMIT SIDE

The operation of the transmit elastic store is very similar to the receive side. The transmit side elastic store is enabled via CCR3.7. A 1.544 MHz (CCR3.1=0) or 2.048 MHz (CCR3.1=1) clock can be applied to the TSYSCLK input. The TSYSCLK can be a bursty clock with rates up to 8.192 MHz. If the user selects to apply a 1.544 MHz clock to the TSYSCLK pin, then the data sampled at TSER will be ignored every fourth channel. Hence Channels 1, 5, 9, 13, 17, 21, 25, and 29 (timeslots 0, 4, 8, 12, 16, 20, 24, and 28) will be ignored. The user must supply a 8 kHz frame sync pulse to the TSSYNC input. See Section 16 for timing details. Controlled slips in the transmit elastic store are reported in the SR2.0 bit and the direction of the slip is reported in the RIR.6 and RIR.7 bits.

13. ADDITIONAL (Sa) AND INTERNATIONAL (Si) BIT OPERATION

Each framer in the DS21FT40 provides for access to both the Sa and the Si bits via two different methods. The first method involves using the internal RAF/RNAF and TAF/TNAF registers and is discussed in Section 13.1. The second method, which is covered in Section 13.2, involves an expanded version of the first method.

13.1 INTERNAL REGISTER SCHEME BASED ON DOUBLE–FRAME

On the receive side, the RAF and RNAF registers will always report the data as it received in the Additional and International bit locations. The RAF and RNAF registers are updated with the setting of the Receive Align Frame bit in Status Register 2 (SR2.6). The host can use the SR2.6 bit to know when to read the RAF and RNAF registers. It has 250 us to retrieve the data before it is lost.

On the transmit side, data is sampled from the TAF and TNAF registers with the setting of the Transmit Align Frame bit in Status Register 2 (SR2.3). The host can use the SR2.3 bit to know when to update the TAF and TNAF registers. It has 250 us to update the data or else the old data will be retransmitted. Data in the Si bit position will be overwritten if the framer is programmed: (1) to source the Si bits from the TSER pin, (2) in the CRC4 mode, or (3) have automatic E–bit insertion enabled. Data in the Sa bit position will be overwritten if any of the TCR2.3 to TCR2.7 bits are set to one. Please see the register descriptions for TCR1 and TCR2 and the Transmit Data Flow diagram in Section 16 for more details.

RAF: RECEIVE ALIGN FRAME REGISTER (Address=2F Hex)

(MSB) (LSB)

Si	0	0	1	1	0	1	1

SYMBOLS	POSITION	NAME AND DESCRIPTION
Si	RAF.7	International Bit.
0	RAF.6	Frame Alignment Signal Bit.
0	RAF.5	Frame Alignment Signal Bit.
1	RAF.4	Frame Alignment Signal Bit.
1	RAF.3	Frame Alignment Signal Bit.
0	RAF.2	Frame Alignment Signal Bit.
1	RAF.1	Frame Alignment Signal Bit
1	RAF.0	Frame Alignment Signal Bit.

RNAF: RECEIVE NON–ALIGN FRAME REGISTER (Address=1F Hex)

(MSB) (LSB)

Si	1	A	Sa4	Sa5	Sa6	Sa7	Sa8

SYMBOLS	POSITION	NAME AND DESCRIPTION
Si	RNAF.7	International Bit.
1	RNAF.6	Frame Non–Alignment Signal Bit.
A	RNAF.5	Remote Alarm.
Sa4	RNAF.4	Additional Bit 4.
Sa5	RNAF.3	Additional Bit 5.
Sa6	RNAF.2	Additional Bit 6.
Sa7	RNAF.1	Additional Bit 7.
Sa8	RNAF.0	Additional Bit 8.

TAF: TRANSMIT ALIGN FRAME REGISTER (Address=20 Hex)

(MSB) (LSB)

Si	0	0	1	1	0	1	1

[Must be programmed with the 7 bit FAS word; the DS21FT40 does not automatically set these bits]

SYMBOLS	POSITION	NAME AND DESCRIPTION
Si	TAF.7	International Bit.
0	TAF.6	Frame Alignment Signal Bit.
0	TAF.5	Frame Alignment Signal Bit.
1	TAF.4	Frame Alignment Signal Bit.
1	TAF.3	Frame Alignment Signal Bit.
0	TAF.2	Frame Alignment Signal Bit.
1	TAF.1	Frame Alignment Signal Bit.
1	TAF.0	Frame Alignment Signal Bit.

TNAF: TRANSMIT NON–ALIGN FRAME REGISTER (Address=21 Hex)

(MSB) (LSB)

Si	1	A	Sa4	Sa5	Sa6	Sa7	Sa8

[Bit 2 must be programmed to one; the DS21FT40 does not automatically set this bit]

SYMBOLS	POSITION	NAME AND DESCRIPTION
Si	TNAF.7	International Bit.
1	TNAF.6	Frame Non–Alignment Signal Bit.
A	TNAF.5	Remote Alarm (used to transmit the alarm).
Sa4	TNAF.4	Additional Bit 4.
Sa5	TNAF.3	Additional Bit 5.
Sa6	TNAF.2	Additional Bit 6.
Sa7	TNAF.1	Additional Bit 7.
Sa8	TNAF.0	Additional Bit 8.

13.2 INTERNAL REGISTER SCHEME BASED ON CRC4 MULTIFRAME

On the receive side, there is a set of eight registers (RSiAF, RSiNAF, RRA, RSa4 to RSa8) that report the Si and Sa bits as they are received. These registers are updated with the setting of the Receive CRC4 Multiframe bit in Status Register 2 (SR2.1). The host can use the SR2.1 bit to know when to read these registers. The user has 2 ms to retrieve the data before it is lost. The MSB of each register is the first received. Please see the register descriptions below and the Transmit Data Flow diagram in Section 16 for more details. On the transmit side, there is also a set of eight registers (TSiAF, TSiNAF, TRA, TSa4 to TSa8) that via the Transmit Sa Bit Control Register (TSaCR), can be programmed to insert both Si and Sa data. Data is sampled from these registers with the setting of the Transmit Multiframe bit in Status Register 2 (SR2.5). The host can use the SR2.5 bit to know when to update these registers. It has 2 ms to update the data or else the old data will be retransmitted. The MSB of each register is the first bit transmitted. Please see the register descriptions below and the Transmit Data Flow diagram in Section 16 for more details.

REGISTER NAME	ADDRESS (HEX)	FUNCTION
RSiAF	58	The eight Si bits in the align frame.
RSiNAF	59	The eight Si bits in the non–align frame.
RRA	5A	The eight reportings of the receive remote alarm (RA).
RSa4	5B	The eight Sa4 reported in each CRC4 multiframe.
RSa5	5C	The eight Sa5 reported in each CRC4 multiframe.
RSa6	5D	The eight Sa6 reported in each CRC4 multiframe.
RSa7	5E	The eight Sa7 reported in each CRC4 multiframe.
RSa8	5F	The eight Sa8 reported in each CRC4 multiframe.
TSiAF	50	The eight Si bits to be inserted into the align frame.
TSiNAF	51	The eight Si bits to be inserted into the non–align frame.
TRA	52	The eight settings of remote alarm (RA).
TSa4	53	The eight Sa4 settings in each CRC4 multiframe.
TSa5	54	The eight Sa5 settings in each CRC4 multiframe.
TSa6	55	The eight Sa6 settings in each CRC4 multiframe.
TSa7	56	The eight Sa7 settings in each CRC4 multiframe.
TSa8	57	The eight Sa8 settings in each CRC4 multiframe.

TSaCR: TRANSMIT Sa BIT CONTROL REGISTER (Address=1C Hex)

(MSB) (LSB)

SiAF	SiNAF	RA	Sa4	Sa5	Sa6	Sa7	Sa8

SYMBOLS	POSITION	NAME AND DESCRIPTION
SiAF	TSaCR.7	International Bit in Align Frame Insertion Control Bit. 0=do not insert data from the TSiAF register into the transmit data stream. 1=insert data from the TSiAF register into the transmit data stream.
SiNAF	TSaCR.6	International Bit in Non–Align Frame Insertion Control Bit. 0=do not insert data from the TSiNAF register into the transmit data stream. 1=insert data from the TSiNAF register into the transmit data stream.
RA	TSaCR.5	Remote Alarm Insertion Control Bit. 0=do not insert data from the TRA register into the transmit data stream. 1=insert data from the TRA register into the transmit data stream.
Sa4	TSaCR.4	Additional Bit 4 Insertion Control Bit. 0=do not insert data from the TSa4 register into the transmit data stream. 1=insert data from the TSa4 register into the transmit data stream.

SYMBOLS	POSITION	NAME AND DESCRIPTION
Sa5	TSaCR.3	Additional Bit 5 Insertion Control Bit. 0=do not insert data from the TSa5 register into the transmit data stream. 1=insert data from the TSa5 register into the transmit data stream.
Sa6	TSaCR.2	Additional Bit 6 Insertion Control Bit. 0=do not insert data from the TSa6 register into the transmit data stream. 1=insert data from the TSa6 register into the transmit data stream.
Sa7	TSaCR.1	Additional Bit 7 Insertion Control Bit. 0=do not insert data from the TSa7 register into the transmit data stream. 1=insert data from the TSa7 register into the transmit data stream.
Sa8	TSaCR.0	Additional Bit 8 Insertion Control Bit. 0=do not insert data from the TSa8 register into the transmit data stream. 1=insert data from the TSa8 register into the transmit data stream.

14. HDLC CONTROLLER FOR THE SA BITS OR DS0

Each framer in the DS21FT40 has the ability to extract/insert data from/ into the Sa bit positions (Sa4 to Sa8) or from/to any multiple of DS0 channels Each framer contains a complete HDLC controller and this operation is covered in Section 14.1.

14.1 GENERAL OVERVIEW

Each framer contains a complete HDLC controller with 64–byte buffers in both the transmit and receive directions. The HDLC controller performs all the necessary overhead for generating and receiving a HDLC formatted message.

The HDLC controller automatically generates and detects flags, generates and checks the CRC check sum, generates and detects abort sequences, stuffs and destuffs zeros (for transparency), and byte aligns to the HDLC data stream.

There are eleven registers that the host will use to operate and control the operation of the HDLC controller. A brief description of the registers is shown in Table 14-1.

HDLC CONTROLLER REGISTER LIST Table 14-1

NAME	FUNCTION
HDLC Control Register (HCR)	general control over the HDLC and BOC controllers
HDLC Status Register (HSR)	key status information for both transmit and receive directions
HDLC Interrupt Mask Register (HIMR)	allows/stops status bits to/from causing an interrupt
Receive HDLC Information Register (RHIR)	status information on receive HDLC controller
Receive HDLC FIFO Register (RHFR)	access to 64–byte HDLC FIFO in receive direction
Receive HDLC DS0 Control Register 1 (RDC1) Receive HDLC DS0 Control Register 2 (RDC2)	controls the HDLC function when used on DS0 channels
Transmit HDLC Information Register (THIR)	status information on transmit HDLC controller
Transmit BOC Register (TBOC)	enables/disables transmission of BOC codes
Transmit HDLC FIFO Register (THFR)	access to 64–byte HDLC FIFO in transmit direction
Transmit HDLC DS0 Control Register 1 (TDC1) Transmit HDLC DS0 Control Register 2 (TDC2)	controls the HDLC function when used on DS0 channels

14.2 HDLC STATUS REGISTERS

Three of the HDLC controller registers (HSR, RHIR, and THIR) provide status information. When a particular event has occurred (or is occurring), the appropriate bit in one of these three registers will be set to a one. Some of the bits in these three status registers are latched and some are real time bits that are not latched. Section 14.4 contains register descriptions that list which bits are latched and which are not. With the latched bits, when an event occurs and a bit is set to a one, it will remain set until the user reads that bit. The bit will be cleared when it is read and it will not be set again until the event has occurred again. The real time bits report the current instantaneous conditions that are occurring and the history of these bits is not latched.

Like the other status registers in the framer, the user will always proceed a read of any of the three registers with a write. The byte written to the register will inform the framer which of the latched bits the user wishes to read and have cleared (the real time bits are not affected by writing to the status register). The user will write a byte to one of these registers, with a one in the bit positions he or she wishes to read and a zero in the bit positions he or she does not wish to obtain the latest information on. When a one is written to a bit location, the read register will be updated with current value and it will be cleared. When a zero is written to a bit position, the read register will not be updated and the previous value will be held. A write to the status and information registers will be immediately followed by a read of the same register. The read result should be logically AND'ed with the mask byte that was just written and this value should be written back into the same register to insure that bit does indeed clear. This second write step is necessary because the alarms and events in the status registers occur asynchronously in respect to their access via the parallel port. This write–read–write (for polled driven access) or write–read (for interrupt driven access) scheme allows an external microcontroller or microprocessor to individually poll certain bits without disturbing the other bits in the register. This operation is key in controlling the DS21FT40 with higher–order software languages.

Like the SR1 and SR2 status registers, the HSR register has the unique ability to initiate a hardware interrupt via the INT* output pin. Each of the events in the HSR can be either masked or unmasked from the interrupt pin via the HDLC Interrupt Mask Register (HIMR). Interrupts will force the INT* pin low when the event occurs. The INT* pin will be allowed to return high (if no other interrupts are present) when the user reads the event bit that caused the interrupt to occur.

14.3 BASIC OPERATION DETAILS

As a basic guideline for interpreting and sending HDLC messages, the following sequences can be applied:

Receive a HDLC Message

1. Enable RPS interrupts.
2. Wait for interrupt to occur.
3. Disable RPS interrupt and enable either RPE, RNE, or RHALF interrupt.
4. Read RHIR to obtain REMPTY status.
    - A. If REMPTY=0, then record OBYTE, CBYTE, and POK bits and then read the FIFO
        - A1. If CBYTE=0 then skip to step 5
        - A2. If CBYTE=1 then skip to step 7
    - B. If REMPTY=1, then skip to step 6
5. Repeat step 4.
6. Wait for interrupt, skip to step 4.
7. If POK=0, then discard whole packet, if POK=1, accept the packet.
8. Disable RPE, RNE, or RHALF interrupt, enable RPS interrupt and return to step 1.

Transmit a HDLC Message

1. Make sure HDLC controller is done sending any previous messages and is current sending flags by checking that the FIFO is empty by reading the TEMPTY status bit in the THIR register.
2. Enable either the THALF or TNF interrupt.
3. Read THIR to obtain TFULL status.
   A. If TFULL=0, then write a byte into the FIFO and skip to next step (special case occurs when the last byte is to be written, in this case set TEOM=1 before writing the byte and then skip to step 6)
   B. If TFULL=1, then skip to step 5
4. Repeat step 3.
5. Wait for interrupt, skip to step 3.
6. Disable THALF or TNF interrupt and enable TMEND interrupt.
7. Wait for an interrupt, then read TUDR status bit to make sure packet was transmitted correctly.

14.4 HDLC REGISTER DESCRIPTION

HCR: HDLC CONTROL REGISTER (Address=B0 Hex)

(MSB) (LSB)

–	RHR	TFS	THR	TABT	TEOM	TZSD	TCRCD

SYMBOLS	POSITION	NAME AND DESCRIPTION
–	HCR.7	Not Assigned. Should be set to zero.
RHR	HCR.6	Receive HDLC Reset. A 0 to 1 transition will reset the receive HDLC controller. Must be cleared and set again for a subsequent reset.
TFS	HCR.5	Transmit Flag/Idle Select. 0 = 7Eh. 1 = FFh.
THR	HCR.4	Transmit HDLC Reset. A 0 to 1 transition will reset the transmit HDLC controller. Must be cleared and set again for a subsequent reset.
TABT	HCR.3	Transmit Abort. A 0 to 1 transition will cause the FIFO contents to be dumped and one FEh abort to be sent followed by 7Eh or FFh flags/idle until a new packet is initiated by writing new data into the FIFO. Must be cleared and set again for a subsequent abort to be sent.
TEOM	HCR.2	Transmit End of Message. Should be set to a one just before the last data byte of a HDLC packet is written into the transmit FIFO at THFR. The HDLC controller will clear this bit when the last byte has been transmitted.
TZSD	HCR.1	Transmit Zero Stuffer Defeat. Overrides internal enable. 0 = enable the zero stuffer (normal operation). 1 = disable the zero stuffer.
TCRCD	HCR.0	Transmit CRC Defeat. 0 = enable CRC generation (normal operation). 1 = disable CRC generation.

HSR: HDLC STATUS REGISTER (Address=B1 Hex)

(MSB) (LSB)

–	RPE	RPS	RHALF	RNE	THALF	TNF	TMEND

SYMBOLS	POSITION	NAME AND DESCRIPTION
–	HSR.7	Not Assigned. Should be set to zero.
RPE	HSR.6	Receive Packet End. Set when the HDLC controller detects either the finish of a valid message (i.e., CRC check complete) or when the controller has experienced a message fault such as a CRC checking error, or an overrun condition, or an abort has been seen. The setting of this bit prompts the user to read the RHIR register for details.
RPS	HSR.5	Receive Packet Start. Set when the HDLC controller detects an opening byte. The setting of this bit prompts the user to read the RHIR register for details.
RHALF	HSR.4	Receive FIFO Half Full. Set when the receive 64–byte FIFO fills beyond the half way point. The setting of this bit prompts the user to read the RHIR register for details.
RNE	HSR.3	Receive FIFO Not Empty. Set when the receive 64–byte FIFO has at least one byte available for a read. The setting of this bit prompts the user to read the RHIR register for details.
THALF	HSR.2	Transmit FIFO Half Empty. Set when the transmit 64–byte FIFO empties beyond the half way point. The setting of this bit prompts the user to read the THIR register for details.
TNF	HSR.1	Transmit FIFO Not Full. Set when the transmit 64–byte FIFO has at least one byte available. The setting of this bit prompts the user to read the THIR register for details.
TMEND	HSR.0	Transmit Message End. Set when the transmit HDLC controller has finished sending a message. The setting of this bit prompts the user to read the THIR register for details.

NOTE:

The RPE, RPS, and TMEND bits are latched and will be cleared when read.

HIMR: HDLC INTERRUPT MASK REGISTER (Address=B2 Hex)

(MSB) (LSB)

–	RPE	RPS	RHALF	RNE	THALF	TNF	TMEND

SYMBOLS	POSITION	NAME AND DESCRIPTION
–	HIMR.7	Not Assigned. Should be set to zero.
RPE	HIMR.6	Receive Packet End. 0 = interrupt masked. 1 = interrupt enabled.
RPS	HIMR.5	Receive Packet Start. 0 = interrupt masked. 1 = interrupt enabled.

SYMBOLS	POSITION	NAME AND DESCRIPTION
RHALF	HIMR.4	Receive FIFO Half Full. 0 = interrupt masked. 1 = interrupt enabled.
RNE	HIMR.3	Receive FIFO Not Empty. 0 = interrupt masked. 1 = interrupt enabled.
THALF	HIMR.2	Transmit FIFO Half Empty. 0 = interrupt masked. 1 = interrupt enabled.
TNF	HIMR.1	Transmit FIFO Not Full. 0 = interrupt masked. 1 = interrupt enabled.
TMEND	HIMR.0	Transmit Message End. 0 = interrupt masked. 1 = interrupt enabled.

RHIR: RECEIVE HDLC INFORMATION REGISTER (Address=B3 Hex)

(MSB) (LSB)

RABT	RCRCE	ROVR	RVM	REMPTY	POK	CBYTE	OBYTE

SYMBOLS	POSITION	NAME AND DESCRIPTION
RABT	RHIR.7	Abort Sequence Detected. Set whenever the HDLC controller sees 7 or more ones in a row.
RCRCE	RHIR.6	CRC Error. Set when the CRC checksum is in error.
ROVR	RHIR.5	Overrun. Set when the HDLC controller has attempted to write a byte into an already full receive FIFO.
RVM	RHIR.4	Valid Message. Set when the HDLC controller has detected and checked a complete HDLC packet.
REMPTY	RHIR.3	Empty. A real–time bit that is set high when the receive FIFO is empty.
POK	RHIR.2	Packet OK. Set when the byte available for reading in the receive FIFO at RHFR is the last byte of a valid message (and hence no abort was seen, no overrun occurred, and the CRC was correct).
CBYTE	RHIR.1	Closing Byte. Set when the byte available for reading in the receive FIFO at RFDL is the last byte of a message (whether the message was valid or not).
OBYTE	RHIR.0	Opening Byte. Set when the byte available for reading in the receive FIFO at RHFR is the first byte of a message.

NOTE:

The RABT, RCRCE, ROVR, and RVM bits are latched and will be cleared when read.

RHFR: RECEIVE HDLC FIFO REGISTER (Address=B4 Hex)

(MSB)							(LSB)
HDLC7	HDLC6	HDLC5	HDLC4	HDLC3	HDLC2	HDLC1	HDLC0

SYMBOLS	POSITION	NAME AND DESCRIPTION
HDLC7	RHFR.7	HDLC Data Bit 7. MSB of a HDLC packet data byte.
HDLC6	RHFR.6	HDLC Data Bit 6.
HDLC5	RHFR.5	HDLC Data Bit 5.
HDLC4	RHFR.4	HDLC Data Bit 4.
HDLC3	RHFR.3	HDLC Data Bit 3.
HDLC2	RHFR.2	HDLC Data Bit 2.
HDLC1	RHFR.1	HDLC Data Bit 1.
HDLC0	RHFR.0	HDLC Data Bit 0. LSB of a HDLC packet data byte.

THIR: TRANSMIT HDLC INFORMATION REGISTER (Address=B6 Hex)

(MSB)							(LSB)
–	–	–	–	–	EMPTY	TFULL	UDR

SYMBOLS	POSITION	NAME AND DESCRIPTION
–	THIR.7	Not Assigned. Could be any value when read.
–	THIR.6	Not Assigned. Could be any value when read.
–	THIR.5	Not Assigned. Could be any value when read.
–	THIR.4	Not Assigned. Could be any value when read.
–	THIR.3	Not Assigned. Could be any value when read.
TEMPTY	THIR.2	Transmit FIFO Empty. A real–time bit that is set high when the FIFO is empty.
TFULL	THIR.1	Transmit FIFO Full. A real–time bit that is set high when the FIFO is full.
UDR	THIR.0	Underrun. Set when the transmit FIFO unwantedly empties out and an abort is automatically sent.

NOTE:

The UDR bit is latched and will be cleared when read.

THFR: TRANSMIT HDLC FIFO REGISTER (Address=B7 Hex)

(MSB) (LSB)

HDLC7	HDLC6	HDLC5	HDLC4	HDLC3	HDLC2	HDLC1	HDLC0

SYMBOLS	POSITION	NAME AND DESCRIPTION
HDLC7	THFR.7	HDLC Data Bit 7. MSB of a HDLC packet data byte.
HDLC6	THFR.6	HDLC Data Bit 6.
HDLC5	THFR.5	HDLC Data Bit 5.
HDLC4	THFR.4	HDLC Data Bit 4.
HDLC3	THFR.3	HDLC Data Bit 3.
HDLC2	THFR.2	HDLC Data Bit 2.
HDLC1	THFR.1	HDLC Data Bit 1.
HDLC0	THFR.0	HDLC Data Bit 0. LSB of a HDLC packet data byte.

RDC1: RECEIVE HDLC DS0 CONTROL REGISTER 1 (Address=B8 Hex)

(MSB) (LSB)

RHS	RSaDS	RDS0M	RD4	RD3	RD2	RD1	RD0

SYMBOLS	POSITION	NAME AND DESCRIPTION
RHS	RDC1.7	Receive HDLC source 0 = Sa bits defined by RCR2.3 to RCR2.7. 1 = Sa bits or DS0 channels defined by RDC1 (see bits defined below).
RSaDS	RDC1.6	Receive Sa Bit / DS0 Select. 0 = route Sa bits to the HDLC controller. RD0 to RD4 defines which Sa bits are to be routed. RD4 corresponds to Sa4, RD3 to Sa5, RD2 to Sa6, RD1 to Sa7 and RD0 to Sa8. 1 = route DS0 channels into the HDLC controller. RDC1.5 is used to determine how the DS0 channels are selected.
RDS0M	RDC1.5	DS0 Selection Mode. 0 = utilize the RD0 to RD4 bits to select which single DS0 channel to use. 1 = utilize the RCHBLK control registers to select which DS0 channels to use. This option is not applicable for the DS21FT40.
RD4	RDC1.4	DS0 Channel Select Bit 4. MSB of the DS0 channel select.
RD3	RDC1.3	DS0 Channel Select Bit 3.
RD2	RDC1.2	DS0 Channel Select Bit 2.
RD1	RDC1.1	DS0 Channel Select Bit 1.
RD0	RDC1.0	DS0 Channel Select Bit 0. LSB of the DS0 channel select.

RDC2: RECEIVE HDLC DS0 CONTROL REGISTER 2 (Address=B9 Hex)

(MSB) (LSB)

RDB8	RDB7	RDB6	RDB5	RDB4	RDB3	RDB2	RDB1

SYMBOLS	POSITION	NAME AND DESCRIPTION
RDB8	RDC2.7	DS0 Bit 8 Suppress Enable. MSB of the DS0. Set to one to stop this bit from being used.
RDB7	RDC2.6	DS0 Bit 7 Suppress Enable. Set to one to stop this bit from being used.
RDB6	RDC2.5	DS0 Bit 6 Suppress Enable. Set to one to stop this bit from being used.
RDB5	RDC2.4	DS0 Bit 5 Suppress Enable. Set to one to stop this bit from being used.
RDB4	RDC2.3	DS0 Bit 4 Suppress Enable. Set to one to stop this bit from being used.
RDB3	RDC2.2	DS0 Bit 3 Suppress Enable. Set to one to stop this bit from being used.
RDB2	RDC2.1	DS0 Bit 2 Suppress Enable. Set to one to stop this bit from being used.
RDB1	RDC2.0	DS0 Bit 1 Suppress Enable. LSB of the DS0. Set to one to stop this bit from being used.

TDC1: TRANSMIT HDLC DS0 CONTROL REGISTER 1 (Address = BA Hex)

(MSB) (LSB)

THE	TSaDS	TDS0M	TD4	TD3	TD2	TD1	TD0

SYMBOLS	POSITION	NAME AND DESCRIPTION
THE	TDC1.7	Transmit HDLC Enable. 0 = disable HDLC controller (no data inserted by HDLC controller into the transmit data stream) 1 = enable HDLC controller to allow insertion of HDLC data into either the Sa position or multiple DS0 channels as defined by TDC1 (see bit definitions below).
TSaDS	TDC1.6	Transmit Sa Bit / DS0 Select. This bit is ignored if TDC1.7 is set to zero. 0 = route Sa bits from the HDLC controller. TD0 to TD4 defines which Sa bits are to be routed. TD4 corresponds to Sa4, TD3 to Sa5, TD2 to Sa6, TD1 to Sa7 and TD0 to Sa8. 1 = route DS0 channels from the HDLC controller. TDC1.5 is used to determine how the DS0 channels are selected.
TDS0M	TDC1.5	DS0 Selection Mode. Not applicable for the DS21FT40. Should be cleared to zero.

SYMBOLS	POSITION	NAME AND DESCRIPTION
TD4	TDC1.4	DS0 Channel Select Bit 4. MSB of the DS0 channel select.
TD3	TDC1.3	DS0 Channel Select Bit 3.
TD2	TDC1.2	DS0 Channel Select Bit 2.
TD1	TDC1.1	DS0 Channel Select Bit 1.
TD0	TDC1.0	DS0 Channel Select Bit 0. LSB of the DS0 channel select.

TDC2: TRANSMIT HDLC DS0 CONTROL REGISTER 2 (Address = BB Hex)

(MSB)							(LSB)
TDB8	TDB7	TDB6	TDB5	TDB4	TDB3	TDB2	TDB1

SYMBOLS	POSITION	NAME AND DESCRIPTION
TDB8	TDC2.7	DS0 Bit 8 Suppress Enable. MSB of the DS0. Set to one to stop this bit from being used.
TDB7	TDC2.6	DS0 Bit 7 Suppress Enable. Set to one to stop this bit from being used.
TDB6	TDC2.5	DS0 Bit 6 Suppress Enable. Set to one to stop this bit from being used.
TDB5	TDC2.4	DS0 Bit 5 Suppress Enable. Set to one to stop this bit from being used.
TDB4	TDC2.3	DS0 Bit 4 Suppress Enable. Set to one to stop this bit from being used.
TDB3	TDC2.2	DS0 Bit 3 Suppress Enable. Set to one to stop this bit from being used.
TDB2	TDC2.1	DS0 Bit 2 Suppress Enable. Set to one to stop this bit from being used.
TDB1	TDC2.0	DS0 Bit 1 Suppress Enable. LSB of the DS0. Set to one to stop this bit from being used.

15. INTERLEAVED PCM BUS OPERATION

In many architectures, the outputs of individual framers are combined into higher speed serial buses to simplify transport across the system. The DS21FT40 can be configured to allow each framer's data and signaling busses to be multiplexed into higher speed data and signaling busses eliminating external hardware saving board space and cost. In particular, the four framers associated with each DS21Q44 die can be combined.

The interleaved PCM bus option supports two bus speeds and interleave modes. The 4.096 MHz bus speed allows two framers to share a common bus. The 8.192 MHz bus speed allows all four of the framers for each DS21Q44 die to share a common bus. Framers can interleave their data either on byte or frame boundaries. Framers that share a common bus must be configured through software and require several device pins to be connected together externally (see figures 15-1 & 15-2). Each framer's elastic stores must be enabled and configured for 2.048 MHz operation. The signal RSYNC must be configured as an input on each framer.

For all bus configurations, one framer will be configured as the master device and the remaining framers on the shared bus will be configured as slave devices. Refer to the IBO register description below for more detail. In the 4.096 MHz bus configuration there is one master and one slave per bus. Figure 15-1 shows the DS21Q44 configured to support two 4.096 MHz buses. Bus 1 consists of framers 0 and 1. Bus 2 consists of framers 2 and 3. Framers 0 and 2 are programmed as master devices. Framers 1 and 3 are programmed as slave devices. In the 8.192 MHz bus configuration there is one master and three slaves. Figure 15-2 shows the DS21Q44 configured to support a 8.192 MHz bus. Framer 0 is programmed as the master device. Framers 1, 2 and 3 are programmed as slave devices. Consult timing diagrams in section 16 for additional information.

When using the frame interleave mode, all framers that share an interleaved bus must have receive signals (RPOS & RNEG) that are synchronous with each other. The received signals must originate from the same clock reference. This restriction does not apply in the byte interleave mode.

IBO: INTERLEAVE BUS OPERATION REGISTER (Address = B5 Hex)

(MSB) (LSB)

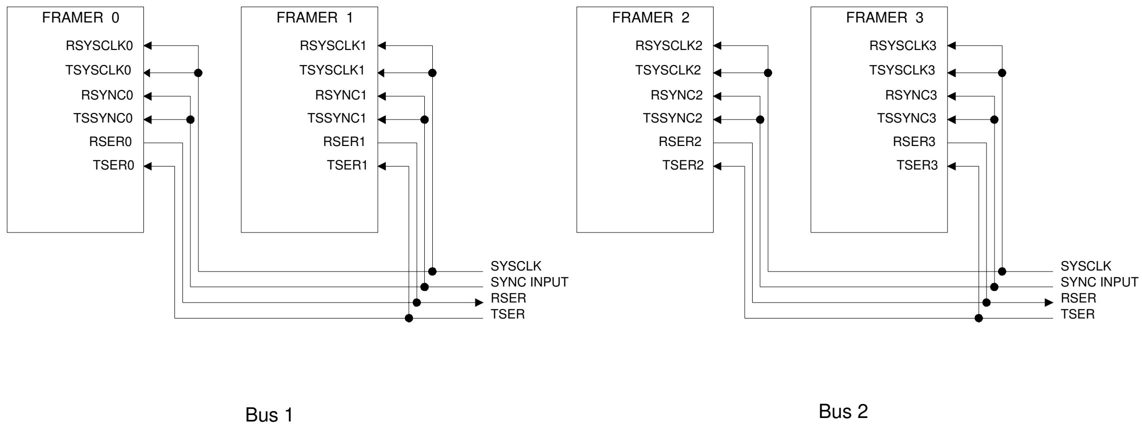
–	–	–	–	IBOEN	INTSEL	MSEL0	MSEL1

SYMBOLS	POSITION	NAME AND DESCRIPTION
–	IBO.7	Not Assigned. Should be set to 0.
–	IBO.6	Not Assigned. Should be set to 0.
–	IBO.5	Not Assigned. Should be set to 0.
–	IBO.4	Not Assigned. Should be set to 0.
IBOEN	IBO.3	Interleave Bus Operation Enable 0 = Interleave Bus Operation disabled. 1 = Interleave Bus Operation enabled.
INTSEL	IBO.2	Interleave Type Select 0 = Byte interleave. 1 = Frame interleave.
MSEL0	IBO.1	Master Device Bus Select Bit 0 See table 15-1.
MSEL1	IBO.0	Master Device Bus Select Bit 1 See table 15-1.

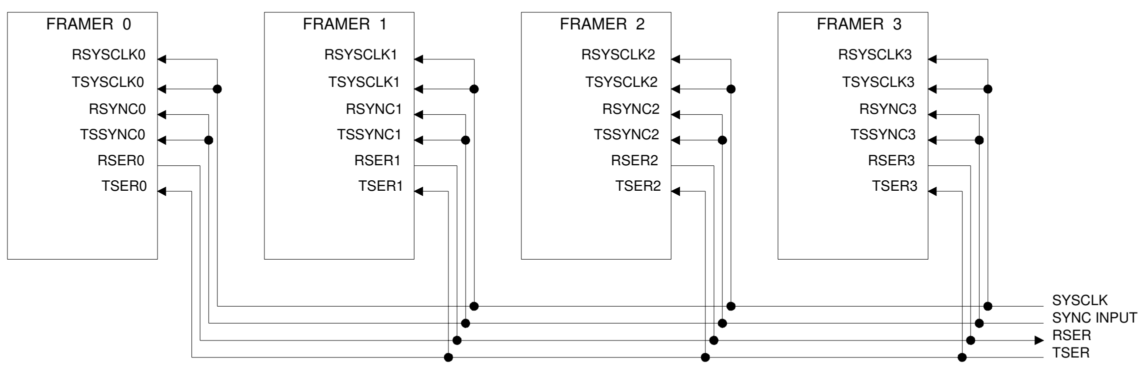
Master Device Bus Select Table 15-1

MSEL1	MSEL0	Function
0	0	Slave device.
0	1	Master device with 1 slave device (4.096 MHz bus rate)
1	0	Master device with 3 slave devices (8.192 MHz bus rate)
1	1	Reserved

4.096 MHz Interleaved Bus External Pin Connection Example Figure 15-1

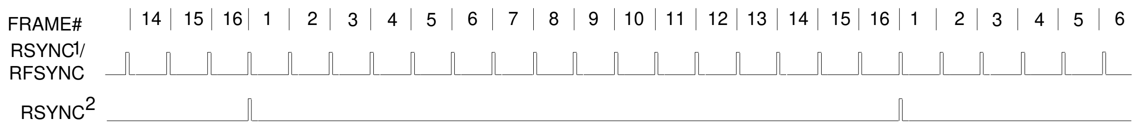


8.192 MHz Interleaved Bus External Pin Connection Example Figure 15-2



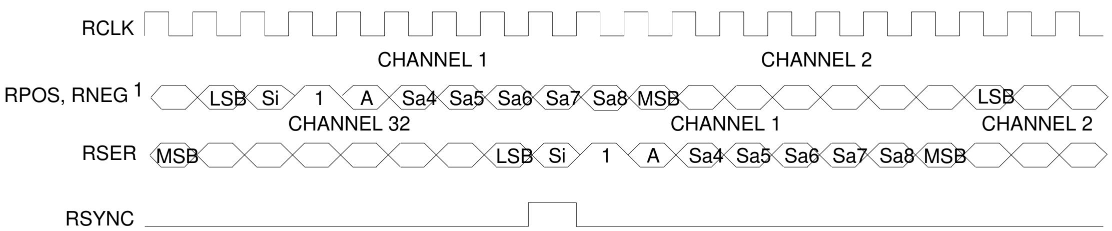
16. TIMING DIAGRAMS

Receive Side Timing Figure 16-1



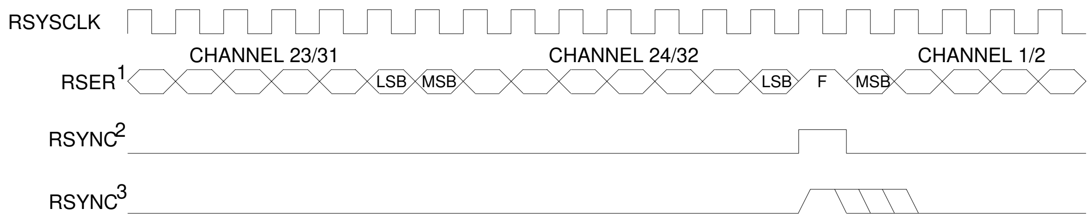
Notes:
1. RSYNC in the frame mode (RCR1.6 = 0)
2. RSYNC in the multiframe mode (RCR1.6 = 1)
3. This diagram assumes the CAS MF begins with the FAS word

RECEIVE SIDE BOUNDARY TIMING (with elastic store disabled) Figure 16-2



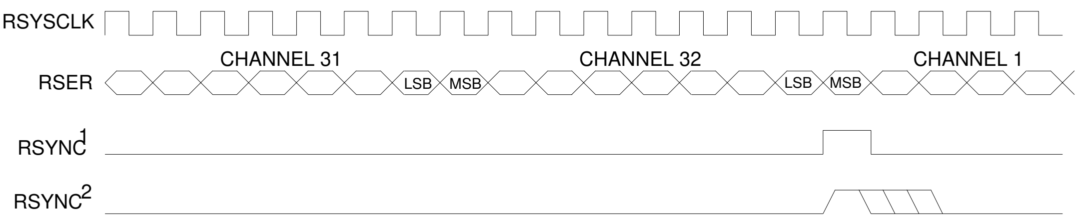
Notes:
1. There is a 6 RCLK delay from RPOS, RNEG to RSER
2. Shown is a non-align frame boundary

RECEIVE SIDE 1.544 MHz BOUNDARY TIMING (with elastic store enabled)
Figure 16-3



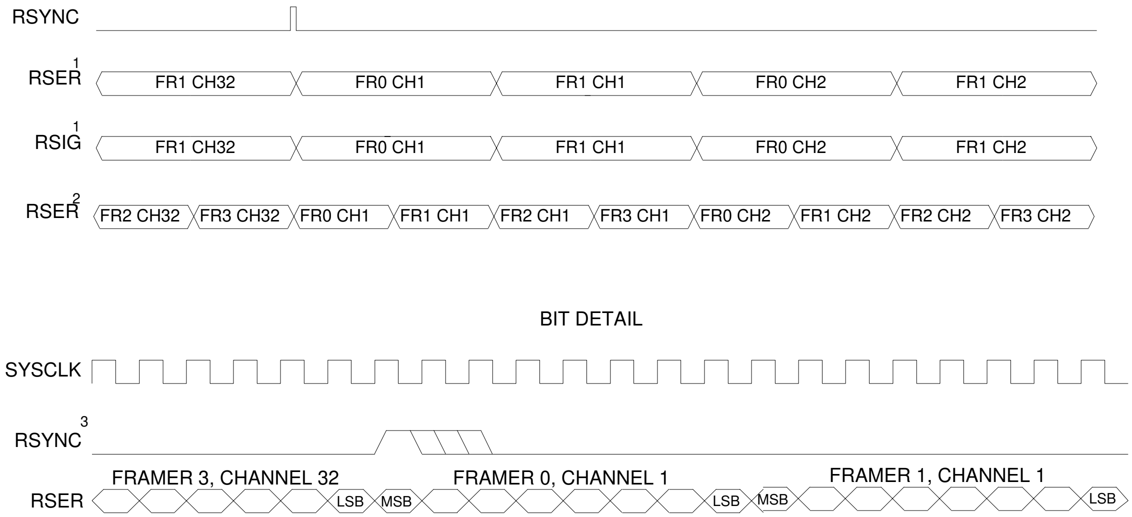
Notes:
1. Data from the E1 channels 1, 5, 9, 13, 17, 21, 25, and 29 is dropped (channel 2 from the E1 link is mapped to channel 1 of the T1 link, etc.) and the F-bit position is added (forced to one)
2. RSYNC is in the output mode (RCR1.5 = 0)
3. RSYNC is in the input mode (RCR1.5 = 1)

RECEIVE SIDE 2.048 MHz BOUNDARY TIMING (with elastic store enabled)
Figure 16-4



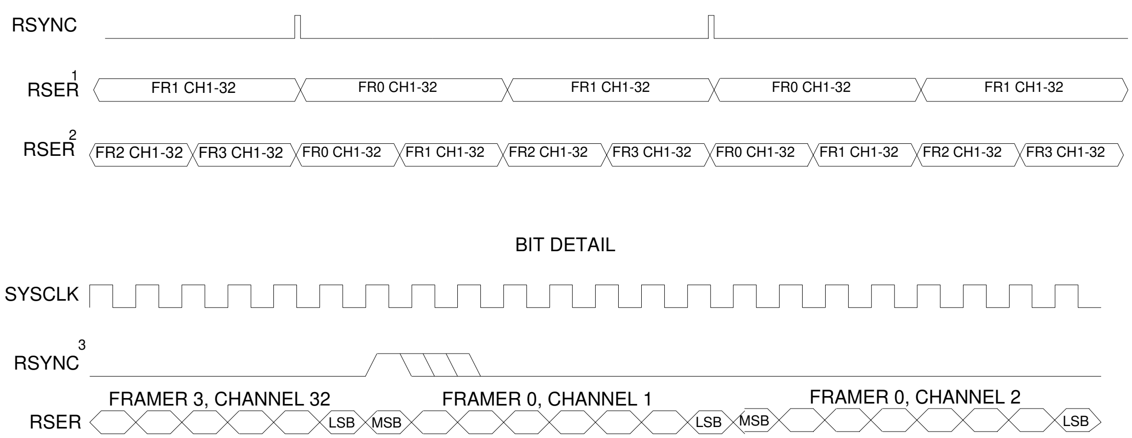
Notes:
1. RSYNC is in the output mode (RCR1.5 = 0)
2. RSYNC is in the input mode (RCR1.5 = 1)

RECEIVE SIDE INTERLEAVED BUS OPERATION BYTE MODE TIMING
Figure 16-5



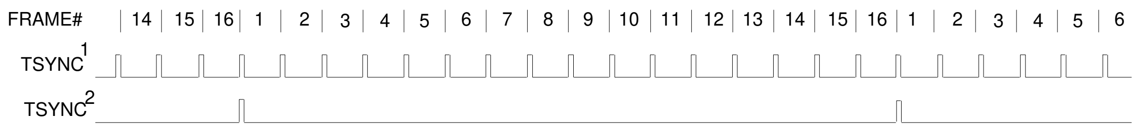
Notes:
1. 4.096 MHz bus configuration.
2. 8.192 MHz bus configuration.
3. RSYNC is in the input mode (RCR1.5 = 1).

RECEIVE SIDE INTERLEAVED BUS OPERATION FRAME MODE TIMING
Figure 16-6



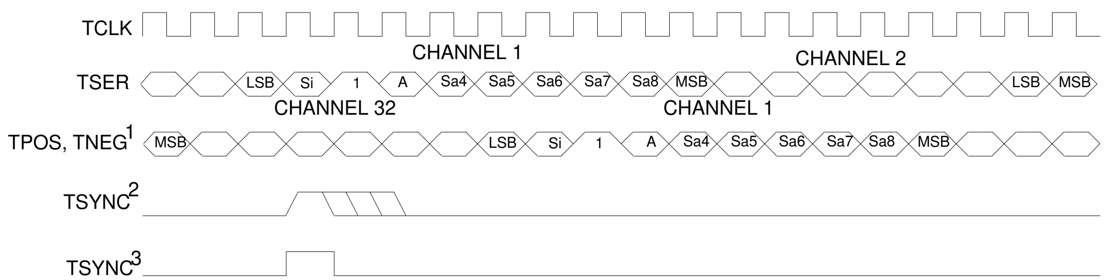
Notes:
1. 4.096 MHz bus configuration.
2. 8.192 MHz bus configuration.
3. RSYNC is in the input mode (RCR1.5 = 1).

TRANSMIT SIDE TIMING Figure 16-7



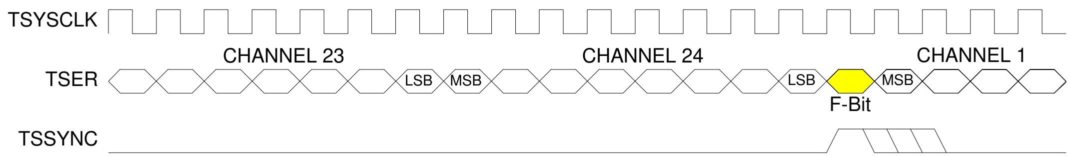
Notes:
1. TSYNC in the frame mode (TCR1.1 = 0)
2. TSYNC in the multiframe mode (TCR1.1 = 1)
3. This diagram assumes both the CAS MF and the CRC4 begin with the align frame

TRANSMIT SIDE BOUNDARY TIMING (with elastic store disabled) Figure 16-8



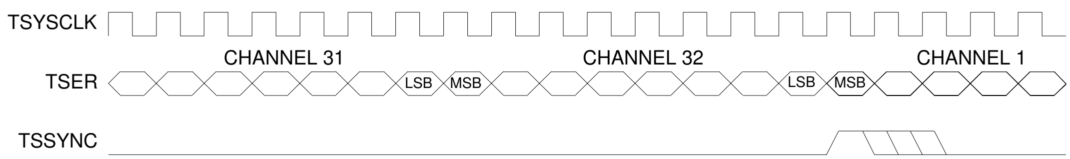
Notes:
1. There is a 5 TCLK delay from TSER to TPOS and TNEG
2. TSYNC is in the input mode (TCR1.0 = 0)
3. TSYNC is in the output mode (TCR1.0 = 1)
4. Shown is a non-align frame boundary

TRANSMIT SIDE 1.544 MHz BOUNDARY TIMING (with elastic store enabled)
Figure 16-9

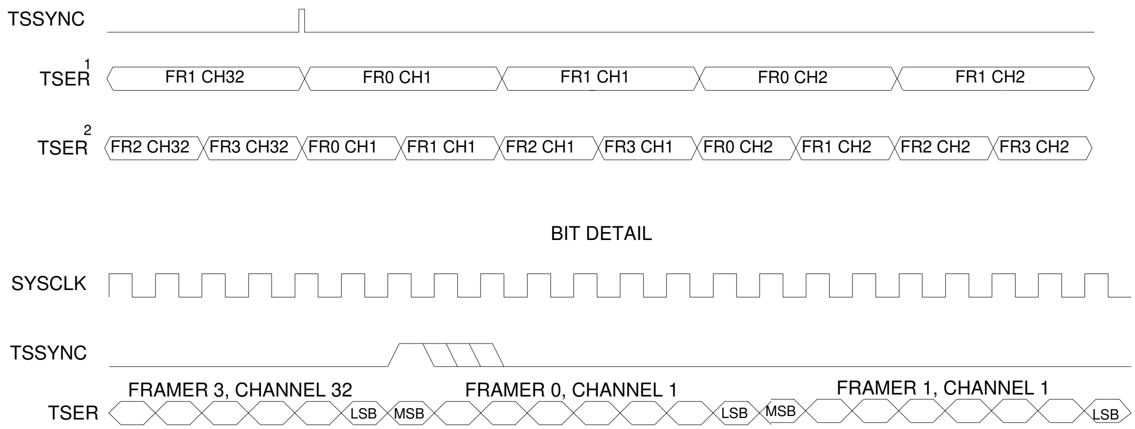


Notes:
1. The F-bit position is ignored by the DS21FT40

TRANSMIT SIDE 2.048 MHz BOUNDARY TIMING (with elastic store enabled)
Figure 16-10

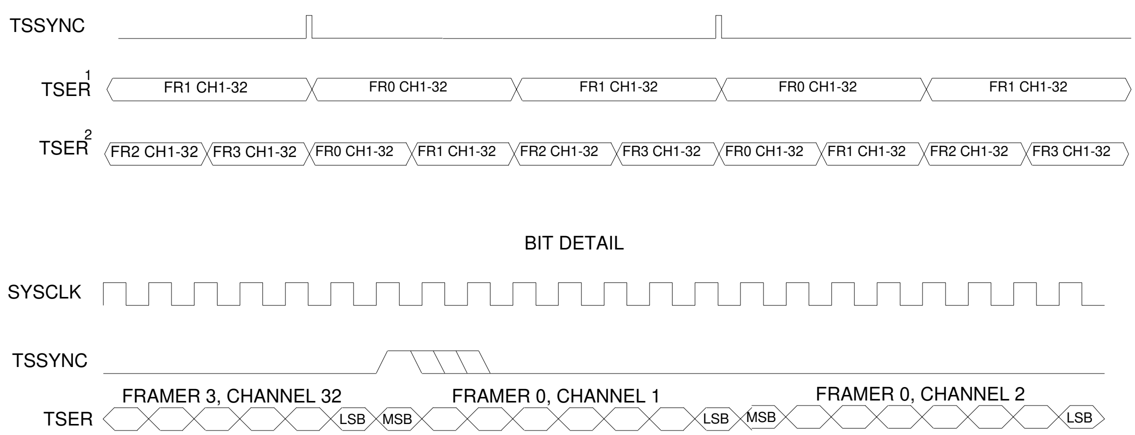


TRANSMIT SIDE INTERLEAVED BUS OPERATION BYTE MODE TIMING
Figure 16-11



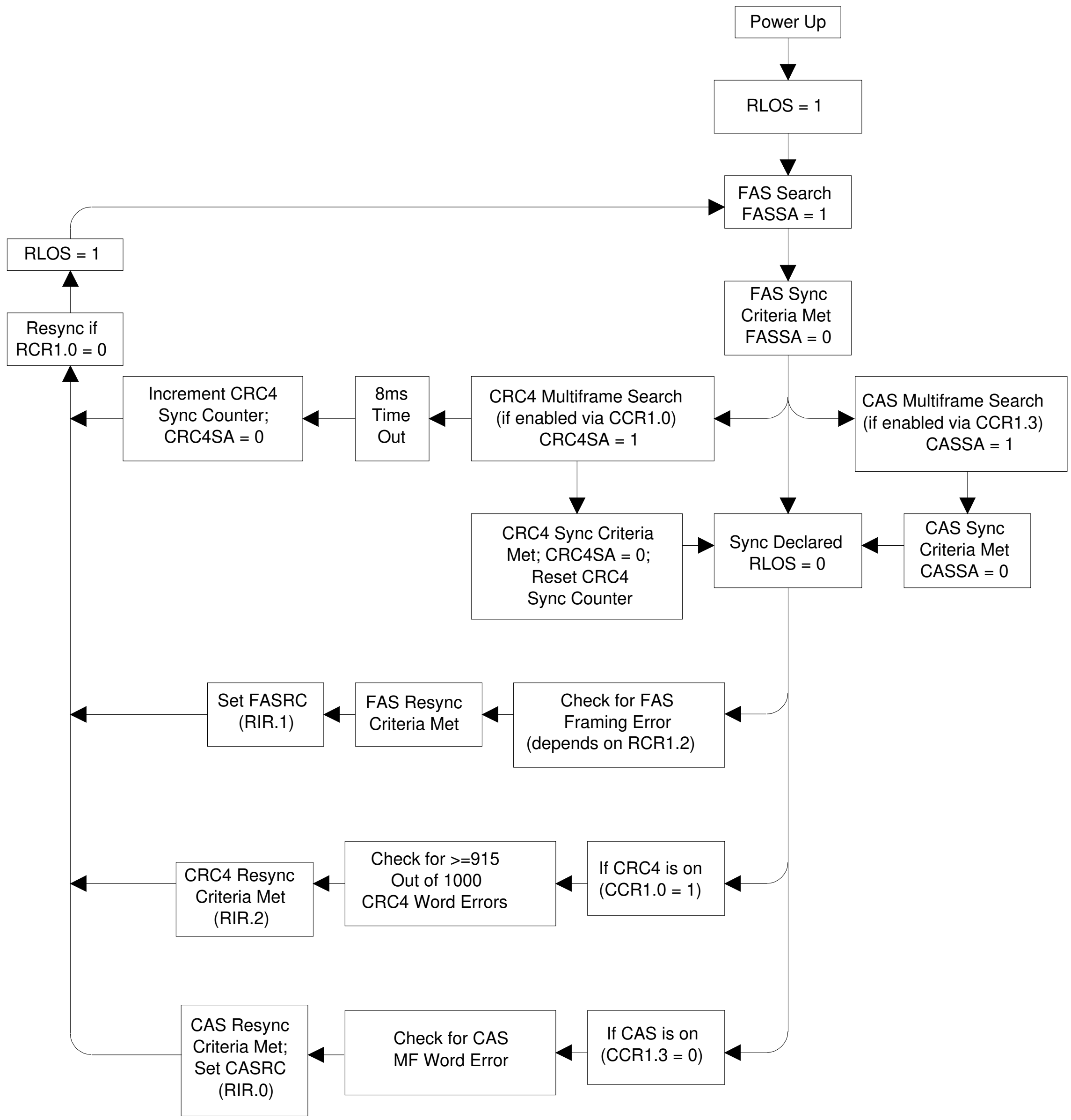
Notes:
1. 4.096 MHz bus configuration.
2. 8.192 MHz bus configuration.

TRANSMIT SIDE INTERLEAVED BUS OPERATION FRAME MODE TIMING
Figure 16-12

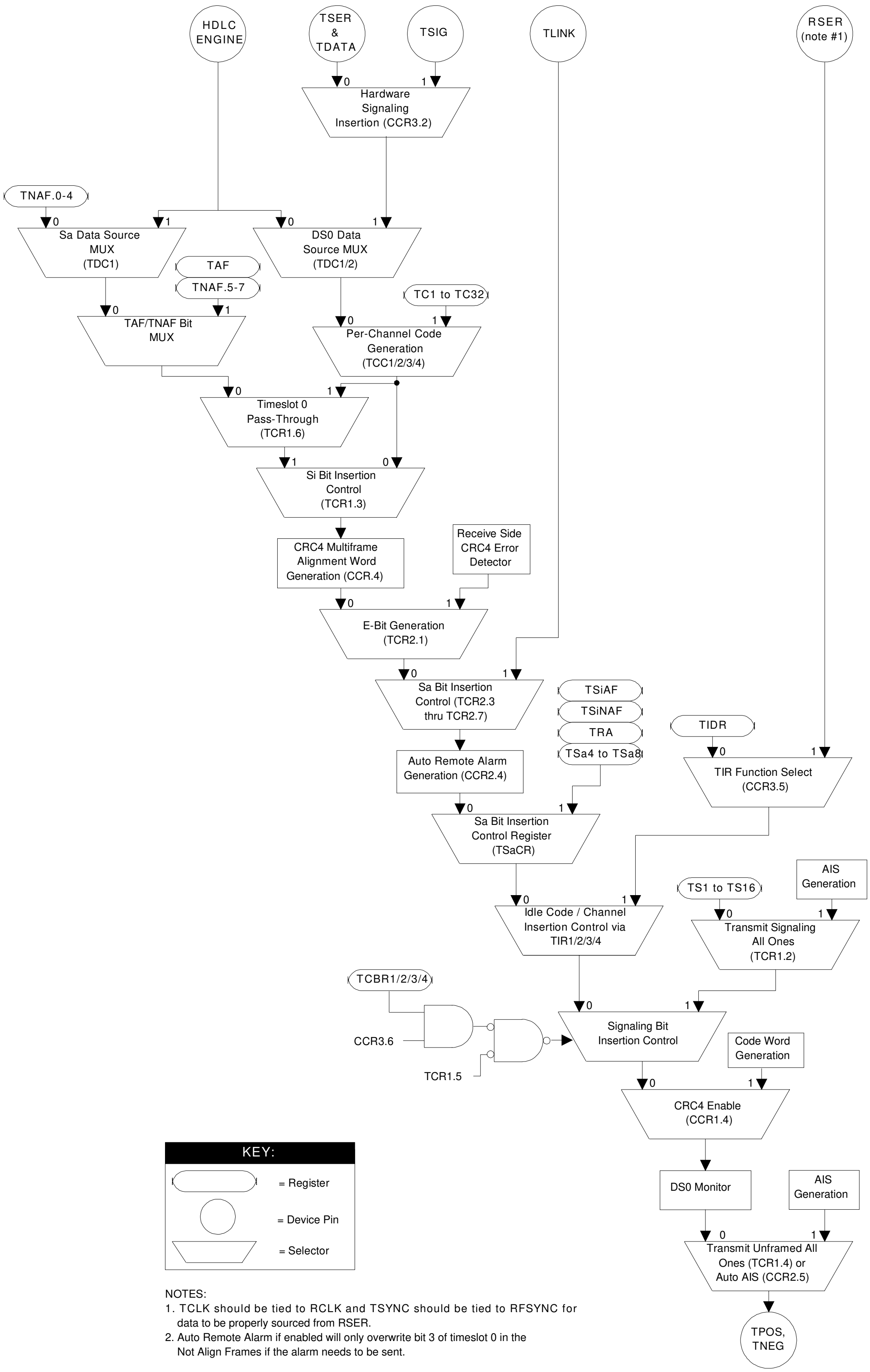


Notes:
1. 4.096 MHz bus configuration.
2. 8.192 MHz bus configuration.

DS21FT40 FRAMER SYNCHRONIZATION FLOWCHART Figure 16-13



DS21FT40 TRANSMIT DATA FLOW Figure 16-14



NOTES:
1. TCLK should be tied to RCLK and TSYNC should be tied to RFSYNC for data to be properly sourced from RSER.
2. Auto Remote Alarm if enabled will only overwrite bit 3 of timeslot 0 in the Not Align Frames if the alarm needs to be sent.

17. OPERATING PARAMETERS

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Non-Supply Pin Relative to Ground	–1.0V to +5.5V
Supply Voltage	–.3V to +3.63V
Operating Temperature for DS21FT40	0ºC to 70ºC
Operating Temperature for DS21FT40N	–40ºC to +85ºC
Storage Temperature	–55ºC to +125ºC
Soldering Temperature	See J-STD-020A

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0ºC to 70ºC for DS21FT40;
0ºC to +85ºC for DS21FT40N)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		5.5	V	
Logic 0	V_{IL}	–0.3		+0.8	V	
Supply	V_{DD}	2.97		3.63	V	

CAPACITANCE

(t_A =25ºC)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5		pF	
Output Capacitance	C_{OUT}		7		pF	

DC CHARACTERISTICS

(0ºC to 70ºC; V_{DD} = 2.97 to 3.63V for DS21FT40;
-40ºC to +85ºC; V_{DD} = 2.97 to 3.63V for DS21Q44N)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current @ 3.3V	I_{DD}		75		mA	1
Input Leakage	I_{IL}	–1.0		+1.0	µA	2
Output Leakage	I_{LO}			1.0	µA	3
Output Current (2.4V)	I_{OH}	–1.0			mA	
Output Current (0.4V)	I_{OL}	+4.0			mA	

NOTES:

1. TCLK=RCLK=TSYSCLK=RSYSCLK=2.048 MHz; outputs open circuited.
2. 0.0V < V IN < V DD .
3. Applied to INT* when 3–stated.

AC CHARACTERISTICS – MULTIPLEXED PARALLEL PORT (MUX=1)

(0ºC to 70ºC; V_{DD} = 2.97 to 3.63V for DS21FT40
–40ºC to +85ºC; V_{DD} = 2.97 to 3.63V for DS21FT40N)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	200			ns	
Pulse Width, DS low or RD* high	PW_{EL}	100			ns	
Pulse Width, DS high or RD* low	PW_{EH}	100			ns	
Input Rise/Fall times	t_R , t_F			20	ns	
R/W* Hold Time	t_{RWH}	10			ns	
R/W* Set Up time before DS high	t_{RWS}	50			ns	
CS1*, CS2*, CS3*, FSO or FS1 Set Up time before DS, WR* or RD* active	t_{CS}	20			ns	
CS1*, CS2*, CS3*, FSO or FS1 Hold time	t_{CH}	0			ns	
Read Data Hold time	t_{DHR}	10		50	ns	
Write Data Hold time	t_{DHW}	0			ns	
Muxed Address valid to AS or ALE fall	t_{ASL}	15			ns	
Muxed Address Hold time	t_{AHL}	10			ns	
Delay time DS, WR* or RD* to AS or ALE rise	t_{ASD}	20			ns	
Pulse Width AS or ALE high	PW_{ASH}	30			ns	
Delay time, AS or ALE to DS, WR* or RD*	t_{ASED}	10			ns	
Output Data Delay time from DS or RD*	t_{DDR}	20		80	ns	
Data Set Up time	t_{DSW}	50			ns	

(see Figures 17-1 to 17-3 for details)

AC CHARACTERISTICS – NON–MULTIPLEXED PARALLEL PORT (MUX=0)

(0ºC to 70ºC; V_{DD} = 2.97 to 3.63V for DS21FT40;
–40ºC to +85ºC; V_{DD} = 2.97 to 3.63V for DS21FT40N)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Set Up Time for A0 to A7, FS0 or FS1 Valid to CS1*, CS2*, CS3* Active	t_1	0			ns	
Set Up Time for CS1*, CS2*, CS3* Active to either RD*, WR*, or DS* Active	t_2	0			ns	
Delay Time from either RD* or DS* Active to Data Valid	t_3			75	ns	
Hold Time from either RD*, WR*, or DS* Inactive to CS1*, CS2*, CS3* Inactive	t_4	0			ns	
Hold Time from CS1*, CS2*, CS3* Inactive to Data Bus 3–state	t_5	5		20	ns	
Wait Time from either WR* or DS* Active to Latch Data	t_6	75			ns	
Data Set Up Time to either WR* or DS* Inactive	t_7	10			ns	
Data Hold Time from either WR* or DS* Inactive	t_8	10			ns	
Address Hold from either WR* or DS* inactive	t_9	10			ns	

See Figures 17–4 to 17-7 for details.

AC CHARACTERISTICS – RECEIVE SIDE

(0ºC to 70ºC; V_{DD} = 2.97 to 3.63V for DS21FT40;
–40ºC to +85ºC; V_{DD} = 2.97 to 3.63V for DS21FT40N)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RCLK Period	t_{CP}		488		ns	
RCLK Pulse Width	t_{CH} t_{CL}	75 75			ns ns	
RSYSCLK Period	t_{SP} t_{SP}	122 122	648 488		ns ns	1 2
RSYSCLK Pulse Width	t_{SH} t_{SL}	50 50			ns ns	
RSYNC Set Up to RSYSCLK Falling	t_{SU}	20		t SH –5	ns	
RSYNC Pulse Width	t_{PW}	50			ns	
RPOS/RNEG Set UP to RCLK Falling	t_{SU}	20			ns	
RPOS/RNEG Hold From RCLK Falling	t_{HD}	20			ns	
RSYSCLK/RCLKI Rise and Fall Times	t_R , t_F			25	ns	
Delay RCLK to RSER Valid	t_{D1}			50	ns	
Delay RCLK to RSYNC	t_{D2}			50	ns	
Delay RSYSCLK to RSER Valid	t_{D3}			50	ns	
Delay RSYSCLK to RMSYNC, RSYNC	t_{D4}			50	ns	

See Figures 17-8 to 17-10 for details.

NOTES:

1. RSYSCLK = 1.544 MHz.
2. RSYSCLK = 2.048 MHz.

AC CHARACTERISTICS – TRANSMIT SIDE

(0ºC to 70ºC; V_{DD} = 2.97 to 3.63V for DS21FT40;
–40ºC to +85ºC; ; V_{DD} = 2.97 to 3.63V for DS21FT40N)

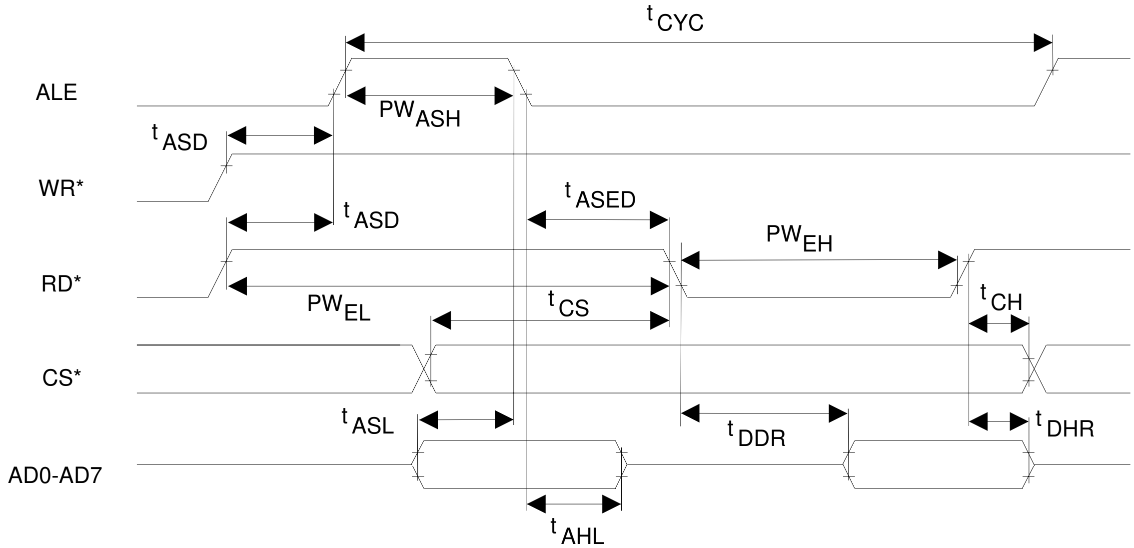
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
TCLK Period	t_{CP}		488		ns	
TCLK Pulse Width	t_{CH} t_{CL}	75 75			ns ns	
TCLKI Pulse Width	t_{LH} t_{LL}	75 75			ns ns	
TSYSCLK Period	t_{SP} t_{SP}	122 122	648 448		ns ns	1 2
TSYSCLK Pulse Width	t_{SH} t_{SL}	50 50			ns ns	
TSYNC or TSSYNC Set Up to TCLK or TSYSCLK falling	t_{SU}	20		t CH –5 or t SH –5	ns	
TSYNC or TSSYNC Pulse Width	t_{PW}	50			ns	
TSER Set Up to TCLK, TSYSCLK Falling	t_{SU}	20			ns	
TSER Hold from TCLK, TSYSCLK Falling	t_{HD}	20			ns	
TCLK or TSYSCLK Rise and Fall Times	t_R , t_F			25	ns	
Delay TCLK to TPOS, TNEG Valid	t_{DD}			50	ns	
Delay TCLK to TSYNC	t_{D2}			50	ns	

See Figures 17–11 to 17–13 for details.

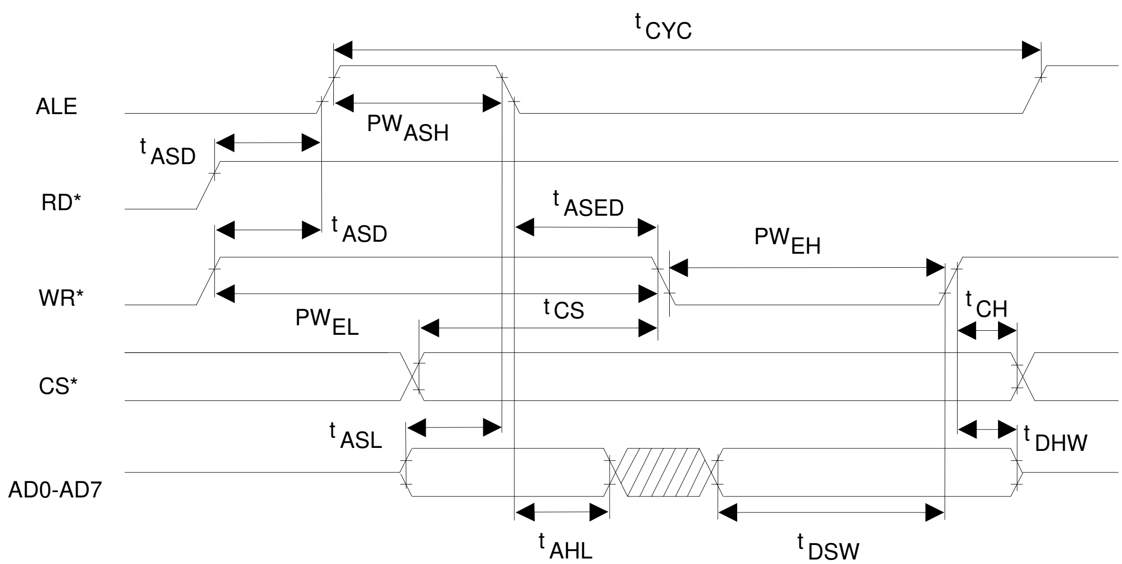
NOTES:

1. TSYSCLK = 1.544 MHz.
2. TSYSCLK = 2.048 MHz.

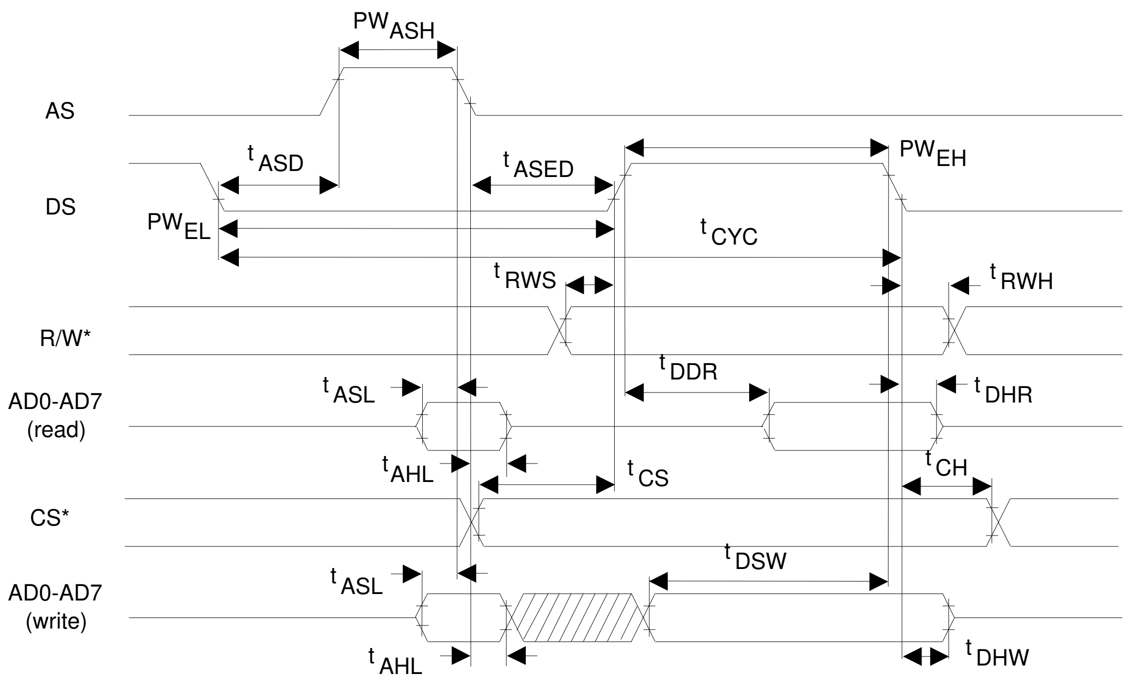
INTEL BUS READ AC TIMING (BTS=0 / MUX = 1) Figure 17-1



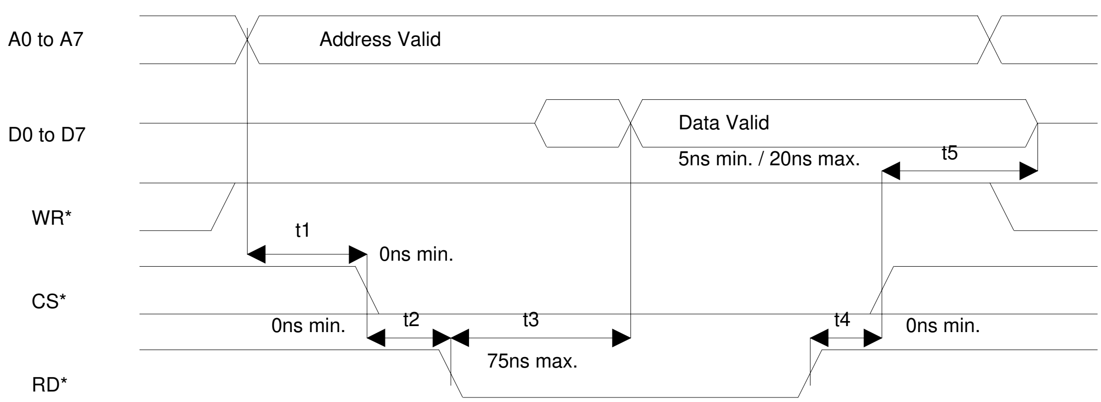
INTEL BUS WRITE TIMING (BTS=0 / MUX=1) Figure 17-2



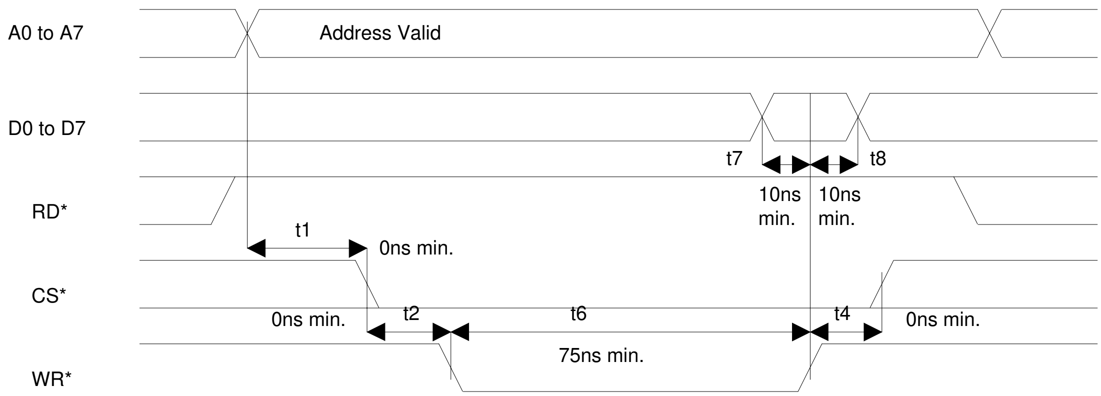
MOTOROLA BUS AC TIMING (BTS = 1 / MUX = 1) Figure 17-3



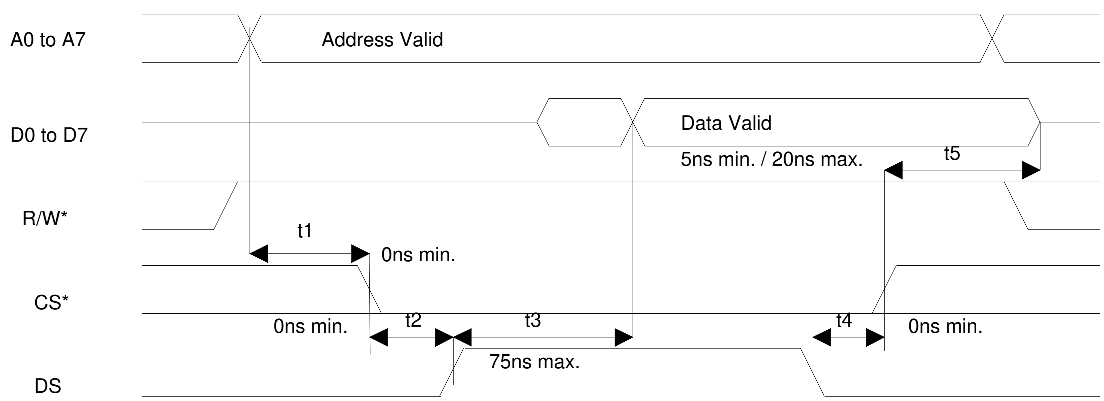
INTEL BUS READ AC TIMING (BTS=0 / MUX=0) Figure 17-4



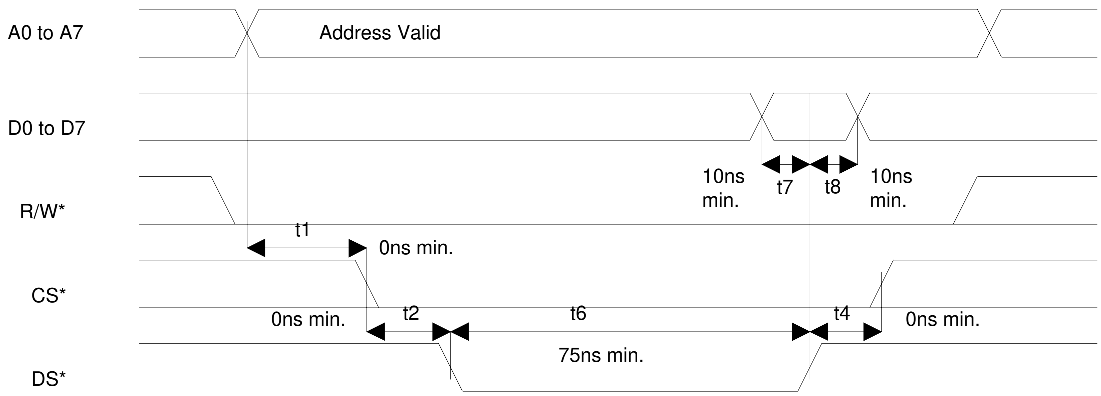
INTEL BUS WRITE AC TIMING (BTS=0 / MUX=0) Figure 17-5



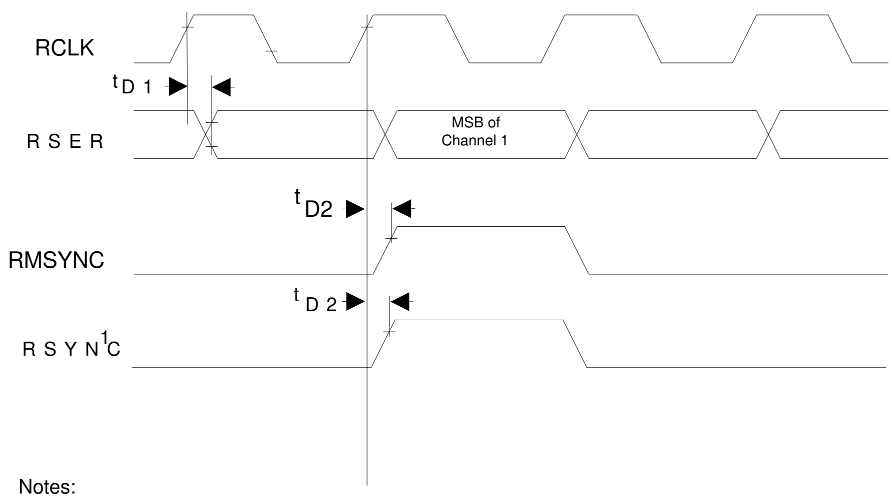
MOTOROLA BUS READ AC TIMING (BTS=1 / MUX=0) Figure 17-6



MOTOROLA BUS WRITE AC TIMING (BTS=1 / MUX=0) Figure 17-7

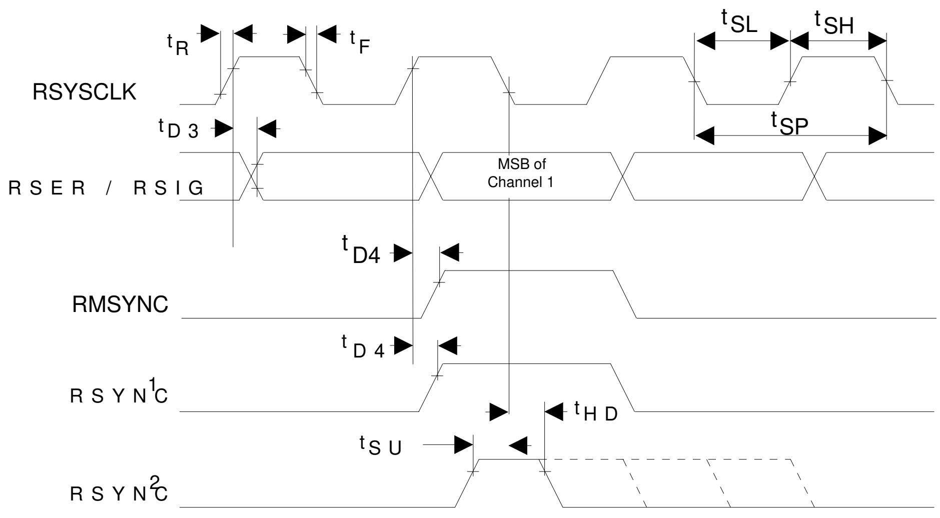


RECEIVE SIDE AC TIMING Figure 17-8



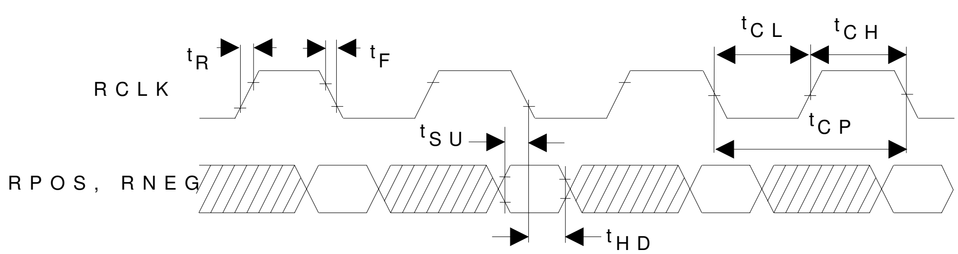
Notes:
1. RSYNC is in the output mode (RCR1.5 = 0).

RECEIVE SYSTEM SIDE AC TIMING Figure 17-9

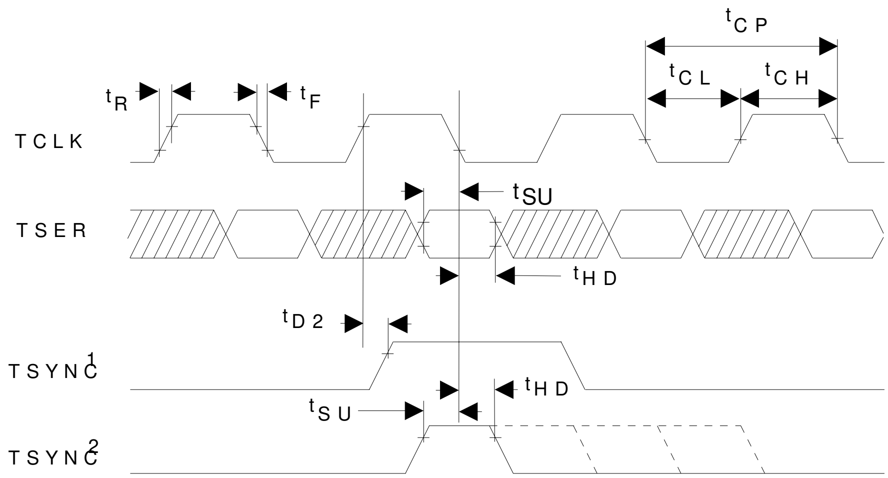


Notes:
1. RSYNC is in the output mode (RCR1.5 = 0)
2. RSYNC is in the input mode (RCR1.5 = 1)

RECEIVE LINE INTERFACE AC TIMING Figure 17-10

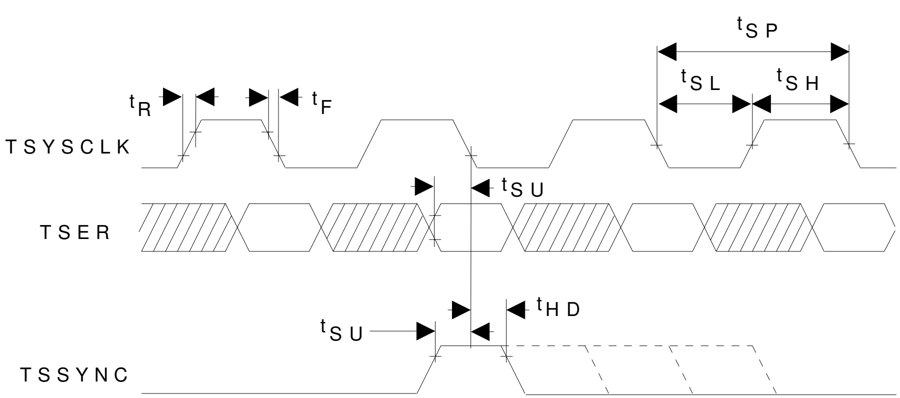


TRANSMIT SIDE AC TIMING Figure 17-11



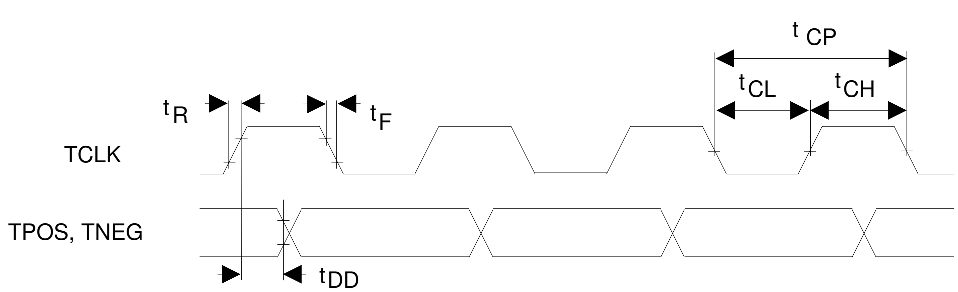
Notes:
1. TSYNC is in the output mode (TCR1.0 = 1).
2. TSYNC is in the input mode (TCR1.0 = 0).
3. TSER is sampled on the falling edge of TCLK when the transmit side elastic store is disabled.

TRANSMIT SYSTEM SIDE AC TIMING Figure 17-12

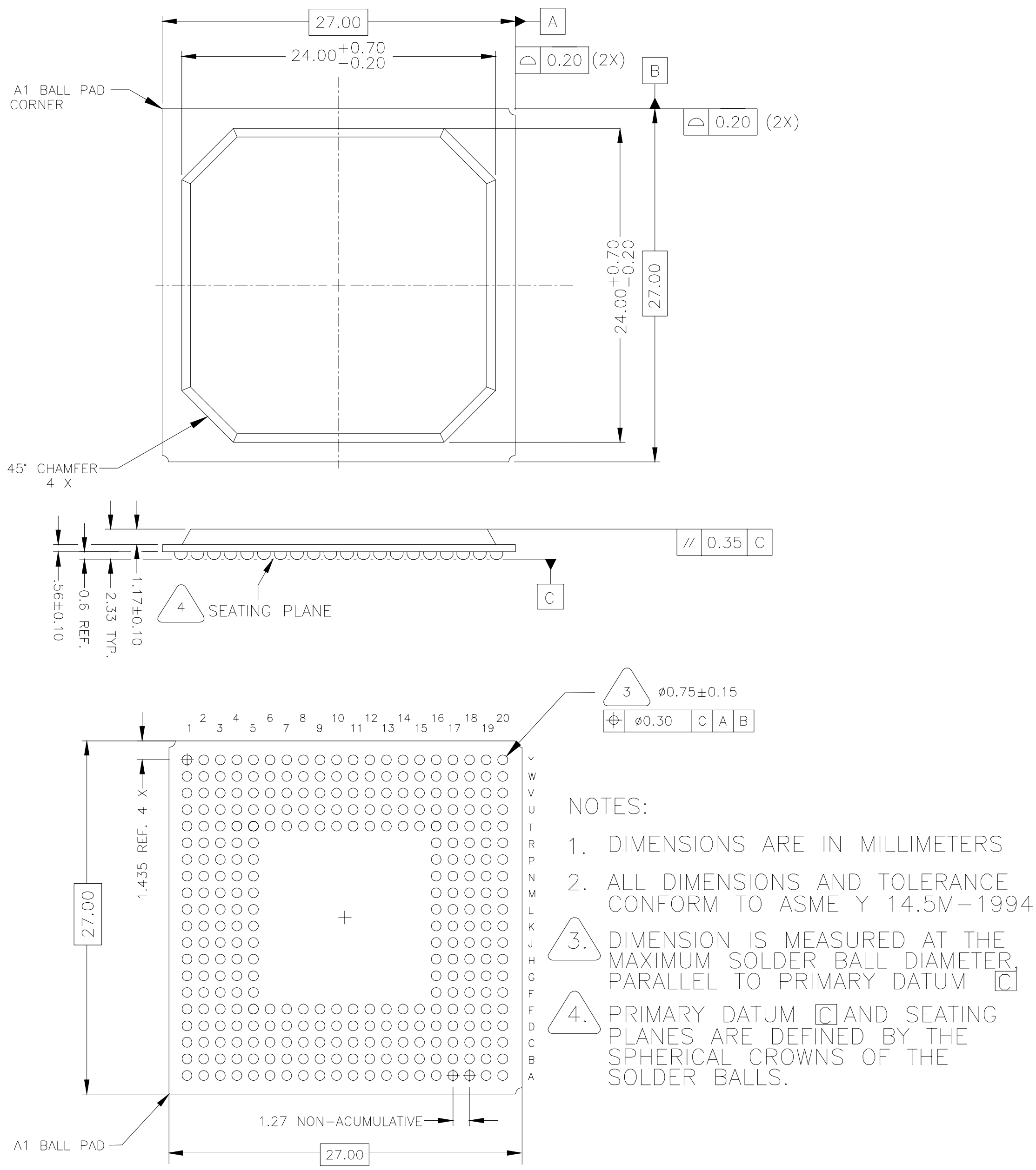


Notes:
1. TSER is only sampled on the falling edge of TSYSCLK when the transmit side elastic store is enabled.

TRANSMIT LINE INTERFACE SIDE AC TIMING Figure 17-13



18. DS21FT40 MECHANICAL DIMENSIONS



POWER SUPPLY DE-COUPLING

In a typical PCB layout for the MCM, all of the VDD pins will connect to a common power plane and all the VSS lines will connect to a common ground plane. The recommended method for de-coupling is shown below in both schematic and pictorial form. As shown in the pictorial, the capacitors should be symmetrically located about the device. Figure 18-1 uses standard capacitors, two .47 uf ceramics and two .01uf ceramics. Since VDD and VSS signals will typically pass vertically to the power and ground planes of a PCB, the de-coupling caps must be placed as close to the DS21FT40 as possible and routed vertically to power and ground planes.

De-coupling scheme using standard tantalum caps. Figure 18-1