ANALOG DEVICES

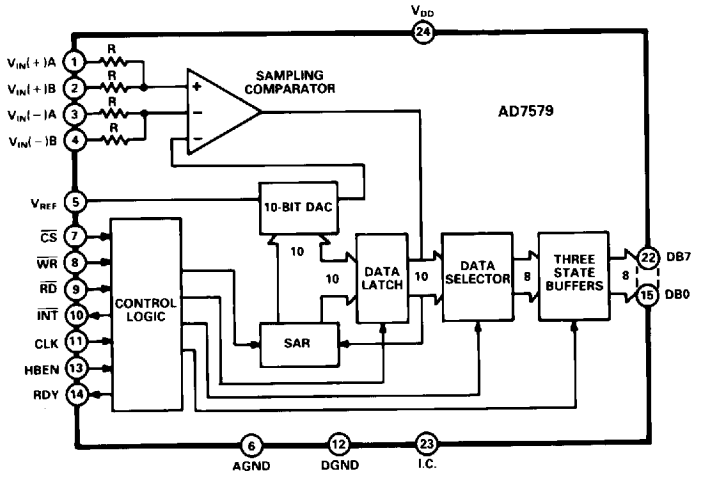
LC²MOS 10-Bit Sampling A/D Converters

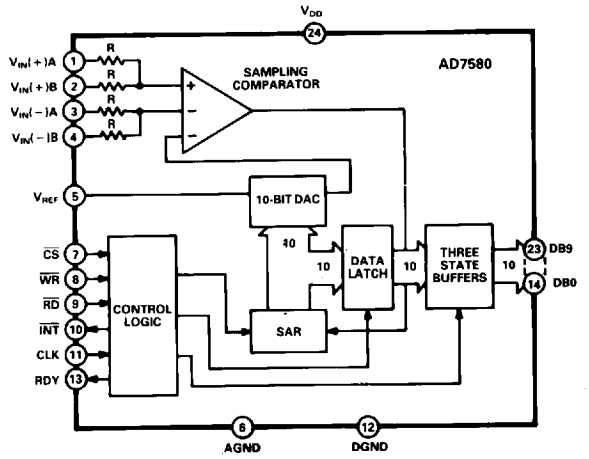
AD7579/AD7580

FEATURES

20μs Conversion Time
On-Chip Sample-Hold
50kHz Sampling Rate
25kHz Full-Power Input Bandwidth
Choice of Data Formats
Single +5V Supply
Low Power (50mW)
Skinny 24-Pin DIP and 28-Terminal Surface Mount Packages

FUNCTIONAL BLOCK DIAGRAMS





GENERAL DESCRIPTION

The AD7579 and AD7580 are 10-bit, successive approximation ADCs. They have differential analog inputs that will accept unipolar or bipolar input signals while operating from only a single +5V supply. Input ranges of 0 to +2.5V, 0 to +5V and ±2.5V are possible with no external signal conditioning. Only an external 2.5V reference and clock and control signals are required to make them operate.

With conversion time of less than 20μs and an on-chip sample-hold amplifier, the devices are ideally suited for digitizing ac signals. The maximum sampling rate is 50kHz, giving an input bandwidth of 25kHz. The parts are specified not only with traditional static specifications such as linearity and offset but also with dynamic specifications (SNR, Harmonic Distortion, IMD).

The AD7579 and AD7580 are microprocessor-compatible with standard microprocessor control inputs ($\overline{CS}$, $\overline{RD}$, $\overline{WR}$, RDY, $\overline{INT}$) and data outputs capable of interfacing to high-speed data buses. There is a choice of data formats, with the AD7579 offering an (8+2) read and the AD7580 offering a 10-bit parallel word.

Space saving and low power are also features of these devices. They dissipate less than 50mW from a single +5V supply and are offered in a 0.3", 24-pin package and in plastic/ceramic chip carrier for surface mounting.

PRODUCT HIGHLIGHTS

1. 20μs conversion time with on-chip sample-hold makes the AD7579 and AD7580 ideal for audio and higher bandwidth signals, e.g., modem applications.
2. Differential analog inputs can accept unipolar or bipolar input signals, but only a single, +5V power supply is needed.
3. Versatile and easy-to-use digital interface has fast bus access/relinquish times, allowing connection to most popular microprocessors.

REV. A

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AD7579/AD7580—SPECIFICATIONS

(V_{DD} = +5V ± 5%, V_{REF} = +2.5V, AGND = DGND = 0V; f_{CLK} = 2.5MHz; All specifications T_{MIN} to T_{MAX} unless otherwise noted. Test conditions as in Figure 12 unless otherwise stated).

Parameter	J, A Versions	K, B Versions	S Version	Units	Conditions/Comments
STATIC CHARACTERISTICS					These specifications apply for the
Resolution	10	10	10	Bits	three Analog Input Ranges. See Differential Applications.
Integral Nonlinearity	± 1	± 1/2	± 1	LSB max	No missing codes guaranteed over the
Differential Linearity Error	± 0.9	± 0.9	± 0.9	LSB max	full temperature range[2].
Full-Scale Error	± 5	± 5	± 5	LSB max	
Zero Code Error[3]	± 2	± 1	± 2	LSB max	Connected as in Figure 12.
	± 3	± 2	± 3	LSB max	Connected as in Figure 14 or 15.
Power Supply Rejection	± 0.5	± 0.5	± 0.5	LSB max	4.75V<V_{DD}<5.25V
DYNAMIC CHARACTERISTICS[4,5]					
Conversion Time[6]	16.9	16.9	16.9	µs min	f_{CLK} = 2.5MHz, t_{WR} = 100ns.
	18.5	18.5	18.5	µs max	See Functional Description.
Sampling Rate	50	50	50	kHz max	
Clock Range	250/2.5	250/2.5	250/2.5	kHz min/MHz max	
Signal-to-Noise Ratio	55	55	55	dB min	See Terminology. T_A = 25°C.
	58	60	58	dB typ	
Total Harmonic Distortion	−58	−58	−58	dB max	T_A = 25°C.
	−64	−68	−64	dB typ	
Intermodulation Distortion	−67	−67	−67	dB typ	This is characterized to both SMPTE and CCITT standards. T_A = 25°C.
Slew Rate	160	160	160	mV/µs max	See Terminology
ANALOG INPUT RANGES[7]					
Figure 12					AD7579/AD7580 connected as in Figure 12
Span	V_{REF}	V_{REF}	V_{REF}	V max	
Common-Mode Range	0 to V_{DD}	0 to V_{DD}	0 to V_{DD}	V max	
CMRR	0.5	0.5	0.5	LSB/V typ	
Figure 14					AD7579/AD7580 connected as in Figure 14
Span	$2V_{REF}$	$2V_{REF}$	$2V_{REF}$	V max	
Common-Mode Range	0 to $2V_{DD}$	0 to $2V_{DD}$	0 to $2V_{DD}$	V max	
CMRR	0.5	0.5	0.5	LSB/V typ	
Figure 15					AD7579/AD7580 connected as in Figure 15
Span	$2V_{REF}$	$2V_{REF}$	$2V_{REF}$	V max	
Common-Mode Range	$-V_{REF}$ to ($2V_{DD}-V_{REF}$)	$-V_{REF}$ to ($2V_{DD}-V_{REF}$)	$-V_{REF}$ to ($2V_{DD}-V_{REF}$)	V max	
CMRR	0.5	0.5	0.5	LSB/V typ	
ATTENUATOR INPUT RESISTANCE	5/15	5/15	5/15	kΩ min/kΩ max	10kΩ typical. Resistance measured between $V_{IN}(+)A$, $V_{IN}(+)B$ or $V_{IN}(-)A$, $V_{IN}(-)B$
COMPARATOR INPUT RESISTANCE	10	10	10	MΩ min	AD7579/AD7580 connected as in Figure 12
REFERENCE INPUT					
V_{REF} (For Specified Performance)	+2.5	+2.5	+2.5	V	± 5%
I_{REF}	1.5	1.5	1.5	mA max	
LOGIC INPUTS					
$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, HBEN, CLK					
V_{INL}, Input Low Voltage	0.8	0.8	0.8	V max	
V_{INH}, Input High Voltage	2.4	2.4	2.4	V min	
I_{IN}, Input Current					
25°C	± 1	± 1	± 1	µA max	V_{IN} = 0 or V_{DD}
T_{min} to T_{max}	± 10	± 10	± 10	µA max	V_{IN} = 0 or V_{DD}
C_{IN}, Input Capacitance[4]	10	10	10	pF max	
LOGIC OUTPUTS					
DB0 to DB7 (DB9)					
V_{OL}, Output Low Voltage	0.4	0.4	0.4	V max	I_{SINK} = 1.6mA
V_{OH}, Output High Voltage	4.0	4.0	4.0	V min	I_{SOURCE} = 400µA
Floating State Leakage Current	± 1	± 1	± 10	µA max	V_{OUT} = 0 to V_{DD}
Floating State Output Capacitance[4]	10	10	10	pF max	
RDY, $\overline{INT}$					
V_{OL}, Output Low Voltage	0.4	0.4	0.4	V max	I_{SINK} = 1.6mA
POWER REQUIREMENT					
V_{DD}	+5	+5	+5	V	± 5% for Specified Performance
I_{DD}	10	10	10	mA max	Typically 5mA with V_{DD} = +5V
Power Dissipation	50	50	50	mW max	

NOTES

[1]Temperature Ranges as follows:
J, K Versions; 0 to +70°C
A, B Versions; −25°C to +85°C
S Version; −55°C to +125°C

[2]Zero code error and gain error adjusted to zero.

[3]Zero code error is measured with respect to an ideal first code transition which occurs at 1/2LSB.

[4]Sample tested at 25°C to ensure compliance.

[5]These specifications apply for full-scale input signals up to 20kHz.

[6]Accuracy may degrade at conversion times other than those specified.

[7]$V_{IN}(+)$ must always be equal to or more positive than $V_{IN}(-)$, in Figures 12, 14, 15.

Specifications subject to change without notice.

TIMING SPECIFICATIONS[1]

Parameter[2,3,4]	Limit at 25°C (All Grades)	Limit at T_{min}, T_{max} (J, K, A, B Grades)	Limit at T_{min}, T_{max} (S Grade)	Units	Test Conditions/Comments
t_1	0	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Setup Time
t_2	40	50	50	ns min	$\overline{WR}$ Pulse Width
t_3	0	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Hold Time
t_4	100	100	120	ns max	$\overline{WR}$ to $\overline{INT}$ Propagation Delay
t_5	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_6	t_{12}	t_{12}	t_{12}	ns min	$\overline{RD}$ Pulse Width
t_7	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_8	20	20	30	ns min	HBEN to $\overline{RD}$ Setup Time
t_9	10	10	10	ns min	HBEN to $\overline{RD}$ Hold Time
t_{10}	110	135	150	ns min	RDY Access Time
t_{11}	100	100	120	ns max	$\overline{RD}$ to $\overline{INT}$ Propagation Delay
t_{12}	110	135	150	ns max	Data Access Time After $\overline{RD}$
t_{13}	10	10	10	ns min	Data Hold Time, RDY Hold Time
	65	80	90	ns max	

NOTES
1. Timing specifications are sample tested at +25°C to ensure compliance. All input control signals are specified with $t_R = t_F = 20$ns (10% to 90% of +5V) and timed from a voltage level of +1.6V.
2. t_4, t_{10}, t_{11} and t_{12} are measured with the load circuits of Figures 3 and 5 and defined as the time required for an output to cross 0.8V or 2.4V.
3. t_{13} is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 4.
4. $\overline{INT}$ and RDY are open-drain outputs and need 3kΩ external pull-up resistors for operation.

Specifications subject to change without notice.

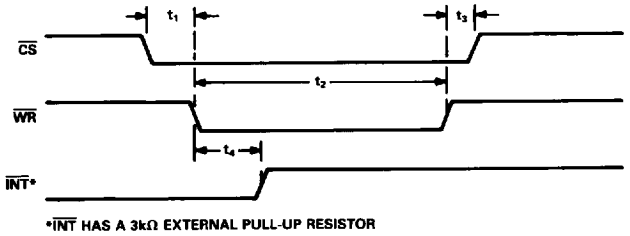


Figure 1. AD7579/AD7580 Start Cycle Timing

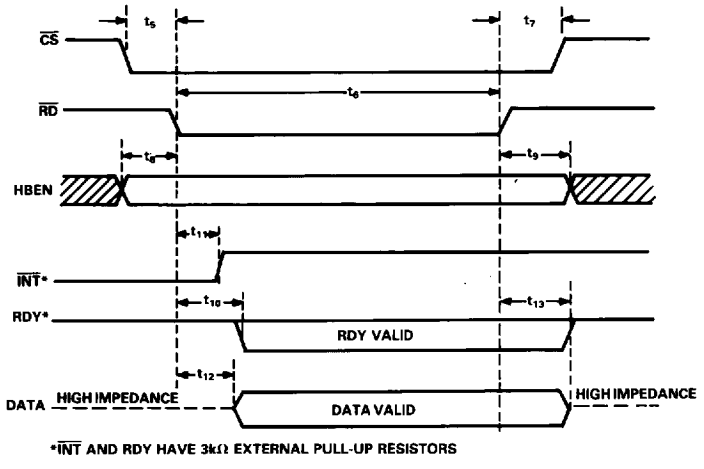
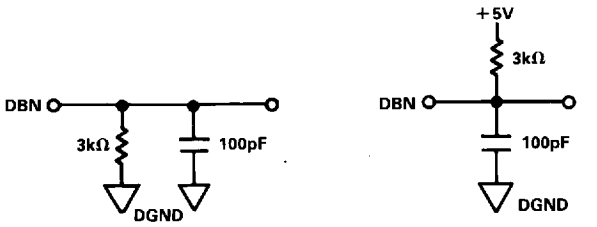


Figure 2. AD7579/AD7580 Read Cycle Timing

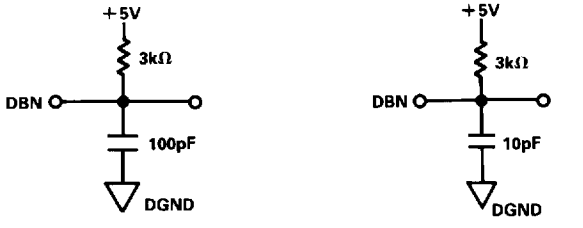


a. High-Z to V_{OH} *b. High-Z to V_{OL}*

Figure 3. Load Circuits for Access Time Tests (t_{12})

a. V_{OH} to High-Z *b. V_{OL} to High-Z*

Figure 4. Load Circuits for Output Float Delay (t_{13})



a. High-Z to V_{OL} *b. V_{OL} to High-Z*

Figure 5. Load Circuit for $\overline{INT}$ Propagation Delays

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to AGND	−0.3V to +7V
V_{DD} to DGND	+0.3V to +7V
AGND to DGND	−0.3V, V_{DD}
Digital Input Voltage to DGND	−0.3V, V_{DD} +0.3V
Digital Output Voltage to DGND	−0.3V, V_{DD} +0.3V
CLK Input Voltage to DGND	−0.3V, V_{DD} +0.3V
V_{REF} to AGND	−0.3V, V_{DD}
$V_{IN}(+)A$, $V_{IN}(+)B$ to AGND (Figure 12)	−0.3V, V_{DD} +0.3V
$V_{IN}(-)A$, $V_{IN}(-)B$ to AGND (Figure 12)	−0.3V, V_{DD} +0.3V
$V_{IN}(+)A$ to AGND (Figure 14)	$-0.6V, 2V_{DD}$ +0.6V
$V_{IN}(-)A$ to AGND (Figure 14)	$-0.6V, 2V_{DD}$ +0.6V
$V_{IN}(+)A$ to AGND (Figure 15)	$-V_{REF}$ −0.6V, $2V_{DD} - V_{REF}$ +0.6V
$V_{IN}(-)A$ to AGND (Figure 15)	$-V_{REF}$ −0.6V, $2V_{DD} - V_{REF}$ +0.6V
Operating Temperature Range	
Commercial (J, K Versions)	0 to +70°C
Industrial (A, B Versions)	−25°C to +85°C
Extended (S Version)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10sec)	+300°C
Power Dissipation (Any Package) to +75°C	450mW
Derates Above +75°C by	6mW/°C

*Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

TERMINOLOGY

LEAST SIGNIFICANT BIT (LSB)

An ADC with 10-bit resolution can resolve one part in 2^{10} (1/1024 of full scale). For the AD7579/AD7580 operating in the unipolar range with 2.5V span, one LSB is 2.44mV.

ZERO CODE ERROR

This is a measure of the difference between the ideal (0.5LSB) and the actual differential analog input level required to produce the first positive LSB code transition (00 . . . 00 to 00 . . . 01).

FULL-SCALE ERROR

The ideal difference between the first transition voltage and last transition voltage for an ADC is (F.S. − 2LSB). AD7579/AD7580 Full-Scale Error is defined as the deviation between this ideal difference and the measured difference.

COMMON-MODE RANGE

The voltage at both inputs to the AD7579/AD7580 can be raised above or lowered below analog ground potential, providing $V_{IN}(+)$ is equal to or more positive than $V_{IN}(-)$. Figures 12, 14, and 15 show circuits for various Analog Input Ranges. The Common-Mode Range represents the voltage extremes which can be applied to the circuits of Figure 12, 14 or 15. For example, when the AD7579/AD7580 is connected as in Figure 15, the Common-Mode Range is −2.5V to +7.5V.

SLEW RATE

Slew Rate is the maximum allowable rate of change of input signal such that the digital sample values are not in error. The Slew Rate performance of AD7579/AD7580 allows sampling of an input full-scale (2.5V pk-pk) sine wave up to 20kHz.

SIGNAL-TO-NOISE RATIO

Signal-to-Noise Ratio (SNR) is measured signal to noise at the output of the ADC. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency. SNR is dependent on the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical SNR for a sine-wave input is given by:

$$SNR = (6.02N + 1.76)\ dB,$$

where N is the number of bits in the ADC. Thus for an ideal 10-bit ADC, SNR = 62dB.

INTERMODULATION DISTORTION

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products, of order (m + n), at sum and difference frequencies of mfa ± nfb, where m,n = 0,1,2,3,----. Intermodulation terms are those for which m or n is not equal to zero.

HARMONIC DISTORTION

Harmonic distortion is the ratio of the square root of the sum-of-the-squares of the rms values of the harmonics to the rms value of the fundamental. For the AD7579/AD7580, Harmonic Distortion is:

$$20 \log \frac{\sqrt{(V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2)}}{V_1}\ dB,$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5, V_6 are the rms amplitudes of the individual harmonics.

ORDERING GUIDE

Model[1, 2]	Temperature Range	INL	Package Option[3]
AD7579JN	0°C to +70°C	±1LSB	N-24
AD7579KN	0°C to +70°C	±1/2LSB	N-24
AD7579JP	0°C to +70°C	±1LSB	P-28A
AD7579KP	0°C to +70°C	±1/2LSB	P-28A
AD7579AQ	−25°C to +85°C	±1LSB	Q-24
AD7579BQ	−25°C to +85°C	±1/2LSB	Q-24
AD7579SQ	−55°C to +125°C	±1LSB	Q-24
AD7579SE	−55°C to +125°C	±1LSB	E-28A

NOTES
[1]Analog Devices reserves the right to ship ceramic (D-24A) in lieu of cerdip (Q-24) hermetic packages.
[2]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheet.
[3]D = Ceramic DIP; E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip. For outline information see Package Information section.

Model[1, 2]	Temperature Range	INL	Package Option[3]
AD7580JN	0°C to +70°C	±1LSB	N-24
AD7580KN	0°C to +70°C	±1/2LSB	N-24
AD7580JP	0°C to +70°C	±1LSB	P-28A
AD7580KP	0°C to +70°C	±1/2LSB	P-28A
AD7580AQ	−25°C to +85°C	±1LSB	Q-24
AD7580BQ	−25°C to +85°C	±1/2LSB	Q-24
AD7580SQ	−55°C to +125°C	±1LSB	Q-24
AD7580SE	−55°C to +125°C	±1LSB	E-28A

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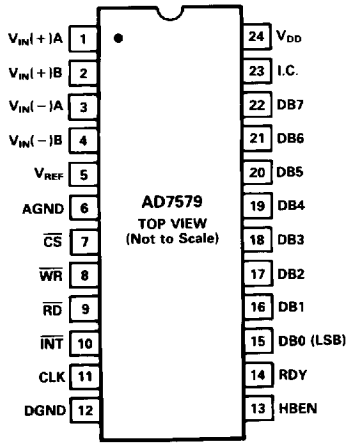
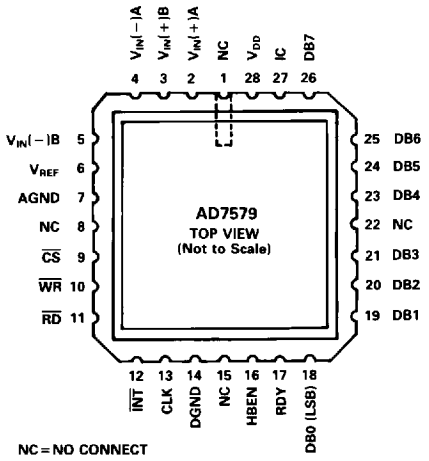
[3]D = Ceramic DIP; E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip. For outline information see Package Information section.

PIN CONFIGURATIONS

DIP

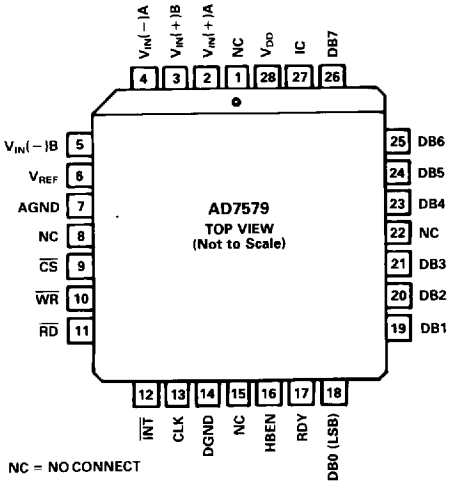


LCCC

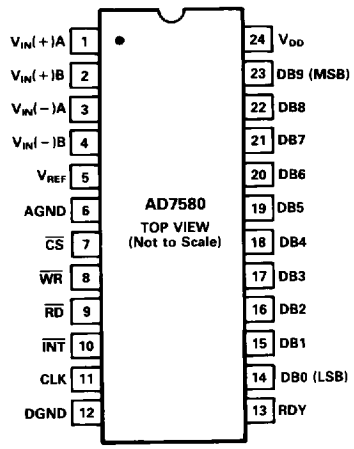


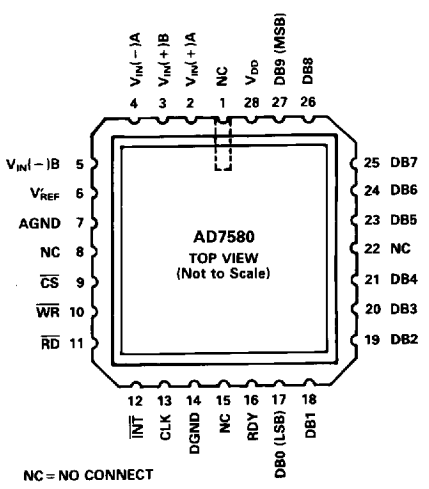
NC = NO CONNECT

PLCC

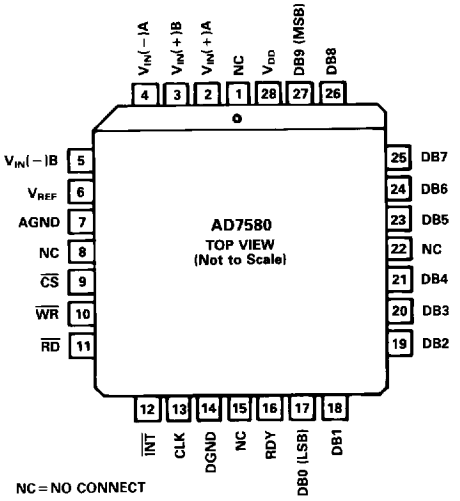


NC = NO CONNECT





NC = NO CONNECT



NC = NO CONNECT

PIN FUNCTION DESCRIPTION (DIP PACKAGE)

Mnemonic	Pin Number AD7579	Pin Number AD7580	Description
$V_{IN}(+)A$	1	1	Analog Input Pin.
$V_{IN}(+)B$	2	2	Analog Input Pin.
$V_{IN}(-)A$	3	3	Analog Input Pin.
$V_{IN}(-)B$	4	4	Analog Input Pin. The four analog input pins connect to the on-chip input attenuator (see Figure 6) and may be configured as in Table I for various input ranges.
V_{REF}	5	5	V_{REF} Input. This is nominally +2.5V.
AGND	6	6	Analog Ground
$\overline{CS}$	7	7	Chip Select Input.
$\overline{WR}$	8	8	Write Input. Used with $\overline{CS}$ to start conversion. See Tables II, III.
$\overline{RD}$	9	9	Read Input. Used with $\overline{CS}$ to read data. See Tables II, III.
$\overline{INT}$	10	10	Open Drain Output. High impedance during conversion. Goes low when conversion is complete.
CLK	11	11	Clock Input.
DGND	12	12	Digital Ground.
HBEN	13	–	High Byte Enable Input. Used in AD7579 for 2 Byte Reading. See Tables II, IV. Either the High Byte or the Low Byte may be read first.
RDY	14	13	Open Drain Output. This is accessed during Read Cycle. When accessed, it is low during conversion and high impedance when conversion is complete.
DB0-DB7	15-22	–	Three-State Data Outputs on AD7579. The data format is right justified.
DB0-DB9	–	14-23	Three-State Data Outputs on AD7580.
I.C.	23	–	Internal connection. This pin is connected internally on the AD7579. It should be left open and not used as a feed-through pin in double-sided printed circuit boards.
V_{DD}	24	24	Positive Power Supply. This is +5V nominal.

Analog Input Range	Connections $V_{IN}(+)A$	$V_{IN}(+)B$	$V_{IN}(-)A$	$V_{IN}(-)B$	Analog Input Span	Common-Mode Range
Figure 12	$V_{IN}(+)$	$V_{IN}(+)$	$V_{IN}(-)$	$V_{IN}(-)$	2.5V	0V to +5V
Figure 14	$V_{IN}(+)$	AGND	$V_{IN}(-)$	AGND	5V	0V to +10V
Figure 15	$V_{IN}(+)$	V_{REF}	$V_{IN}(-)$	V_{REF}	5V	−2.5V to +7.5V

Table I. Analog Input Ranges

$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	HBEN	Function
1	X	X	X	Not Selected
0	1	1	X	Selected, WAIT for $\overline{WR}$, $\overline{RD}$
0	⊔	1	X	Start Conversion on ↓ of $\overline{WR}$
0	1	0	0	Enable ADC Data (8 LSBs)*
0	1	0	1	Enable ADC Data (2 MSBs)*

*Data is Right Justified.

Table II. AD7579 Truth Table

$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	Function
1	X	X	Not Selected
0	1	1	Selected, WAIT for $\overline{WR}$, $\overline{RD}$
0	⊔	1	Start Conversion on ↓ of $\overline{WR}$
0	1	0	Enable ADC data (10 Bits)

Table III. AD7580 Truth Table

HBEN	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
LOW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
HIGH	$\overline{EOC}$*	0	0	0	0	0	DB9	DB8

*$\overline{EOC}$ is an internal End of Conversion flag.

Table IV. AD7579 Output Data Format

CIRCUIT INFORMATION

ANALOG INPUT CIRCUITRY

The AD7579 is a 10-bit ADC with an (8+2) output bus structure designed for 8-bit microprocessor systems. The AD7580 is a 10-bit ADC with a 10-bit parallel output bus structure. The ADC circuitry is identical in both parts. Block diagrams are shown on the first page of this data sheet.

Figure 6 shows the input circuitry to the ADC comparator. This comparator has differential inputs which are accessed through the attenuator networks made up of resistors R. The attenuators can be used to scale and offset analog input voltages, and this is done in Figures 14 and 15 to alter the basic ADC input range. The analog inputs to the comparator are differential with the provisos that V+ is always greater than or equal to V−, V− is greater than or equal to AGND and that V+ is less than or equal to V_{DD}. These conditions must be satisfied when using the ADC in any of the voltage ranges.

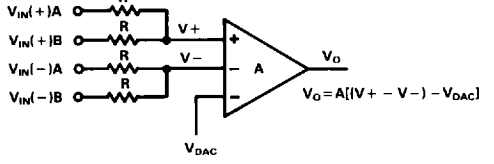


Figure 6. AD7579/AD7580 Input Circuit

Figure 7 shows an ac equivalent input circuit for the AD7579/AD7580 when used in the 2.5V Unipolar Mode of Figure 12. The ADC comparator is a sampled data comparator and the input circuitry for this is represented by S_A, Req and C_A. Req is a combination of the switch-on resistance and the input impedance of the comparator. When conversion starts, $V_{IN}(+)$ is sampled for at least ($2t_{CLK}$ + t_{WR} + 200ns) before the comparator goes into the hold mode. This means that the analog input has a minimum of 1.1μs (f_{CLK} = 2.5MHz, t_{WR} = 100ns) to settle before the comparator makes a decision. By using the typical values in Figure 7 for R, Req and C_A, the input time constant is 50ns. Settling to ±1/4LSB in a 10-bit system takes 8.3 time constants or 415ns in this case. This means that $V_{IN}(+)$ has plenty of time to settle before the ADC comparison cycle begins. It is important to remember that any source resistance or source capacitance appearing at the input will also increase the settling time and this should be kept to a minimum in all cases.

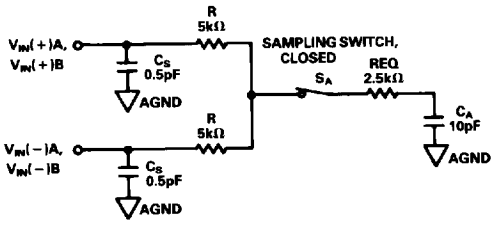


Figure 7. AD7579/AD7580 Equivalent Input Circuit During Sampling

With a 2.5MHz clock, the AD7579/AD7580 has a maximum conversion time of 18.5μs. If 1μs is allowed for reading the data outputs, the maximum sampling rate for the device is 50kHz. This means that the maximum analog input frequency is 25kHz according to the Nyquist theory. The ADC input impedance in the Unipolar Configuration of Figure 12 is 10MΩ. A medium bandwidth op amp will drive this at 25kHz. When the input attenuators are used for signal conditioning, the input impedance is 10kΩ. The drive requirements on the amplifier will now be greater but any errors resulting will be gain errors only. Suitable op amps for driving the AD7579/AD7580 in any of the input configurations are the AD711, AD OP-27, AD544. These will deliver specified device performance over the input bandwidth.

REFERENCE INPUT

The AD7579/AD7580 V_{REF} input is connected to the on-chip DAC. The input impedance of this is code dependent and the greatest variation occurs when the DAC resistors are at their lower limit. In this case, the impedance changes from 1.75kΩ to 5.25kΩ as the DAC is switched. To ensure that the error during conversion is less than 1/2LSB, the Reference output impedance should be less than 1Ω. References which satisfy this are the AD580 (shown in Figure 8) and the AD1403 from Analog Devices. If a trimmable reference such as the AD584 is used, it is possible to trim out the ADC full-scale error by adjusting the reference output.

INTERNAL SAMPLE-AND-HOLD

When an ADC without sample-and-hold is used to digitize ac signals, the analog input must not change by more than 1/2LSB during the conversion. This puts severe limitations on the allowable input signal bandwidth to such devices. A sample-and-hold amplifier must be used in front of the ADC if increased bandwidth is required. The charge balanced comparator used in the AD7579/AD7580 for the A/D conversion provides the user with an inherent sample-and-hold function. The ADC is specified to work with sampling rates up to 50kHz. This rate allows time to do a conversion and read the result into memory. Since at least two samples are needed to define an input sine wave according to the Nyquist theory, the analog input signal bandwidth for the AD7579/AD7580 is 25kHz. Figures 20, 21 and 22 show the performance of the ADC when digitizing ac signals.

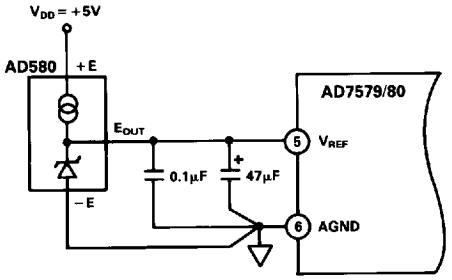


Figure 8. Using the AD580 as the Reference for the AD7579/AD7580

While the AD7579/AD7580 is converting, V+ (see Figure 6) is held and V− is being tracked. This limits the rate of change, $^{dv}/_{dt}$, on $V_{IN}(-)$. For example, if the Common-Mode frequency is 60Hz, then the allowable amplitude of this to introduce no more than 1/2LSB linearity error is 160mV pk-pk. As the Common-Mode frequency increases, this allowable amplitude decreases. Figure 9 shows how a 100mV pk-pk Common-Mode signal affects linearity error as its frequency is increased up to 1kHz.

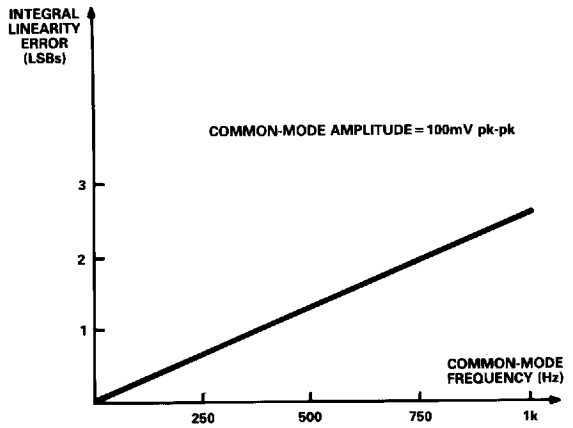


Figure 9. AD7579/AD7580 Error vs. Common-Mode Frequency

CLOCK INPUT

The AD7579/AD7580 is specified to operate with a 2.5MHz clock on the CLK input pin. This pin may be driven directly by CMOS or TTL buffers. The mark/space ratio on the clock can vary from 40/60 to 60/40. As the clock frequency is slowed down, it can result in slightly degraded accuracy performance. This is due to leakage effects on the hold capacitor in the internal sample-and-hold. Figure 10 is a typical plot of accuracy versus clock frequency for the ADC.

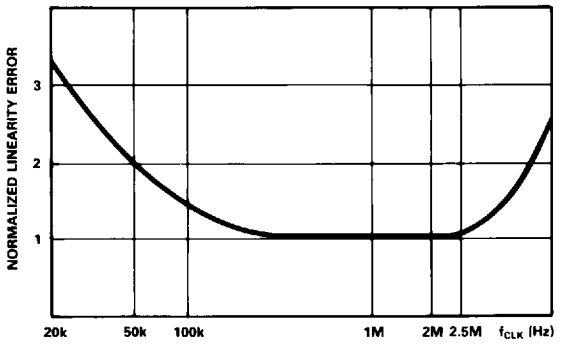


Figure 10. Normalized Linearity Error vs. Clock Frequency

FUNCTIONAL DESCRIPTION

Figure 11 shows the events sequence when the AD7579/AD7580 is converting. The device is selected when $\overline{CS}$ goes low and the first phase of conversion begins when $\overline{WR}$ goes low. This is an initializaton phase and causes the internal DAC to be set to full scale, comparators set to auto-zero and V+ (see Figure 6) to be sampled. The second phase begins some time after $\overline{WR}$ goes back high. This time can vary between 0 and 4 clock periods and depends on the state of an on-chip divide-by-4 counter which is used for internal synchronization. This is the start of the successive approximation procedure. V+ is held after 2-1/2 clock periods have elapsed. V− is sampled and the DAC output is switched into the comparator. There is $(1\text{-}1/2 \times t_{CLK})$ left for comparison and then the MSB result is latched. The MSB test takes 4 clock cycles as do each of the succeeding bit tests. Thus, the successive approximation always takes 40 clock cycles.

When all the bits have been tested, the SAR holds a 10-bit word representing the input signal. After a further 2 clock cycles this is transferred to a three state output latch, and three internal flag bits (RDY, $\overline{INT}$, $\overline{EOC}$) are set. The user can access the data outputs by bringing $\overline{RD}$ and $\overline{CS}$ low. RDY and $\overline{INT}$ are both open drain outputs with RDY accessed by $\overline{RD}$ and $\overline{INT}$ being permanently available. When $\overline{INT}$ is loaded with the circuit of Figure 5(a), it typically takes 60ns to reach V_{OL}. $\overline{EOC}$ is only available on the AD7579 (see Table V). It appears on DB7, when reading the high Byte.

When the ADC is finished the conversion, the conditions of V+, V− and the comparators are maintained and the ADC is now ready to start a new conversion. If $\overline{WR}$ and CLK are asynchronous, the total time from start to end of conversion is variable. Minimum conversion time is $(t_{WR} + 42\ t_{CLK})$, and maximum conversion time is $(t_{WR} + 46\ t_{CLK})$.

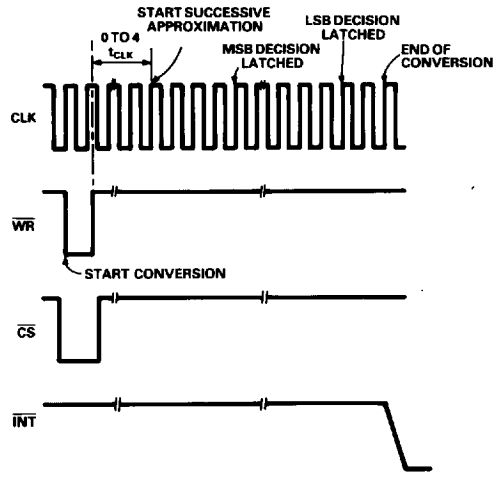


Figure 11. AD7579/AD7580 Conversion Sequence

APPLYING THE AD7579/AD7580

The AD7579/AD7580 has a flexible input stage consisting of two input attenuators. It is possible to realize various analog input ranges by reconfiguring these attenuators. The following diagrams show the ADC connected in the most popular configurations.

DIFFERENTIAL APPLICATIONS

Figure 12 shows the AD7579/AD7580 connected in the standard unipolar mode. Figure 13 and Table V show the ideal input/output

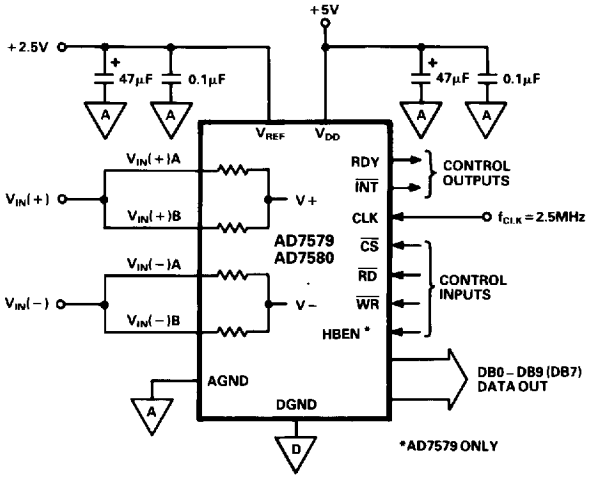


Figure 12. Unipolar 2.5V Operational Diagram

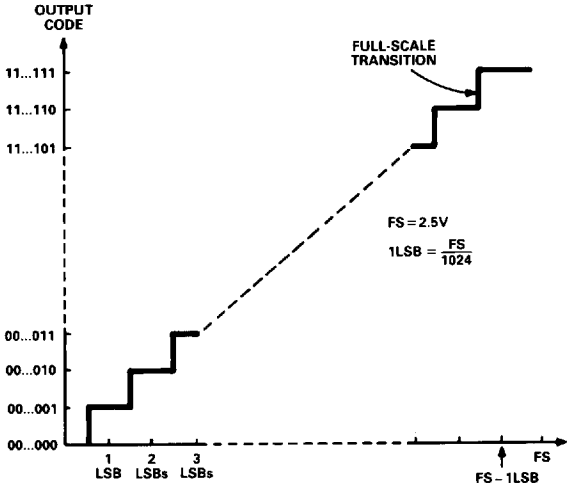


Figure 13. Ideal Input/Output Transfer Characteristic

Differential Analog Input, Volts	Digital Output DB9 DB0
+0.000	00 0000 0000
+0.00244	00 0000 0001
+1.24756	01 1111 1111
+1.25	10 0000 0000
+1.25244	10 0000 0001
+2.49512	11 1111 1110
+2.49756	11 1111 1111

Table V. Input/Output Code Table for Figure 12

transfer characteristic and the input/output code table respectively. Code transitions occur between successive integer LSB values (i.e., 1/2LSB, 3/2LSBs, etc.). The output code is straight binary with 1LSB = FS/1024 = 2.5/1024V = 2.4mV. The input voltage span is 2.5V and the common-mode range is 0V to +5V, when V_{DD} = 5V. This means that the lowest voltage which can be tolerated at any of the analog inputs is 0V, and the highest voltage which can be tolerated is +5V.

Figures 14 and 15 show the input attenuators on the AD7579/AD7580 configured to change the basic range of the device. A 5V range can be configured by grounding one end of each attenuator and applying the differential input to the other ends. This is shown in Figure 14. The span is 5V and the common-mode range is 0 to +10V. In Figure 15, one end of each attenuator is tied to V_{REF} (2.5V), and this allows each of the other legs to go to −2.5V without causing the comparator input to go negative. Assuming V_{REF} is 2.5V, the span of this circuit is 5V and the common-mode range is −2.5V to +7.5V. Note that reducing V_{DD} below 5 volts causes a corresponding reduction in CMR. See Specifications page for full details.

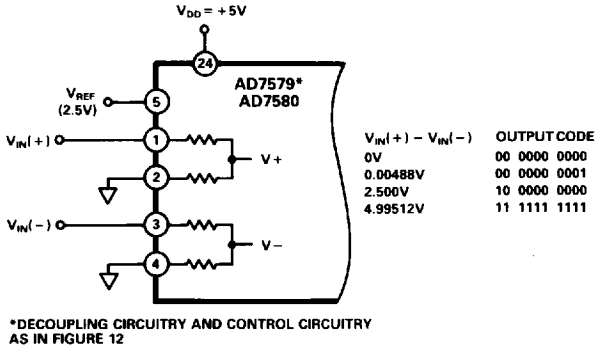


Figure 14. 5V Span with 0 to 10V CMR

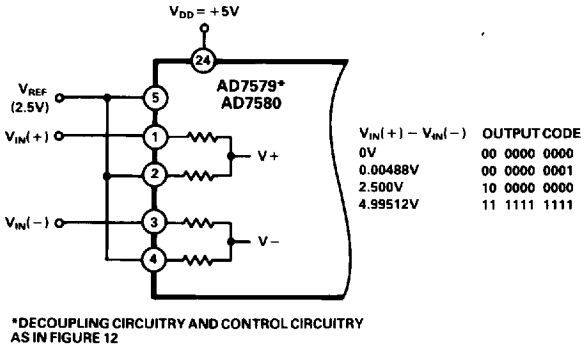


Figure 15. 5V Span with −2.5V to +7.5V CMR

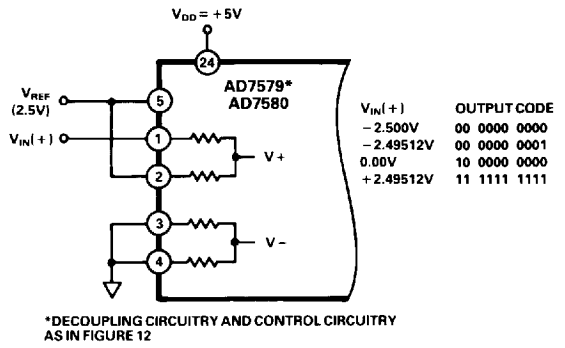


Figure 16. Single-Ended Bipolar Operation, −2.5V to +2.5V

SINGLE-ENDED APPLICATIONS

In many cases, users of the AD7579/AD7580 will want to measure single-ended input voltages (i.e., ground referred signals). The circuits of Figures 12, 14 and 15 can be easily adapted to accept such signals. If $V_{IN}(-)$ in Figure 12 is tied to AGND, then the analog input range is 0V to +2.5V. By connecting $V_{IN}(-)$ of Figure 14 to AGND, the analog input range becomes 0V to +5V. Figure 15 can be modified as in Figure 16 to accept input voltages in the range −2.5V to +2.5V. Each of these circuits are special cases of the Differential Input circuits and are achieved by making the negative input to the internal comparator equal to AGND.

OFFSET AND FULL-SCALE ADJUSTMENT

Figure 17 shows the AD7579/AD7580 connected in the single-ended Unipolar 2.5V range with offset and full-scale calibration circuitry. The zero error of the ADC is the deviation of the actual LSB transition from the ideal LSB transition. In many cases, the zero of the ADC will not need adjustment. When it does, R1 in Figure 17 provides 25mV of adjustment which is sufficient to null out both the op amp and ADC offset error. Resistors R3 and R4 bias $V_{IN}(-)$ to approximately 8mV and ensure that the offset error is never positive. This allows the error to be nulled in the single supply system of Figure 17. Apply +0.5LSB to V_{IN} and adjust R1 until the ADC output code flickers between 00 ..... 000 and 00 ..... 001.

For full-scale calibration, apply a voltage of (2.5V − 1.5LSB) to V_{IN}. Then adjust R2 until the output code flickers between 11 ..... 110 and 11 ..... 111. When the full-scale calibration is complete, return to the offset adjustment procedure and check that further adjustment is not necessary.

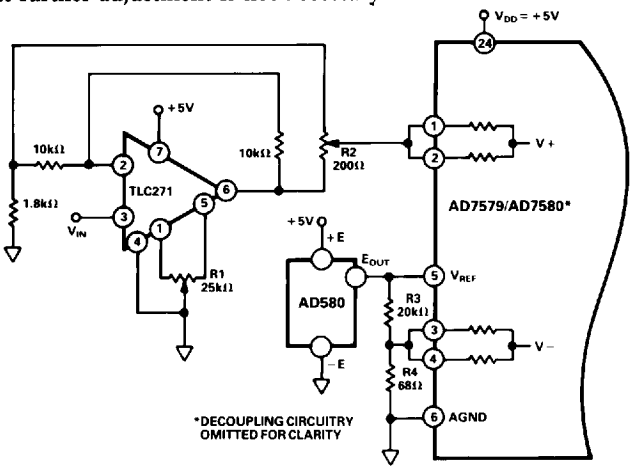


Figure 17. Offset and Full-Scale Calibration for Single-Ended Circuit

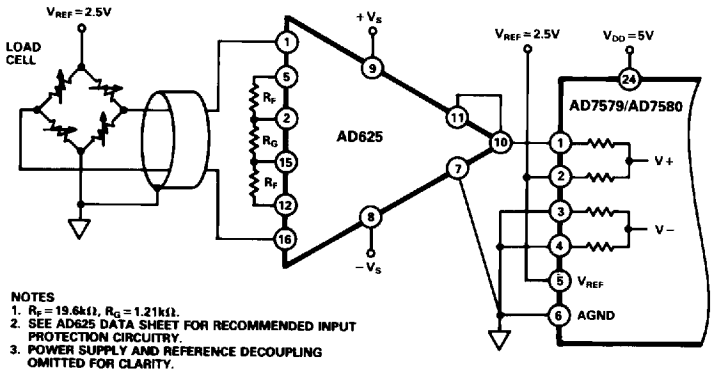


Figure 18a. AD7579/AD7580 and AD625 in a Data Acquisition System

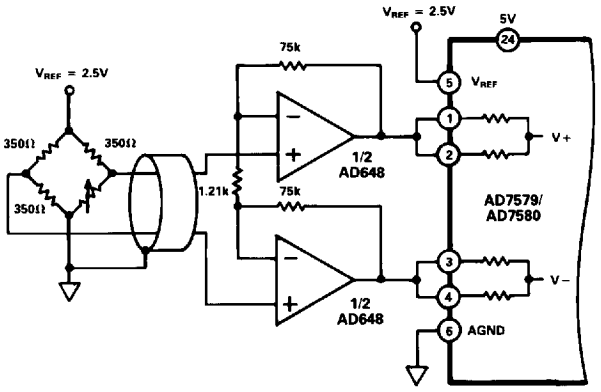


Figure 18b. AD7579/AD7580 and AD648 in a Data Acquisition System

AD7579/AD7580 IN DATA ACQUISITION SYSTEMS

The AD7579/AD7580 is suitable for many data acquisition circuits. Figure 18a shows one such circuit in which a load cell is used to produce a signal in response to an applied force. Typically these transducers produce 30mV full scale per volt of excitation. Since the excitation in this case is 2.5V, the output from the load cell is ±75mV when the maximum specified force is applied. The AD625 Instrumentation Amplifier is set for a gain of 33.33 which means that the input signal to the ADC is ±2.5V. Thus, the AD7579/AD7580 is configured in the single-ended, ±2.5V range of Figure 16. When no force is applied to the load cell, the ADC output will sit at mid-scale. With maximum negative force applied the ADC output will be all zeros; whereas, with maximum positive force the output will be all 1s. Offset and gain calibration of this system can be accomplished by trimming the offsets and gain of the instrumentation amplifier.

Figure 18b shows a differential transducer unbalanced by ≈10Ω supplying a 0 to 20mV maximum signal. The resistors are chosen for a gain of 125, and the ADC is configured to accept 0 to 2.5V differential signal. This is a lower-cost alternative to using an instrumentation amplifier.

Note that in the circuits of Figure 18, V_{REF} for the ADC and the excitation voltage for the load cell are both +2.5V. If the same reference drives both these points, then the ADC operation is ratiometric which eliminates system errors due to reference drift. The main reason why the same reference would not be used to drive both load cell and ADC is physical location. When the load cell is remote from the ADC circuitry, it might not be practical to have the same drive for both circuits.

APPLICATIONS HINTS

Layout: To obtain the best performance from the AD7579/AD7580, lay it out on a printed circuit board. Digital and analog lines on the board should be separated as much as possible. In particular, take care not to run any digital track adjacent to an analog signal track or underneath the AD7579/AD7580. The analog inputs should be screened by AGND.

Grounding: Establish a single-point analog ground (STAR ground) at Pin 6 (AGND) or as close as possible to the AD7579/AD7580. This is shown in Figure 19. Pin 12 (AD7579/AD7580 DGND) and all other analog grounds should be connected to this single analog ground point. However, do not connect any other digital grounds to this analog ground point. Low impedance analog and digital power supply returns are essential to low noise operation of the ADC and these tracks should be kept as wide as possible.

Noise: Input signal leads to $V_{IN}(+)A$, $V_{IN}(+)B$, $V_{IN}(-)A$, $V_{IN}(-)B$ and signal return leads from AGND (Pin 6) should be kept as short as possible to minimize input noise coupling. In applications where this is not possible a shielded cable between source and ADC is recommended.

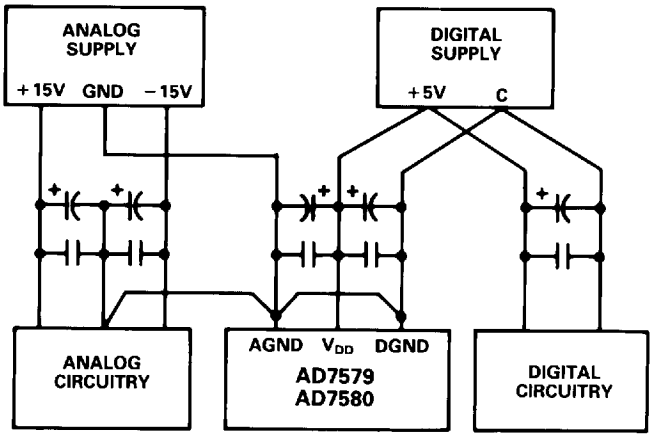


Figure 19. Power Supply Grounding Practice

DIGITAL SIGNAL PROCESSING APPLICATIONS

In Digital Signal Processing (DSP) application areas like voice recognition, echo cancellation and adaptive filtering, the dynamic characteristics (SNR, Harmonic Distortion, Intermodulation Distortion) of ADCs are critical. For this reason, the AD7579/AD7580 is specified dynamically as well as with standard D.C. specifications (linearity error, offset error, etc.).

Figure 20 shows a 2048 point FFT plot of an AD7579/AD7580 with an input signal of 3.58kHz. The SNR is 60.1dBs. The largest harmonic appears at $2f_O$ (7.16kHz) and is 70dB down from the fundamental. Harmonics above $3f_O$ are in the noise floor. Note that when SNR is calculated, it includes harmonics.

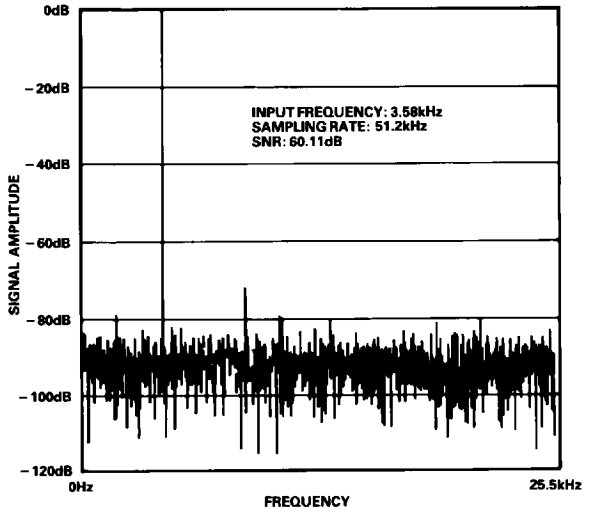


Figure 20. AD7579/AD7580 Spectral Response

If these were excluded the SNR figure would be closer to the ideal of 62dB for a 10-bit ADC. The relationship between Signal-to-Noise Ratio (SNR) and ADC resolution is expressed in the following equation:

$$SNR = (6.02N + 1.76)dB$$

This is for an ideal ADC with no differential or integral linearity errors. These errors will cause a degradation in SNR. By working backwards in the above equation it is possible to get a measure of ADC performance expressed in effective number of bits. This is shown over frequency in Figure 21 for the AD7579/AD7580. The effective number of bits typically falls between 9.7 and 9.8 corresponding to SNRs of 60.0 and 60.6dBs.

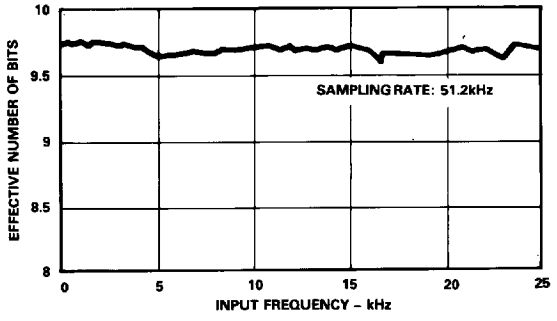


Figure 21. AD7579/AD7580 Effective Number of Bits

When a sine wave of specified frequency is applied to the AD7579/AD7580 and several thousand samples are taken, it is possible to plot a histogram showing the frequency of occurrence of each of 1024 ADC codes. A perfect ADC would produce a cusp probability density function described by the equation

$$p(V) = \frac{1}{(A^2 - V^2)^{1/2}}$$

A is the peak amplitude of the sine wave and p(V) the probability of occurrence at the voltage V. If a particular step is wider than the ideal width, then the code associated with that step will accumulate more counts than the code for an ideal step. Likewise, a step narrower than ideal width will have fewer counts. Missing codes are easily seen because a missing code means zero counts for a particular code. The absence of large spikes in the histogram indicates small differential nonlinearity. The actual histogram obtained is shown in Figure 22 and corresponds very well with the ideal cusp shape. It shows that the AD7579/AD7580 has very small differential nonlinearity and no missing codes with an input frequency of 25kHz.

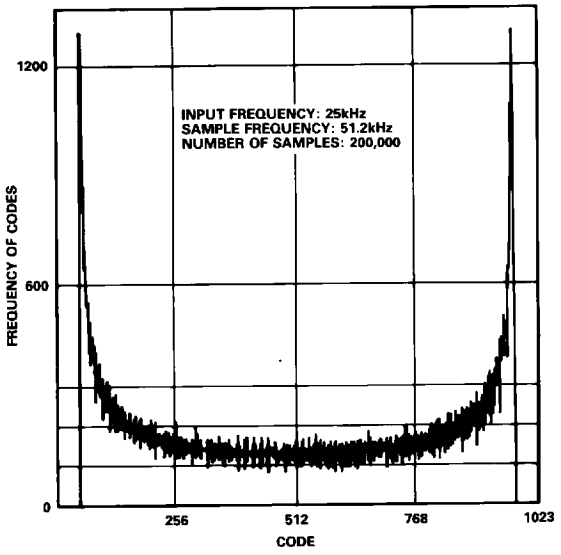


Figure 22. Histogram Plot for AD7579/AD7580

Whenever the AD7579/AD7580 is used to sample ac signals, it is essential that the signal sampling occurs at exactly equal intervals. This minimizes errors due to sampling uncertainty or jitter. The $\overline{WR}$ command for the AD7579/AD7580 needs to be synchronized with the CLK input to ensure equal interval sampling.

Two conditions must be satisfied to ensure proper synchronization: 1) The time interval between successive $\overline{WR}$ signals needs to be long enough to allow a conversion to finish and the data to be read into memory. 2) Because of the internal operation of the ADC, the number of clock pulses between successive write signals must be a multiple of four.

The conversion time for the AD7579/AD7580 has a maximum value of (t_{WR} + 46 t_{CLK}). If 4 t_{CLK} is allowed for reading the data outputs into a buffer then the interval between successive $\overline{WR}$ signals must be at least 50 t_{CLK}. The easiest way to satisfy both this requirement and number 2 above is to divide f_{CLK} by 64 to produce the $\overline{WR}$ signal. Alternatively, if a programmable timer/counter on a processor board is available, then it will be possible to easily divide f_{CLK} by 52.

MICROPROCESSOR INTERFACING

Reading Data

Conversion is started in the AD7579/AD7580 by bringing $\overline{WR}$ low. It is recommended that the user wait until conversion is complete before reading data. This can be achieved in any of the following ways:

1. Insert a software delay greater than the ADC conversion time between the conversion start instruction and the data read instructions.
2. Use the externally available $\overline{INT}$ signal to interrupt the microprocessor. This is an open drain output which goes low at the end of conversion.
3. On the AD7579, it is possible to interrogate the $\overline{EOC}$ status flag (See Table IV) to determine when conversion is complete. Reading may then proceed.

MC68000 Interface

Figure 23 shows an interface diagram for the AD7580 and the MC68000. The address decoding means that the AD7580 is a memory mapped device. For example, if the AD7580 is memory mapped as address COOOH, then a write instruction to this address will start a conversion, i.e.,

MOVE.W DO COOO

starts a conversion. When the conversion is complete, the MC68000 acquires the result by reading from COOOH, i.e.,

MOVE.W COOO, DO.

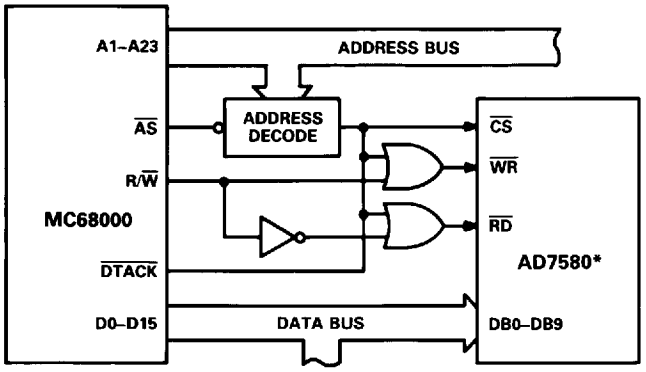


Figure 23. MC68000 to AD7580 Interface

8088 Interface

The AD7579, with its (8+2) data format, is ideal for use with the 8088 microprocessor. Figure 24 is the interface diagram. Again, a write instruction is required to start a conversion and a read at the end of conversion reads data into the processor. For the 8088 the appropriate instructions are:

MOV COOO, AX	Start a conversion
MOV AX, COO1	Read 2 MSBs of data
MOV AX, COOO	Read 8 LSBs of data

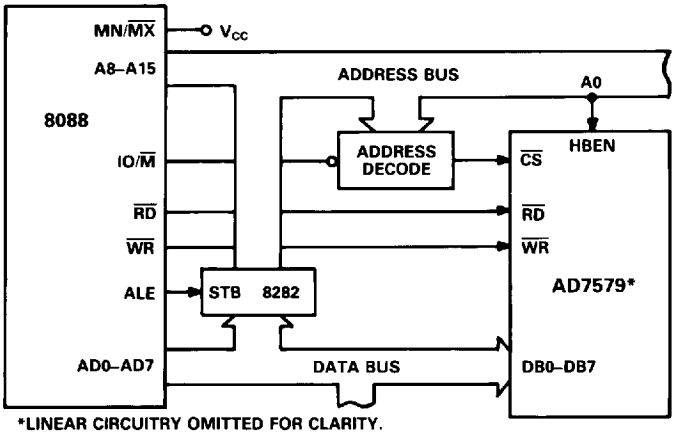


Figure 24. 8088 to AD7579 Interface

TMS32020 Interface

Figure 25 shows the AD7580 to TMS32020 interface. OUTA,PA starts a conversion and INA,PA reads data from the ADC when conversion is complete. PA is the Port Address.

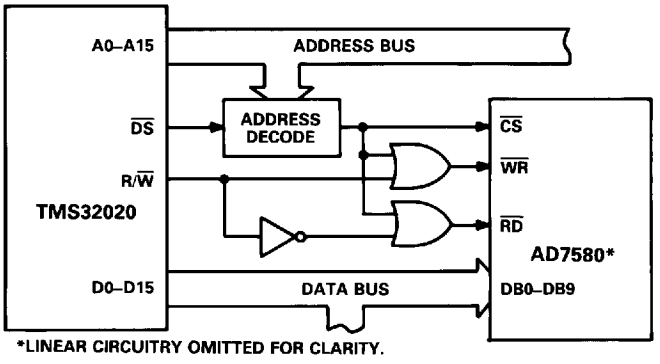


Figure 25. TMS32020 to AD7580 Interface

PRINTED CIRCUIT BOARD LAYOUT

Figure 26 is a circuit diagram showing the AD7579 or AD7580 being used to digitize an analog signal. The circuit board contains the ADC, reference, and a grid where the user can add additional circuitry. If the AD7580 is used, then links L6 and L8 should be inserted; and if AD7579 is used, L7 should be inserted with L6 and L8 omitted. Note that Pins 13 to 23 are not labelled. Depending on which ADC is used the function of these pins changes. See the Pin Function Description section for full details.

Links L1 to L5 at the analog input allow the user to choose various analog input ranges. With L1, L2 and L3 in place and the others omitted, the input range is 0V to +2.5V. Omitting L3 allows the user to measure input voltages which have a common-mode signal. The 0V to +5V range is achieved by inserting L2, L3 and L4 and omitting L1 and L5. With L2, L3 and L5 in place and L1, L4 omitted, the Analog input range is −2.5V to +2.5V.

IC2 (AD580) provides the +2.5V reference for the ADC. All the input and output control signals enter and leave the board through J1, which can be a Eurocard connector or a standard edge connector. Resistors R1 and R2 are the pull-ups required for the RDY and $\overline{INT}$ open-drain outputs. Note that the complete circuit operates from a +5V power supply.

The printed circuit board layout is shown in Figures 27 and 28. Figure 27 is the component side layout and Figure 28 is the solder side layout. The component overlay is shown in Figure 29.

In the layout, the AD580 is kept as close to the AD7579/AD7580 as possible. The STAR ground point is located at Pin 6 (AGND) of the ADC. Pin 12 (DGND), reference ground and the analog ground plane are connected to this point.

To ensure optimum performance, the AD7579/AD7580 power supply is decoupled with C1 and C2. The V_{REF} input to the ADC is decoupled with C3 and C4. Note how all the decoupling capacitors are placed as close as possible to the ADC.

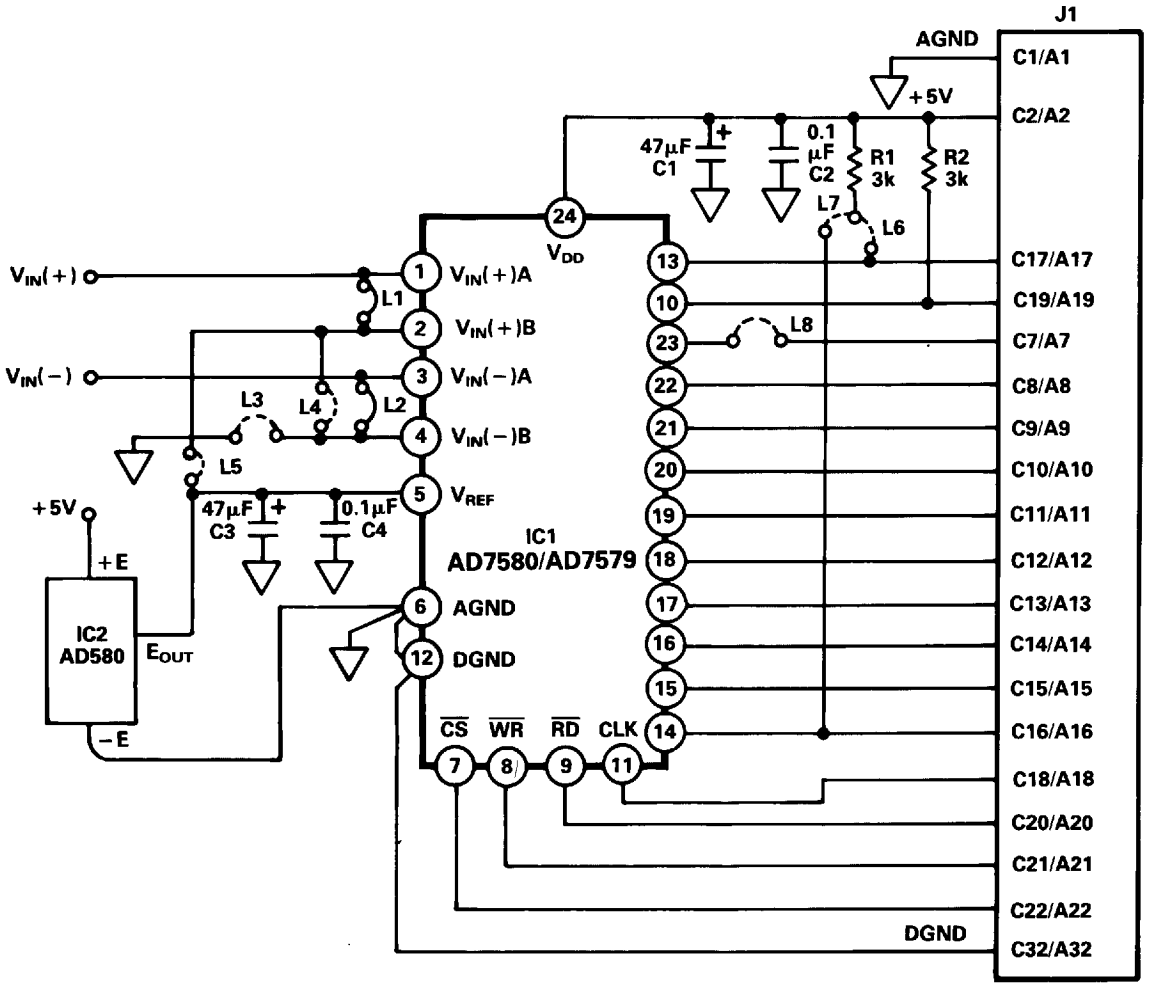


Figure 26. Schematic for AD7579/AD7580 Board

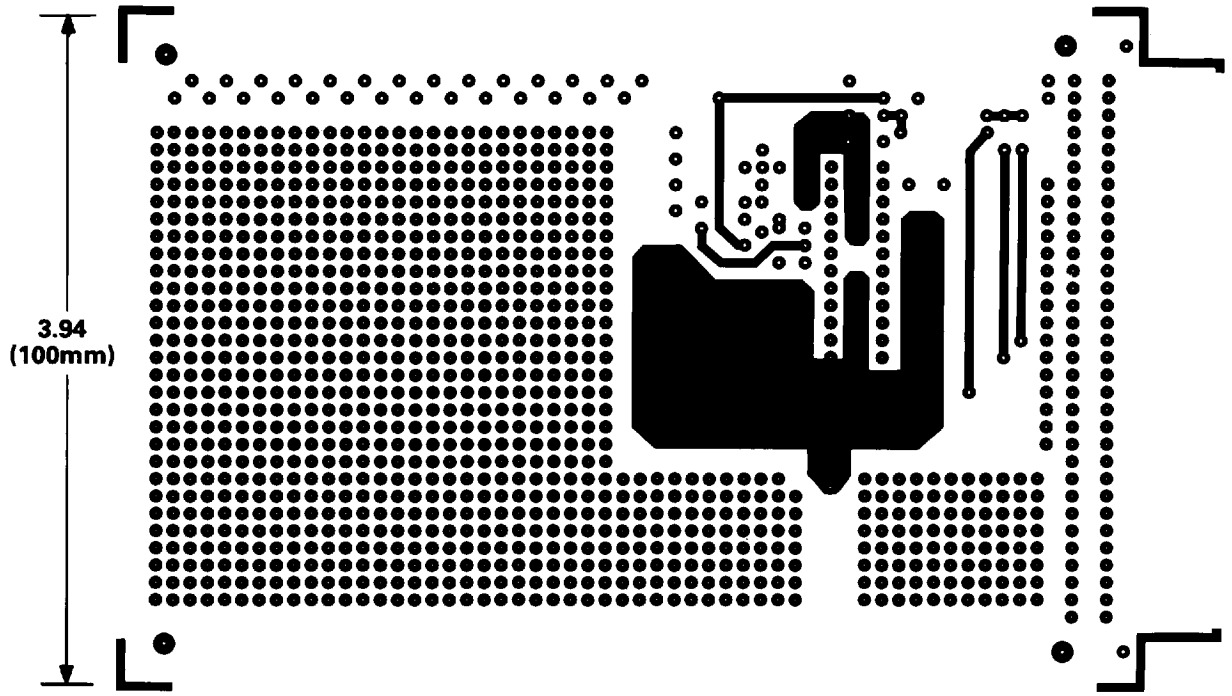


Figure 27. PCB Component Side Layout for Figure 26

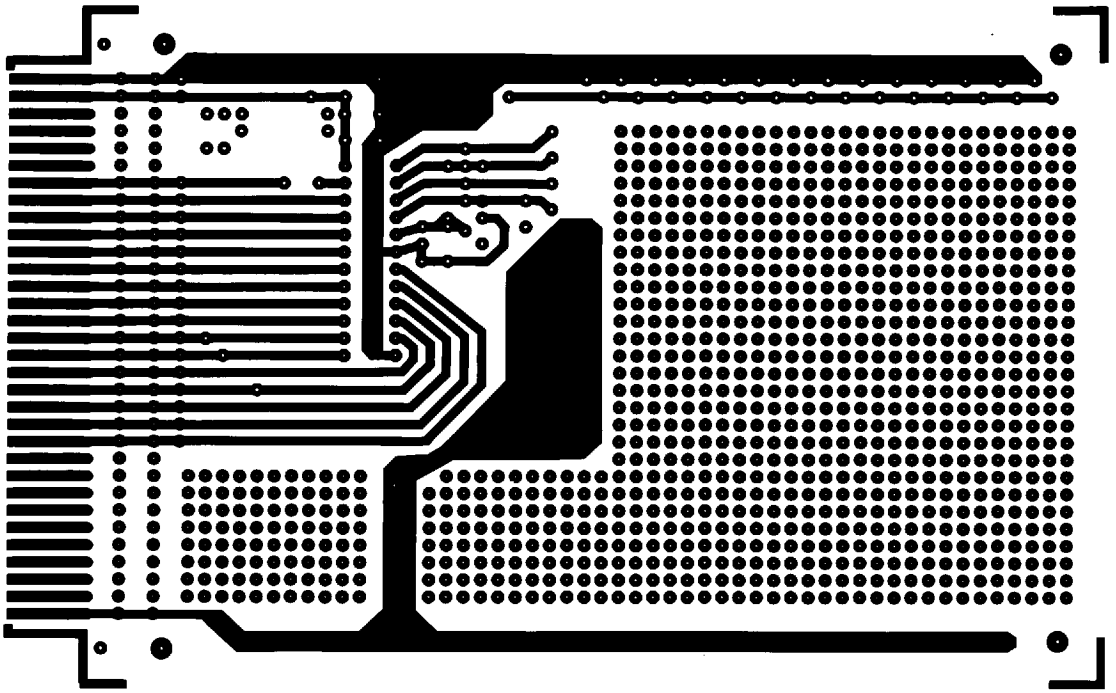


Figure 28. PCB Solder Side Layout for Figure 26

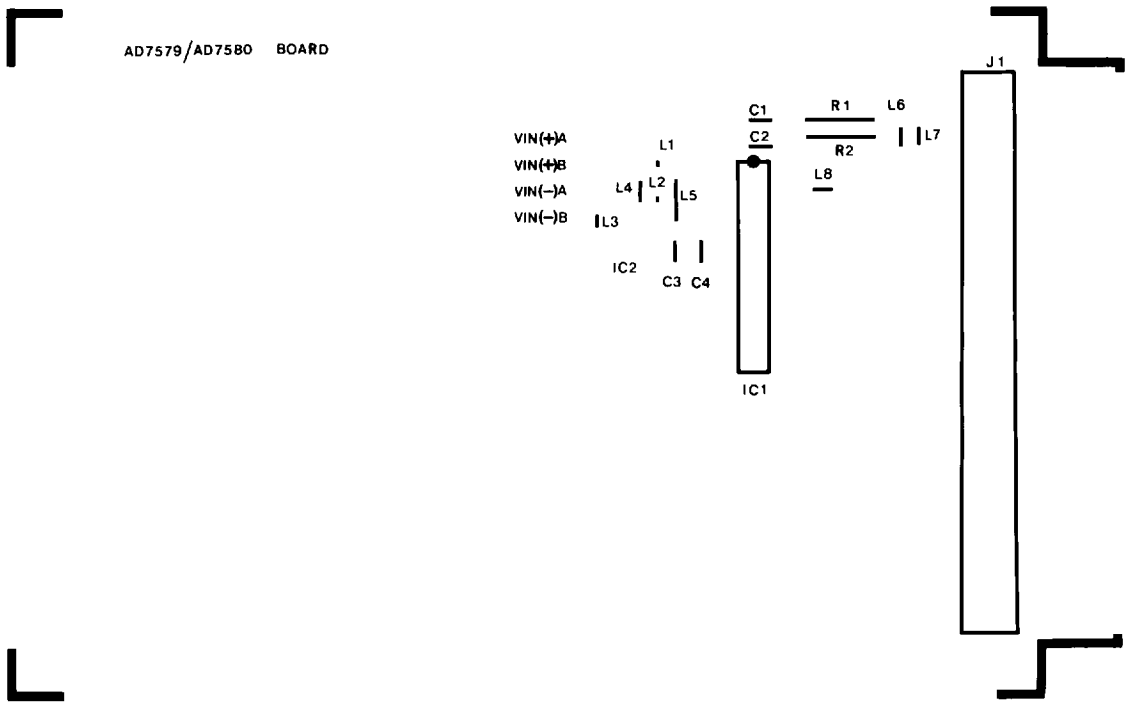


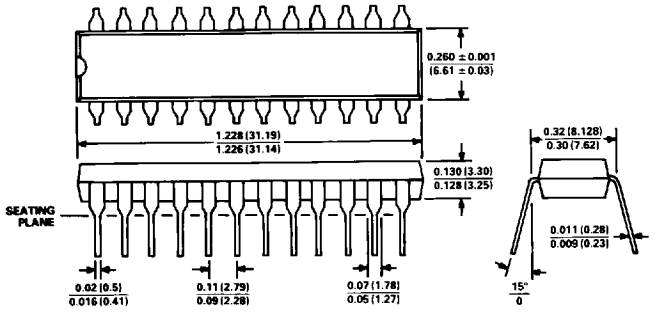
Figure 29. Component Overlay for Circuit of Figure 26

MECHANICAL INFORMATION

OUTLINE DIMENSIONS

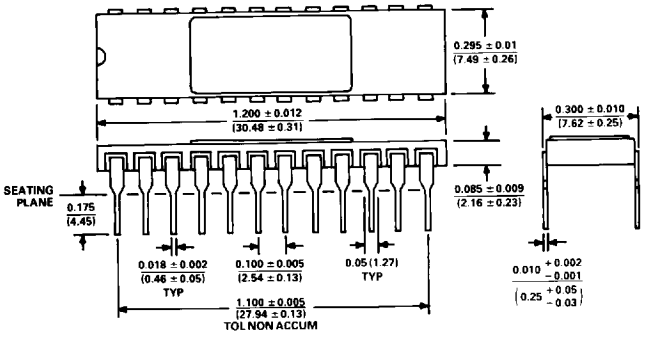
Dimensions shown in inches and (mm).

24-PIN PLASTIC (SUFFIX N)



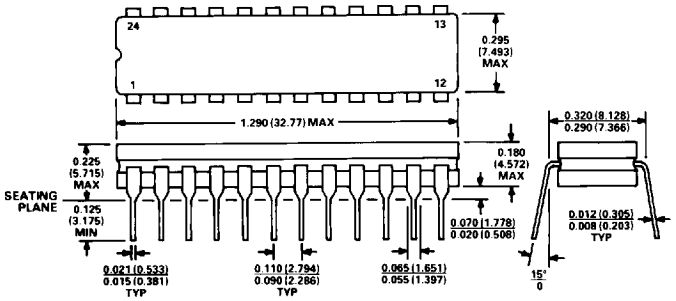
NOTES
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. PLASTIC LEADS WILL BE EITHER SOLDER DIPPED OR TIN LEAD PLATED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

24-PIN CERAMIC (SUFFIX Q)



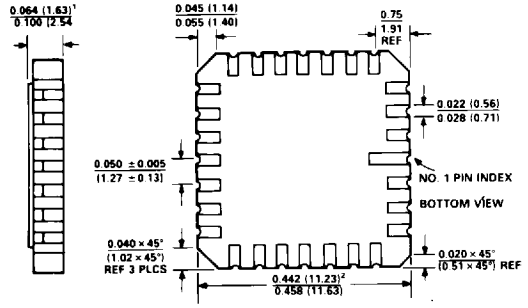
NOTES
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. CERAMIC DIP LEADS WILL BE EITHER GOLD OR TIN PLATED IN ACCORDANCE WITH MIL-M-385 TO REQUIREMENTS.
3. METAL LID IS CONNECTED TO DGND.

24-PIN CERDIP (SUFFIX Q)



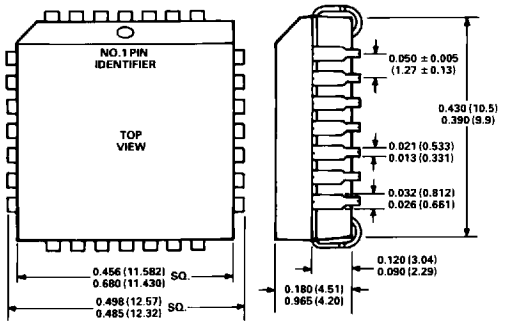
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. CERDIP LEADS WILL BE EITHER TIN PLATED OR SOLDER DIPPED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

28-TERMINAL LEADLESS CERAMIC CHIP CARRIER (SUFFIX E)



NOTES
1. THIS DIMENSION CONTROLS THE OVERALL PACKAGE THICKNESS.
2. APPLIES TO ALL FOUR SIDES.
3. ALL TERMINALS ARE GOLD PLATED.

28-TERMINAL PLASTIC LEADED CHIP CARRIER (SUFFIX P)



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