GTL2009

3-bit GTL Front-Side Bus frequency comparator

Rev. 01 — 22 September 2005 Product data sheet

1. General description

The GTL2009 is designed for the Nocona and Dempsey/Blackford dual Intel Xeon processor platforms to compare the Front-Side Bus (FSB) frequency settings and set the common FSB frequency at the lowest setting if both processor slots are occupied or the FSB setting of the occupied processor slot if only one processor is being used. A default FSB frequency of 100 MHz is initially set upon power-up when V_{DD} is greater than 1.5 V.

Magnitude comparisons and frequency multiplexing to compute the common FSB frequency occurs when the two 3-bit FSB GTL inputs from the chip sets are valid. The common FSB frequency GTL outputs switch from the default frequency to the computed frequency when the GTL reference voltage input (VREF) crosses a static 0.6 V internally generated input comparator reference voltage. The GTL2009 then continually monitors the FSB frequency and slot occupied inputs for any further changes.

The Nocona and Dempsey/Blackford Xeon processors specify a V_{TT} of 1.2 V and 1.1 V, as well as a nominal V_{ref} of 0.76 V and 0.73 V respectively. To allow for future voltage level changes that may extend V_{ref} to 0.63 of V_{TT} (minimum of 0.693 V with V_{TT} of 1.1 V) the GTL2009 allows a minimum V_{ref} of 0.66 V. Characterization results show that there is little DC or AC performance variation between these levels.

The GTL2009 is a companion chip to the GTL2006 platform health management GTL-to-LVTTL translator and the newer GTL2007 that adds an enable function that disables the error output to the monitoring agent for platforms that monitor the individual error conditions from each processor.

2. Features

- Compares FSB frequency inputs to set the lowest frequency as the common bus frequency.
- Operates at a range of GTL signal levels
- 3.0 V to 3.6 V operation
- LVTTL I/O are not 5 V tolerant
- Companion chip to GTL2006 and GTL2007
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78, which exceeds 500 mA
- Available in TSSOP16 package

PHILIPS

3. Quick reference data

Table 1: Quick reference data

T_{amb} = 25 °C

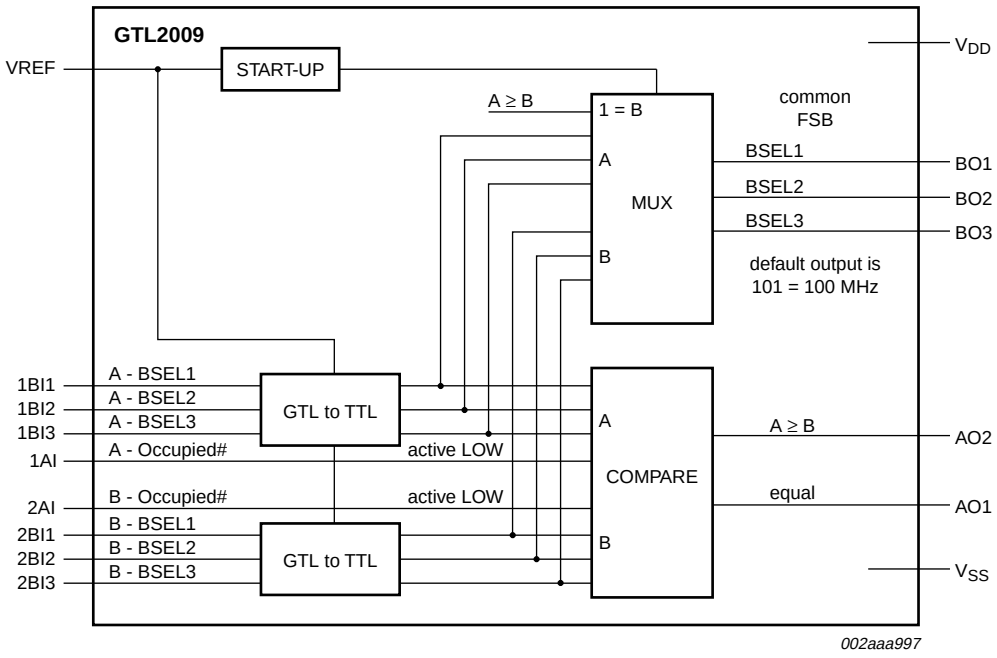
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PLH}	LOW-to-HIGH propagation delay; BI to BO	C_L = 30 pF; V_{DD} = 3.3 V	3.0	16.5	30	ns
t_{PHL}	HIGH-to-LOW propagation delay; BI to BO		2.3	16.2	30	ns

4. Ordering information

Table 2: Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
GTL2009PW	GTL2009	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

5. Functional diagram



If B - Occupied only, then A ≥ B = 1.

If A - Occupied only, then A ≥ B = 0.

If A and B - Occupied, then A ≥ B = 1 if A frequency higher than B frequency.

Pin assignment: A = LVTTL, B = GTL, I = Input, O = Output.

Refer to Section 7.2 “Default conditions input”.

Fig 1. Functional diagram of GTL2009

6. Pinning information

6.1 Pinning

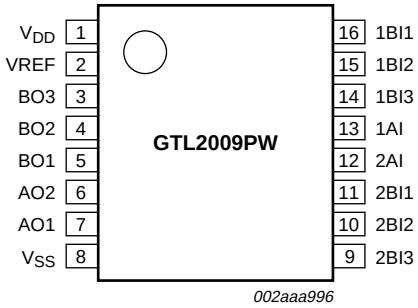


Fig 2. Pin configuration for TSSOP16

6.2 Pin description

Table 3: Pin description

Symbol	Pin	Type	Description
V_{DD}	1	supply	supply voltage
VREF	2	V_{ref}	V_{ref} input voltage
BO3	3	GTL output	BSEL3
BO2	4	GTL output	BSEL2
BO1	5	GTL output	BSEL1
AO2	6	LVTTL output	A ≥ B
AO1	7	LVTTL output	equal
V_{SS}	8	ground	ground supply
2BI3	9	GTL input	B-BSEL3
2BI2	10	GTL input	B-BSEL2
2BI1	11	GTL input	B-BSEL1
2AI	12	LVTTL input	B-occupied
1AI	13	LVTTL input	A-occupied
1BI3	14	GTL input	A-BSEL3
1BI2	15	GTL input	A-BSEL2
1BI1	16	GTL input	A-BSEL1

7. Functional description

Refer to Figure 1 “Functional diagram of GTL2009”.

7.1 Function tables

Table 4: FSB frequency selection

BSEL3	BSEL2	BSEL1	FSB
H	L	H	100 MHz
L	L	H	133 MHz
L	H	H	166 MHz
L	H	L	200 MHz
L	L	L	266 MHz
H	L	L	333 MHz
H	H	L	400 MHz
H	H	H	reserved

Table 5: FSB frequency comparison

Default on start-up is 101

Processor A FSB	Processor B FSB	Pins BO1/BO2/BO3
		Common FSB frequency
A ≥ B	A ≥ B	B
A < B	A < B	A
not occupied	B	B
A	not occupied	A
A = B	A = B	A or B

Table 6: FSB the same output

Processor A FSB	Processor B FSB	Compare	Pin AO1
		A frequency = B frequency	
A > B	A > B	no	L
A < B	A < B	no	L
A = B	A = B	yes	H

Table 7: FSB processor A greater than or equal to processor B output

Pin 1AI		Pin 2AI		Compare	Pin AO2
A-occupied		B-occupied		A frequency > B frequency	
L	yes	L	yes	no	L
				yes	H
H	no	L	yes	X	H
L	yes	H	no	X	L
H	no	H	no	X	H

7.2 Default conditions input

The FSB GTL output data is masked and a specific default value (100 MHz) is inserted upon power-up when V_{DD} is greater than 1.5 V. The FSB GTL output data is unmasked and valid data is supplied when the VREF input crosses a static 0.6 V internally generated input comparator reference voltage. For slowly rising GTL V_{TT} supply (0.7 V/500 µs), the switch-over happens at the 0.6 V threshold. For fast rising GTL V_{TT} supply (0.7 V/100 ns), the switch-over typically occurs between 350 ns to 1.5 µs after the 0.6 V threshold is exceeded.

The AO1 and AO2 outputs do not have ‘default conditions’ like those assigned to the GTL outputs. Instead, these two pins will power-up according to the conditions applied to the 1A1 and 2A1 input pins as shown in Table 8. If the slot is occupied, the input is LOW.

Table 8: AO1 and AO2 power-up conditions

H = HIGH; L = LOW.

1AI	2AI	V_{DD}	AO1	AO2
L	L	<1.5 V	L	L
L	L	>1.5 V	H	H
L	H	<1.5 V	L	L
L	H	>1.5 V	L	L
H	L	<1.5 V	L	L
H	L	>1.5 V	L	H
H	H	<1.5 V	L	L
H	H	>1.5 V	H	H

It is important to note that the AO1 and AO2 outputs may be valid a little before 1.5 V and will rise with V_{DD}. Valid outputs from the system level perspective will be achieved after V_{DD} is in regulation, V_{TT} ramps up, and after the internal propagation delay of the GTL2009. No firm answer for this can be given since the time it takes for V_{DD} to be in regulation varies from 100 ms to 1000 ms, and the rise time of V_{TT} is unknown. The GTL2009 outputs are valid after the GTL inputs are valid plus 19.6 ns (worst-case propagation delay of the GTL-to-LVTTL path).

8. Application design-in information

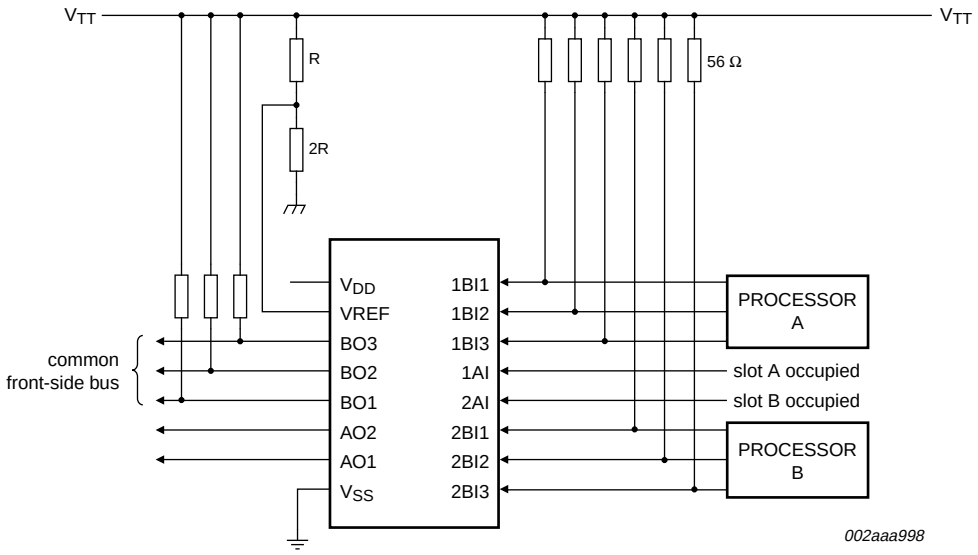


Fig 3. Application diagram

8.1 Frequently asked questions

Question 1: When the GTL2009 is unpowered, the LVTTL inputs may be pulled up to 3.3 V and we want to make sure that there is no leakage path to the power rail under this condition. Are the LVTTL inputs high-impedance when the device is unpowered and will there be any leakage?

Answer 1: When the device is unpowered, the LVTTL inputs will be in a high-impedance state and will not leak to V_{DD} if they are pulled HIGH or LOW while the device is unpowered.

Question 2: What is the condition of the GTL and LVTTL output pins when the device is unpowered?

Answer 2: The open-drain GTL outputs will not leak to the power supply if they are pulled HIGH or allowed to float while the device is unpowered. The GTL inputs will also not leak to the power supply under the same conditions. The LVTTL totem pole outputs, however, are not open-drain type outputs and there will be current flow on these pins if they are pulled HIGH when V_{DD} is at ground.

9. Limiting values

Table 9: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). [1]
Voltages are referenced to V_{SS} (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			–0.5	+4.6	V
I_{IK}	input clamping current	$V_I < 0$ V		-	–50	mA
V_I	input voltage	A port (LVTTL)	[3]	–0.5	+4.6	V
		B port (GTL)	[3]	-	–50	mA
I_{OK}	output clamping current	$V_O < 0$ V		-	–50	mA
V_O	output voltage	output in Off or HIGH state; A port	[3]	–0.5	+4.6	V
		output in Off or HIGH state; B port	[3]	–0.5	+4.6	V
I_{OL}	LOW-state output current [4]	A port		-	24	mA
		B port		-	30	mA
I_{OH}	HIGH-state output current [5]	A port		-	–24	mA
T_{stg}	storage temperature			–60	+150	°C
T_j	junction temperature		[2]	-	+125	°C

[1] Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Section 10 “Recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

[3] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[4] Current into any output in the LOW state.

[5] Current into any output in the HIGH state.

10. Recommended operating conditions

Table 10: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		3.0	3.3	3.6	V
V_{TT}	termination voltage	GTL	-	1.2	-	V
V_{ref}	reference voltage	GTL	0.66	0.8	1.1	V
V_I	input voltage	A port	0	3.3	3.6	V
		B port	0	V_{TT}	3.6	V
V_{IH}	HIGH-state input voltage	A port	2	-	-	V
		B port	V_{ref} + 0.050	-	-	V
V_{IL}	LOW-state input voltage	A port	-	-	0.8	V
		B port	-	-	V_{ref} – 0.050	V
I_{OH}	HIGH-state output current	A port	-	-	–12	mA
I_{OL}	LOW-state output current	A port	-	-	12	mA
		B port	-	-	15	mA
T_{amb}	ambient temperature	operating in free air	–40	-	+85	°C

11. Static characteristics

Table 11: Static characteristics

Over recommended operating conditions. Voltages are referenced to V_{SS} (ground = 0 V). T_{amb} = −40 °C to +85 °C.

Symbol	Parameter	Conditions		Min	Typ [1]	Max	Unit
V_{OH}	HIGH-level output voltage; A port	V_{DD} = 3.0 V to 3.6 V; I_{OH} = −100 µA	[2]	V_{DD} − 0.2	2.99	-	V
		V_{DD} = 3.0 V; I_{OH} = −16 mA	[2]	2.1	2.37	-	V
V_{OL}	LOW-level output voltage; A port	V_{DD} = 3.0 V; I_{OL} = 8 mA	[2]	-	0.27	0.4	V
		V_{DD} = 3.0 V; I_{OL} = 12 mA	[2]	-	0.4	0.55	V
	LOW-level output voltage; B port	V_{DD} = 3.0 V; I_{OL} = 15 mA	[2]	-	0.11	0.4	V
I_I	input current; A port	V_{DD} = 3.6 V; V_I = V_{DD}		-	-	± 1	µA
		V_{DD} = 3.6 V; V_I = 0 V		-	-	± 1	µA
	input current; B port	V_{DD} = 3.6 V; V_I = V_{TT} or V_{SS}		-	-	± 1	µA
I_{LO}	output leakage current; B port	V_{DD} = 3.6 V; V_O = V_{TT}		-	-	± 1	µA
I_{DD}	supply current; A or B port	V_{DD} = 3.6 V; V_I = V_{DD} or V_{SS}; I_O = 0 mA		-	5.5	10	mA
ΔI_{DD}	additional quiescent supply current; A port or control inputs	V_{DD} = 3.6 V; V_I = V_{DD} − 0.6 V	[3]	-	32	500	µA
C_{io}	input/output capacitance; A port	V_O = 3.0 V or 0 V		-	7.8	-	pF
	input/output capacitance; B port	V_O = V_{TT} or 0 V		-	4.5	-	pF

[1] All typical values are measured at V_{DD} = 3.3 V and T_{amb} = 25 °C.

[2] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[3] This is the increase in supply current for each input that is at the specified LVTTL voltage level, rather than V_{DD} or V_{SS}.

12. Dynamic characteristics

Table 12: Dynamic characteristics

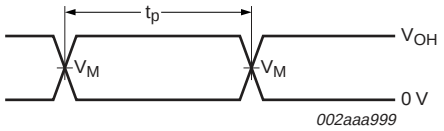
V_{DD} = 3.3 V ± 0.3 V

Symbol	Parameter	Conditions	Limits						Unit
			V_{ref} = 0.73 V; V_{TT} = 1.1 V			V_{ref} = 0.76 V; V_{TT} = 1.2 V			
			Min	Typ [1]	Max	Min	Typ [1]	Max	
t_{PLH}	LOW-to-HIGH propagation delay; AI to AO	Figure 4 and Figure 8	1.4	7.9	14.5	1.4	7.8	14.5	ns
t_{PHL}	HIGH-to-LOW propagation delay; AI to AO		2.0	9.0	16.0	2.0	8.8	16.0	ns
t_{PLH}	LOW-to-HIGH propagation delay; BI to AO	Figure 6	2.6	16.3	30.0	2.5	16.5	30.5	ns
t_{PHL}	HIGH-to-LOW propagation delay; BI to AO		2.8	13.9	25.0	2.9	14.0	25.0	ns
t_{PLH}	LOW-to-HIGH propagation delay; BI to BO	Figure 7	3.0	16.5	30.0	3.0	16.5	30.0	ns
t_{PHL}	HIGH-to-LOW propagation delay; BI to BO		2.3	16.2	30.0	2.3	16.2	30.0	ns
t_{PLH}	LOW-to-HIGH propagation delay; AI to BO	Figure 5	2.1	7.9	14.0	2.0	8.3	14.5	ns
t_{PHL}	HIGH-to-LOW propagation delay; AI to BO		1.4	7.3	13.5	1.5	7.7	14.0	ns

[1] All typical values are at V_{DD} = 3.3 V and T_{amb} = 25 °C.

12.1 AC waveforms

V_M = 1.5 V at $V_{DD} \geq 3.0$ V for A ports; $V_M = V_{ref}$ for B ports.



V_M = 1.5 V for A port and V_{ref} for B port.
V_{OH} = 3 V for A port and V_{TT} for B port
t_p = pulse duration

Fig 4. Pulse duration

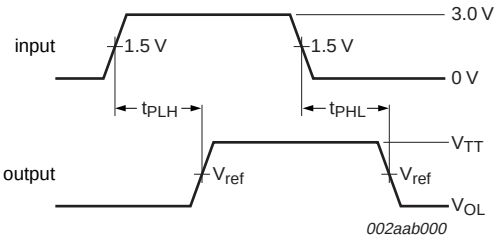
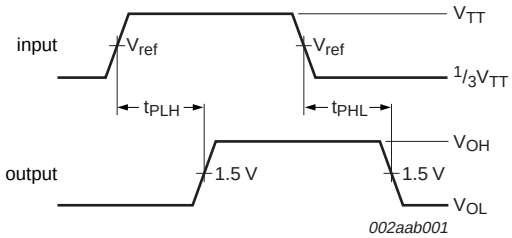


Fig 5. Propagation delay, A port to B port



PRR ≤ 10 MHz; Z_o = 50 Ω; $t_r \leq 2.5$ ns; $t_f \leq 2.5$ ns

Fig 6. Propagation delay, BI to AO

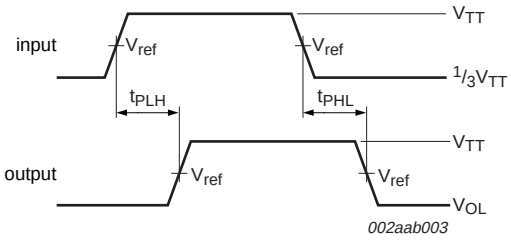


Fig 7. Propagation delay, BI to BO

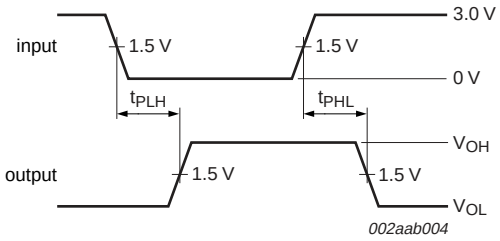


Fig 8. Propagation delay, AI to AO

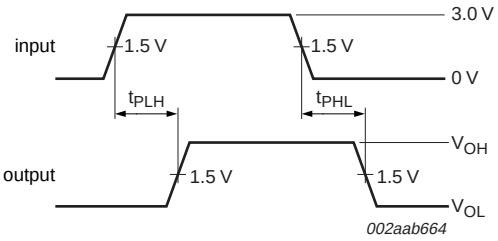


Fig 9. Propagation delay, 1AI to AO2

13. Test information

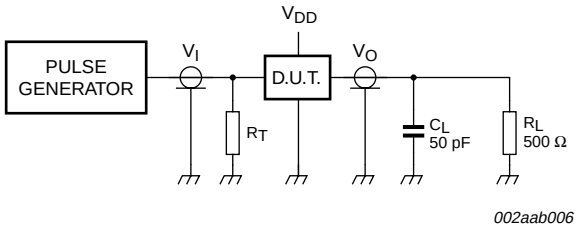


Fig 10. Load circuitry for A outputs

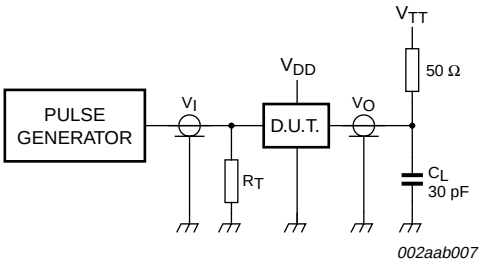


Fig 11. Load circuit for B outputs

Definitions:

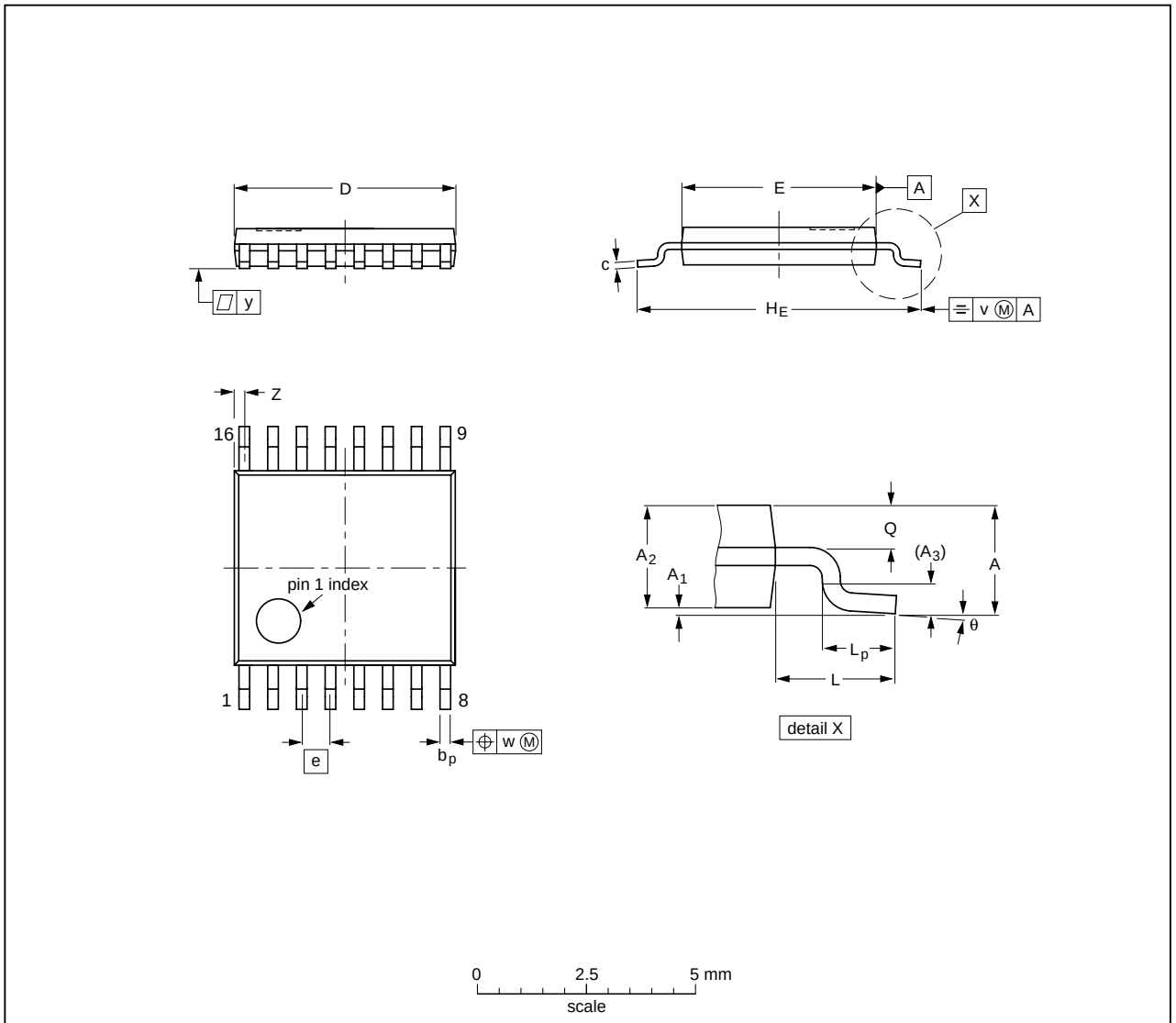
R_L — load resistor

C_L — load capacitance includes jig and probe capacitance.

R_T — termination resistance should be equal to Z_o of pulse generators.

14. Package outline

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 12. Package outline SOT403-1 (TSSOP16)

15. Soldering

15.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

15.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

15.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;

– smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

15.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

15.5 Package related soldering information

Table 13: Suitability of surface mount IC packages for wave and reflow soldering methods

Package [1]	Soldering method	
	Wave	Reflow [2]
BGA, HTSSON..T [3], LBGA, LFBGA, SQFP, SSOP..T [3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable [4]	suitable
PLCC [5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended [5] [6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended [7]	suitable
CWQCCN..L [8], PMFP [9], WQCCN..L [8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

16. Abbreviations

Table 14: Abbreviations

Acronym	Definition
CDM	Charged Device Model
ESD	Electrostatic Discharge
FSB	Front-Side Bus
GTL	Gunning Transceiver Logic
HBM	Human Body Model
LVTTL	Low Voltage Transistor-Transistor Logic
MM	Machine Model
PRR	Pulse Rate Repetition

17. Revision history

Table 15: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
GTL2009_1	20050922	Product data sheet	-	9397 750 13556	-

18. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

19. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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23. Contents

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