# UM11595

## PTN38007-EVM/PTN38003A-EVM evaluation board

Rev. 1.0 — 28 June 2021 User manual

**Document information**

| Information | Content |
|---|---|
| Keywords | PTN38007, PTN38003A, PTN5110, USB Type-C, CC Logic, Orientation Detection, USB3.1 Gen2, USB3.2, USB4.0, SuperSpeed, DisplayPort, Linear Redriver |
| Abstract | The PTN38007-EVM/PTN38003A-EVM is capable of interfacing a USB Type-C port with various alternate mode devices. The evaluation board is intended for use as an evaluation and customer demonstration tool, as well as a reference design. |

**Revision history**

| Rev | Date | Description |
|---|---|---|
| v.1.0 | 20210628 | Initial version |

## Important notice

NXP provides the enclosed product(s) under the following conditions:

This evaluation kit is intended for use of ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY. It is provided as a sample IC pre-soldered to a printed circuit board to make it easier to access inputs, outputs, and supply terminals. This evaluation board may be used with any development system or other source of I/O signals by simply connecting it to the host MCU or computer board via off-the-shelf cables. This evaluation board is not a Reference Design and is not intended to represent a final design recommendation for any particular application. Final device in an application will be heavily dependent on proper printed circuit board layout and heat sinking design as well as attention to supply filtering, transient suppression, and I/O signal quality.

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# 1 Introduction

PTN38007 and PTN38003A (PTN38007/3A) are a Type-C USB3.2/ DP1.4 combo redriver optimized for USB3 and DisplayPort applications on either the Downstream Facing Port (DFP) or Upstream Facing Port (UFP) by following the four high-speed differential data flow to extend the signal reach.

This document explains in detail how to connect the PTN38007/3A-EVM evaluation board in a system using external PD controller in a stand-alone mode, and how to configure the on-board multiplexers for each operation mode. The document also illustrates the LPCUSBSIO module operation and configuration with the PTN38007/3A-EVM evaluation board.

# 2 Finding kit resources and information on the NXP web site

NXP Semiconductors provides online resources for this evaluation board and its supported device(s) on http://www.nxp.com.

The information page for PTN38007-EVM evaluation board is at http://www.nxp.com/PTN38007-EVM, and the information page for PTN38003A-EVM evaluation board is at http://www.nxp.com/PTN38003A-EVM. The information page provides overview information, documentation, software and tools, parametrics, ordering information and a **Getting Started** tab. The **Getting Started** tab provides quick-reference information applicable to using the PTN38007/3A-EVM evaluation board, including the downloadable assets referenced in this document.

## 2.1 Collaborate in the NXP community

The NXP community is for sharing ideas and tips, ask and answer technical questions, and receive input on just about any embedded design topic.

The NXP community is at http://community.nxp.com.

# 3 Getting ready

Working with the PTN38007/3A-EVM evaluation board requires the kit contents, additional hardware and a Windows PC workstation with installed software.

## 3.1 Kit contents

- Assembled and tested evaluation board in an anti-static bag
- Quick Start Guide

## 3.2 Additional hardware

In addition to the kit contents, the following hardware is necessary or beneficial when working with this kit.

- One PC/Notebook with USB-C supporting USB3.2 Gen1/2, DisplayPort, Thunderbolt 3 (PTN38007 only), or USB4 (PTN38007 only). A USB-A connector is also needed to configure EVM via micro-USB cable
- Corresponding device for evaluation: USB3.2 Gen1/2, DisplayPort monitor, Thunderbolt 3 (PTN38007 only), or USB4 (PTN38007 only)

- One Type-C cable to connect between EVM and device
- One micro-USB cable to connect EVM to a PC

### 3.3 Windows PC workstation

This evaluation board requires a Windows PC workstation. Meeting these minimum specifications should produce great results when working with this evaluation board.

- USB-enabled computer with Windows 7 or Windows 10

### 3.4 Software

Installing software is necessary to work with this evaluation board. All listed software is available on the evaluation board's information page at http://www.nxp.com/PTN38007-EVM or http://www.nxp.com/PTN38003A-EVM.

## 4 Getting to know the hardware

The stand-alone board is intended to evaluate PTN38007/3A on an existing USB Type-C port that supports USB3.1/3.2, DisplayPort, Thunderbolt 3 and USB4. When using the DFP board ("$H_2$" is marked on the top side of the board), the user connects the upstream port (J101) of this evaluation board directly to a Type-C port of a computer or phone without any Type-C cable, and downstream port (J102) is connected to a device or docking station through either a standard Type-C cable, or tethered cable from the device/dock.

When using the UFP board ("$D_2$" is marked on the top side of the board), user connects the downstream port (J201) of this evaluation board directly to a Type-C port of a device or a docking station without any Type-C cable, and upstream port (J202) is connected to a computer or a phone through a standard Type-C cable.

While this board is powered through a USB micro-B cable (5 V input) on J105, PTN38007/3A, on-board AUX/LS multiplexers, and PCA9570 GPIO expanders are powered up, and the user can use an $I^2C$ tool such as LPCUSBSIO (built-in function in LPCUSBSIO module) to configure PTN38007/3A into different operating modes, using the GPIO expander's output to configure plug orientation and multiplexer selection (tri-stated or DisplayPort AUX Enabled). A GUI interface is also available to configure the above configurations.

## 4.1 Block diagram

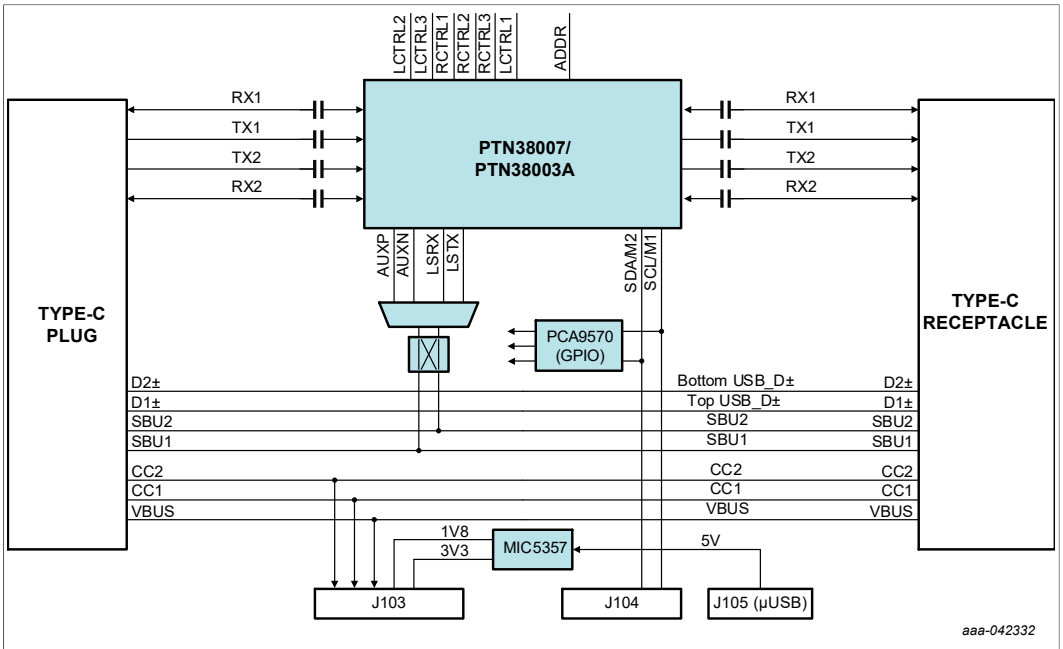



**Figure 1. Block diagram**

## 4.2 PCB photo


**Figure 2. PTN38007/3A-EVM evaluation board front side**

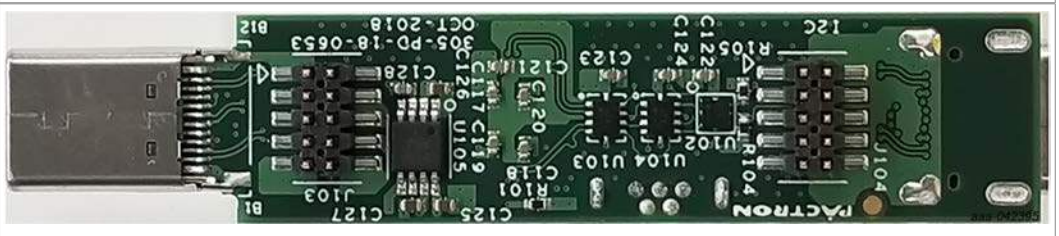


**Figure 3. PTN38007/3A-EVM evaluation board back side**

## 4.3 PTN38007/3A-EVM evaluation board schematics

### 4.3.1 Type-C connector and PTN38007/3A (DFP)

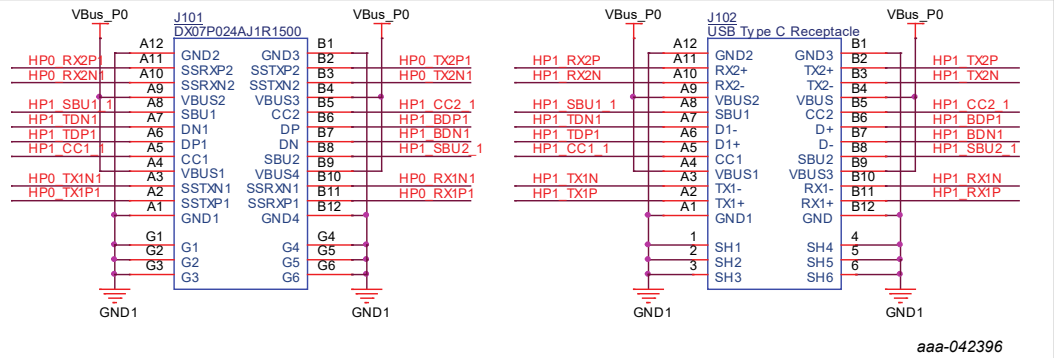



**Figure 4. Schematic of Type-C connector and PTN38007/3A (DFP)**

The connection between PTN38007/3A and upstream/downstream Type-C receptacles are according to the datasheet's pin assignment.

When PTN38007/3A is used in DFP configuration, the board is marked with '$H_2$' as "connecting to Host side". J101 is used as a UFP port that plugs into a computer, and J102 is used as a DFP port that plugs into a device or dock. CC1/CC2/VBUS/SBU1/SUB2/USB2_D± signals pass through from the plug side to receptacle side.

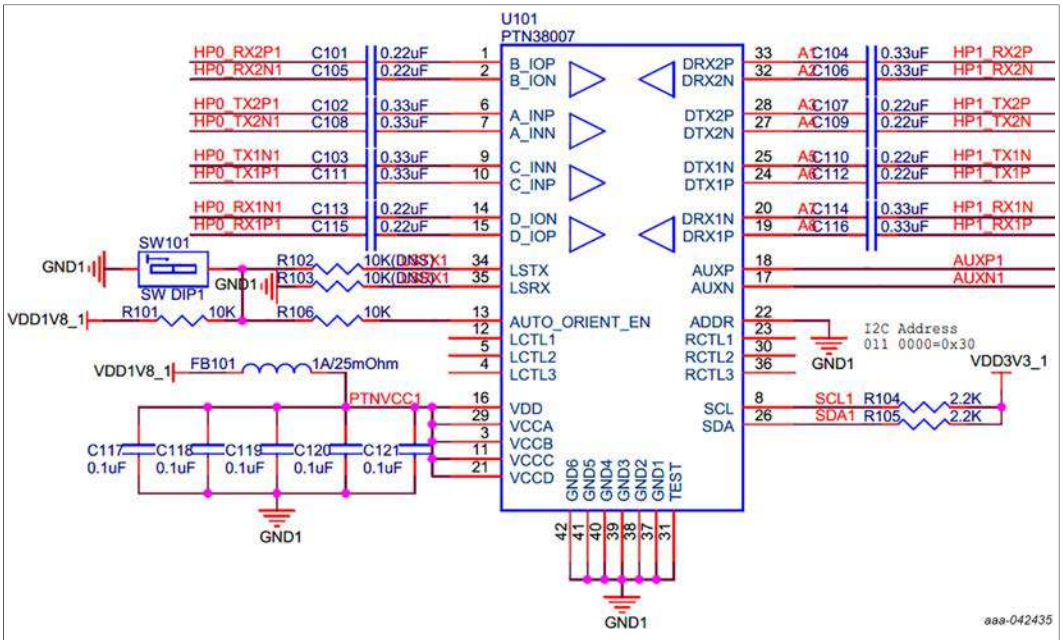



**Figure 5. Schematic of DFP board**

On the DFP board, PTN38007/3's 7-bit $I^2C$ address is set to 0110 000 by connecting ADDR/ORIENT pin to GND directly. This address is being used by GUI to distinguish if a DFP or a UFP board is being used. The AUTO_ORIENTATION_EN pin is pulled up by default, thus the AUTO ORIENTATION DETECTION function is enabled. However, this will not impact the normal operation. GUI scripts will always override this function, and correct orientation is always programmed.

### 4.3.2 Type-C connector and PTN38007/3A (UFP)

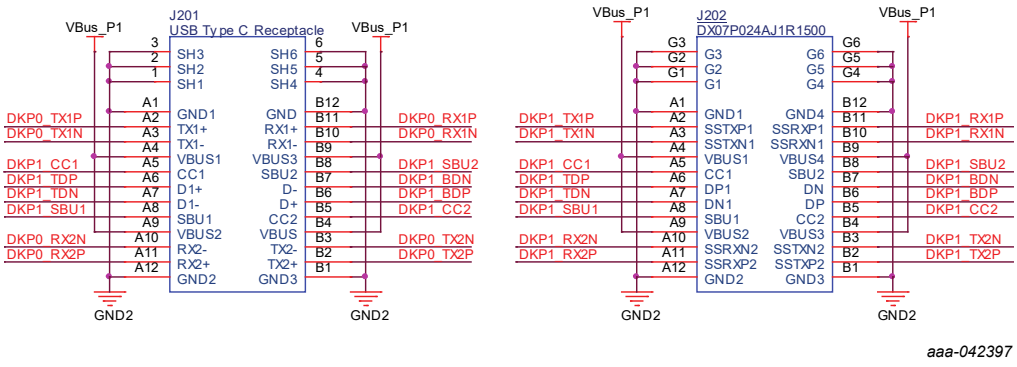



**Figure 6. Schematic of Type-C Connector and PTN38007/3A (UFP)**

The connection between PTN38007/3A and upstream/downstream Type-C receptacles are according to the datasheet's pin assignment.

When PTN38007/3A is used in UFP configuration, the board is marked with '$D_2$' as "connecting to Device side". J201 is used as a UFP port that plugs into a computer, and J202 is used as a DFP port that plugs into a device or dock. CC1/CC2/VBUS/SBU1/ SUB2/USB2_D± signals pass through from the plug side to receptacle side.

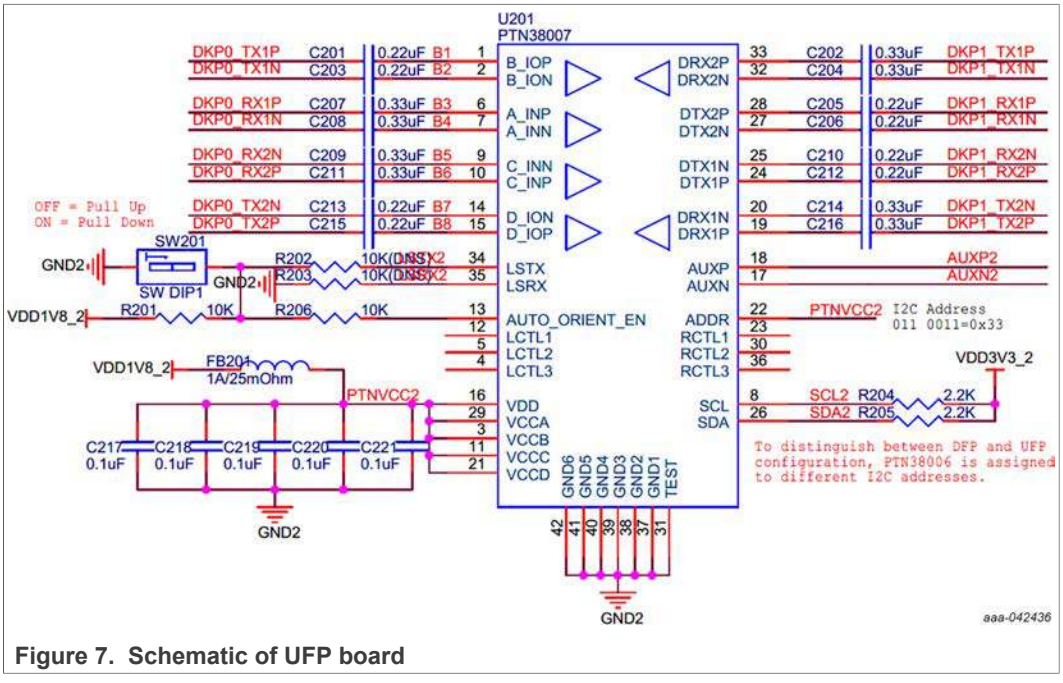



**Figure 7. Schematic of UFP board**

On the UFP board, PTN38007/3A's 7-bit $I^2C$ address is set to 0110 011 by connecting ADDR/ORIENT pin to VDD directly. This address is being used by GUI to distinguish if a DFP or a UFP board is being used. The AUTO_ORIENTATION_EN pin is pulled up by default, thus the AUTO ORIENTATION DETECTION function is enabled. However, this will not impact the normal operation. GUI scripts will always override this function, and correct orientation is always programmed.

### 4.3.3 Low-speed switches

There are two layers of low-speed switches using NX3DV221 multiplexers; they are used to sort out the correct polarity of the SBU signals, and then route to PTN38007/3A for snooping purposes.

U104 is implemented as a crossbar switch to orient SBU1 and SBU2 signals as AUXP/AUXN or AUXN/AUXP according to the MUX_ORIENTATION signal. U103 routes the corresponding SBU1/2 signals to PTN38007/3A's AUX and LS snooping pins, depending on whether the interface is in DP alternate mode or Thunderbolt/USB4 mode.

Thunderbolt/USB4 mode and LS signal snooping is only available in PTN38007/3A, and should be ignored in PTN38003A. In a design, these muxes are not needed since the AUX snooping polarity can be changed through PTN38003A's register 0x04 bit [3].

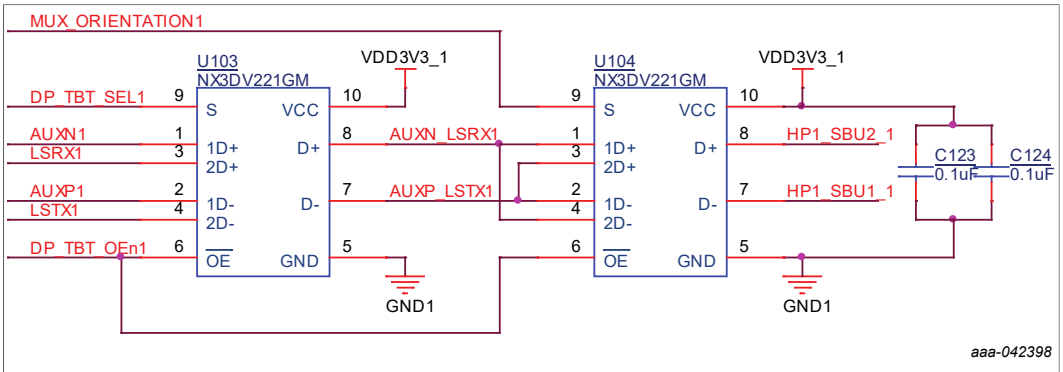



**Figure 8. Schematic of low-speed switches**

### 4.3.4 GPIO expanders

Low-speed switch controls are configured through the GPIO expanders. The GUI user interface also incorporates these controls.

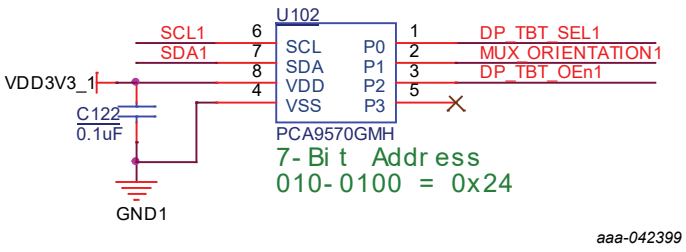



**Figure 9. Schematic of GPIO expanders**

The following table summarizes the GPIO expander's control signal assignment; its 7-bit $I^2C$ slave address is 010 0100.

**Table 1. Control signal assignment for GPIO expander**

| Bit | Signal Name | Comment |
|---|---|---|
| 0 | DP_TBT_SEL | Select DisplayPort or Thunderbolt mode<br>0 = DisplayPort Alternate Mode<br>1 = Thunderbolt Alternate Mode |
| 1 | MUX_ORIENTATION | Select CC line orientation<br>0 = Normal orientation<br>1 = Reversed orientation |

**Table 1. Control signal assignment for GPIO expander...*continued***

| Bit | Signal Name | Comment |
|---|---|---|
| 2 | DP_TBT_OEn | Enable/Disable low-speed switch outputs<br>0 = Enabled<br>1 = Disabled |
| 3 | Output Not Used | Data bit is used to further distinguish different operating modes with the same byte programming. |

In each device operating mode, each bit should be configured as shown in Table 2 and Table 3. Therefore, a predefined byte can be programmed to the GPIO expander's output while transitioning into different modes.

**Table 2. DFP configuration**

| DFP configuration | | Mode 0 Safe State | Mode 1 USB3 Only | Mode 2 USB3+DP2Lane | Mode 3 DP4Lane | Mode 4 Thunderbolt | Mode 5 USB4.0 |
|---|---|---|---|---|---|---|---|
| 0 | DP_TBT_SEL | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | MUX_ORIENTATION | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 |
| 2 | DP_TBT_OEn | 0 | 0 | 0 | 0 | 1 | 1 |
| 3 | Not Used | 0 | 1 | 0 | 1 | 0 | 1 |
| Byte Programming | | 0x04/0x06 | 0x0c/0x0e | 0x00/0x02 | 0x08/0x0a | 0x01/0x03 | 0x09/0x0b |

**Table 3. UFP configuration**

| UFP configuration | | Mode 0 Safe State | Mode 1 USB3 Only | Mode 2 USB3+DP2Lane | Mode 3 DP4Lane | Mode 4 Thunderbolt | Mode 5 USB4.0 |
|---|---|---|---|---|---|---|---|
| 0 | DP_TBT_SEL | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | MUX_ORIENTATION | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 |
| 2 | DP_TBT_OEn | 0 | 0 | 1 | 1 | 0 | 0 |
| 3 | Not Used | 0 | 1 | 0 | 1 | 0 | 1 |
| Byte Programming | | 0x04/0x06 | 0x0c/0x0e | 0x01/0x03 | 0x09/0x0b | 0x00/0x02 | 0x08/0x0a |

### 4.3.5 Board headers

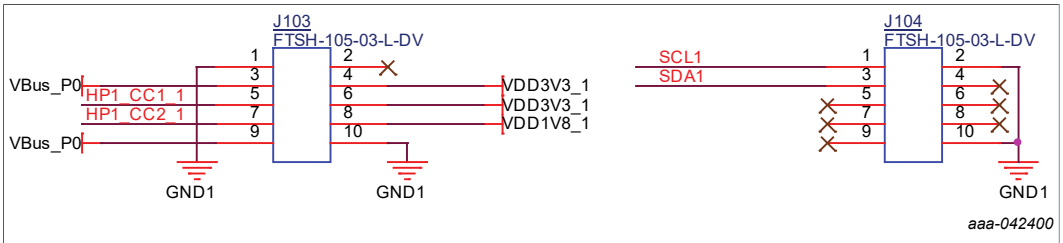



**Figure 10. Schematic of board headers**

There are two 10-pin 50-mil spacing headers (J103 and J104) providing signal connection to the PTN5110 PD baseboard (or LPCUSBSIO module) when the PD baseboard is used. While using PTN38007/3A-EVM evaluation board by itself, J104 can also connect to Aardvark I2C/SPI Host Adapter or Promira Serial Platform with a 100 mil spacing to 50 mil spacing adapter (Digikey Part# 1471-1373-ND).

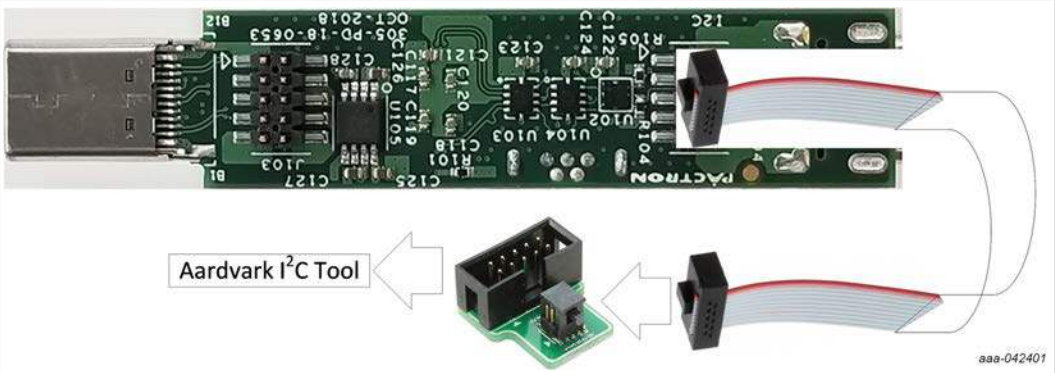



**Figure 11. Connection of board headers**

### 4.3.6 1.8 V and 3.3 V power supplies

The board is supplied with one 5 V power supply source through J105 (micro-USB connector) when in stand-alone mode (without LPCUSBSIO module). There is an LDO power supply that converts 5 V to 3.3 V and 1.8 V. The 1.8 V power supply is used by PTN38007/3A, and the 3.3 V power supply is used by the GPIO expander.

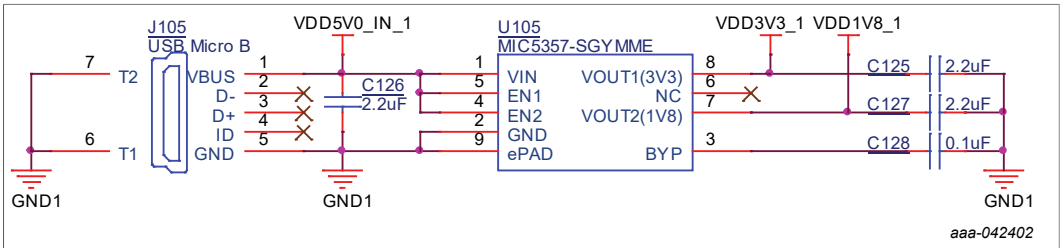



**Figure 12. Schematic of 1.8 V and 3.3 V power supplies**

If the PTN38007/3A-EVM evaluation board is used with an LPCUSBSIO module, USB2 connection to the PTN5110 Sniffer Board (or LPCUSBSIO module) also provides 5 V to the system. There are two switching power supplies on the PTN5110 Sniffer Board (or LPCUSBSIO module) converting 5 V to 1.8 V and 3.3 V; these two power rails are fed into J103 pin 4 (3.3 V), pin 6 (3.3 V), and pin 8 (1.8 V). PTN38007/3A-EVM evaluation board can directly consume power from these pins, and it is not necessary to provide additional power to J105 in this configuration.

Using the LPCUSBSIO module is recommended, and by default, U105 and J105 are not installed.

# 5 I²C programming guide

By default, the following 7-bit I²C addresses are used:

- GPIO Expander: 010 0100
- PTN38007/3: 0110 000 (DFP – $H_2$ board) or 0110 011 (UFP – $D_2$ board)

In this section, the following conventions indicate writing to respective device's internal register addresses:

- GPIO[] = 0xrr: Set GPIO expander's port data to value of 0xrr (there is only one register in this GPIO expander, and there is no need to indicate the address in this context). This is equivalent to GPIO[0xrr] = 0xrr

- Reg[0xnn] = 0xrr: Set PTN38007/3's register @ address 0xnn to value of 0xrr

## 5.1 Power-on initialization

```
// Initialize GPIO Expander

GPIO[] = 0x04 // In Safe State

// PTN38007/3A Initialization for Safe State

// USB3 Initialization

Reg[0x0f] = 0x00 // Enable LOS Detector

Reg[0x10] = 0x0e // Downstream RCTL[2:1] = 10dB, should adapt to
different PCB design if necessary

Reg[0x12] = 0x0e // Upstream LCTL[2:1] = 10dB, should adapt to
different PCB design if necessary

Reg[0x11] = 0x03 // Upstream RCTL[3] = 950mVppd, should adapt to
different PCB design if necessary

Reg[0x13] = 0x03 // Downstream LCTL[3] = 950mVppd, should adapt
to different PCB design if necessary

// DisplayPort Initialization

Reg[0x07] = 0x0e // Lane 0 LCTL[2:1] = 8.3dB, should adapt to
different PCB design if necessary

Reg[0x09] = 0x0e // Lane 1 LCTL[2:1] = 8.3dB, should adapt to
different PCB design if necessary

Reg[0x0b] = 0x0e // Lane 2 LCTL[2:1] = 8.3dB, should adapt to
different PCB design if necessary

Reg[0x0d] = 0x0e // Lane 3 LCTL[2:1] = 8.3dB, should adapt to
different PCB design if necessary

Reg[0x08] = 0x03 // Lane 0 LCTL[3] = 950mVppd, should adapt to
different PCB design if necessary

Reg[0x0a] = 0x03 // Lane 1 LCTL[3] = 950mVppd, should adapt to
different PCB design if necessary

Reg[0x0c] = 0x03 // Lane 2 LCTL[3] = 950mVppd, should adapt to
different PCB design if necessary

Reg[0x0e] = 0x03 // Lane 3 LCTL[3] = 950mVppd, should adapt to
different PCB design if necessary

// Thunderbolt Initialization

Reg[0x15] = 0x09 // Downstream RCTL[2:1] = 12.7dB, should adapt
to different PCB design if necessary

Reg[0x17] = 0x09 // Upstream LCTL[2:1] = 12.7dB, should adapt to
different PCB design if necessary

Reg[0x16] = 0x03 // Upstream RCTL[3] = 950mVppd, should adapt to
different PCB design if necessary
```

```
Reg[0x18] = 0x03 // Downstream LCTL[3] = 950mVppd, should adapt
to different PCB design if necessary

// DFP SafeState Initialization

Reg[0x04] = 0x00 // Default Safe State, With Normal Orientation
```

## 5.2 Operating mode programming

Depending on the operating mode negotiated between the DFP and UFP sides, the following registers should be programmed accordingly.

### 5.2.1 DFP board programming

If the evaluation board is not used, GPIO programming steps are not necessary, and only PTN38007/3A programming steps are required.

**Table 4. DFP modes orientation**

| Orientation<br>DFP Modes | Normal Orientation | Reversed Orientation |
|---|---|---|
| Safe State (Mode = 0) | GPIO[] = 0x04<br>Reg[0x04] = 0x00 | GPIO[] = 0x06<br>Reg[0x04] = 0x10 |
| USB3 Only (Mode = 1) | GPIO[] = 0x0c<br>Reg[0x04] = 0x01 | GPIO[] = 0x0e<br>Reg[0x04] = 0x11 |
| USB3+DP2Lane (Mode = 2) | GPIO[] = 0x00<br>Reg[0x04] = 0x02 | GPIO[] = 0x02<br>Reg[0x04] = 0x12 |
| DP4Lane (Mode = 3) | GPIO[] = 0x08<br>Reg[0x04] = 0x03 | GPIO[] = 0x0a<br>Reg[0x04] = 0x13 |
| Thunderbolt (Mode = 4) | GPIO[] = 0x01<br>Reg[0x04] = 0x04 | GPIO[] = 0x03<br>Reg[0x04] = 0x14 |
| USB4 (Mode = 5) | GPIO[] = 0x09<br>Reg[0x04] = 0x05 | GPIO[] = 0x0b<br>Reg[0x04] = 0x15 |

### 5.2.2 UFP board programming

If the evaluation board is not used, GPIO programming steps are not necessary, and only PTN38007/3A programming steps are required.

**Table 5. UFP modes orientation**

| Orientation<br>UFP Modes | Normal Orientation | Reversed Orientation |
|---|---|---|
| Safe State (Mode = 0) | GPIO[] = 0x04<br>Reg[0x04] = 0x20 | GPIO[] = 0x06<br>Reg[0x04] = 0x30 |
| USB3 Only (Mode = 1) | GPIO[] = 0x0c<br>Reg[0x04] = 0x21 | GPIO[] = 0x0e<br>Reg[0x04] = 0x31 |
| USB3+DP2Lane (Mode = 2) | GPIO[] = 0x01<br>Reg[0x04] = 0x22 | GPIO[] = 0x03<br>Reg[0x04] = 0x32 |
| DP4Lane (Mode = 3) | GPIO[] = 0x09<br>Reg[0x04] = 0x23 | GPIO[] = 0x0b<br>Reg[0x04] = 0x33 |

**Table 5. UFP modes orientation***...continued*

| Orientation<br>UFP Modes | Normal Orientation | Reversed Orientation |
|---|---|---|
| Thunderbolt (Mode = 4) | GPIO[] = 0x00<br>Reg[0x04] = 0x24 | GPIO[] = 0x02<br>Reg[0x04] = 0x34 |
| USB4 (Mode = 5) | GPIO[] = 0x08<br>Reg[0x04] = 0x25 | GPIO[] = 0x0a<br>Reg[0x04] = 0x35 |

# 6 LPCUSBSIO module

The LPCUSBSIO module can be used with PTN38007/3A-EVM evaluation board together to demonstrate programmability of PTN38007/3A through only $I^2C$-bus interface. This module includes a PTN5110 PD PHY and a LPC11U35 microcontroller, and can sniff or monitor CC line traffic to detect if a different alternate mode is negotiated between host and device, and program PTN38007/3A to enter the respective alternate mode accordingly.

If PTN38007/3A-EVM evaluation board is plugged onto a PTN5110 PD baseboard, a PD CC line sniffer and a microcontroller on the baseboard monitors the plug-in orientation, the CC line communications between the upstream port and downstream port are decoded, and the on-board microcontroller configures PTN38007/3A and multiplexers according to the CC communication.

A user can still use the GUI interface and LPCUSBSIO (built-in function in LPCUSBSIO module) to monitor and/or further configure the board if necessary. A separate GUI is also available to communicate between the on-board LPC microcontroller and host PC using USB2.0 interface. By default, the PD sniffer function is not used, and only the USB-2-$I^2C$ bridge (LPCUSBSIO) is implemented in the firmware flashed to the module.

## 6.1 Block diagram

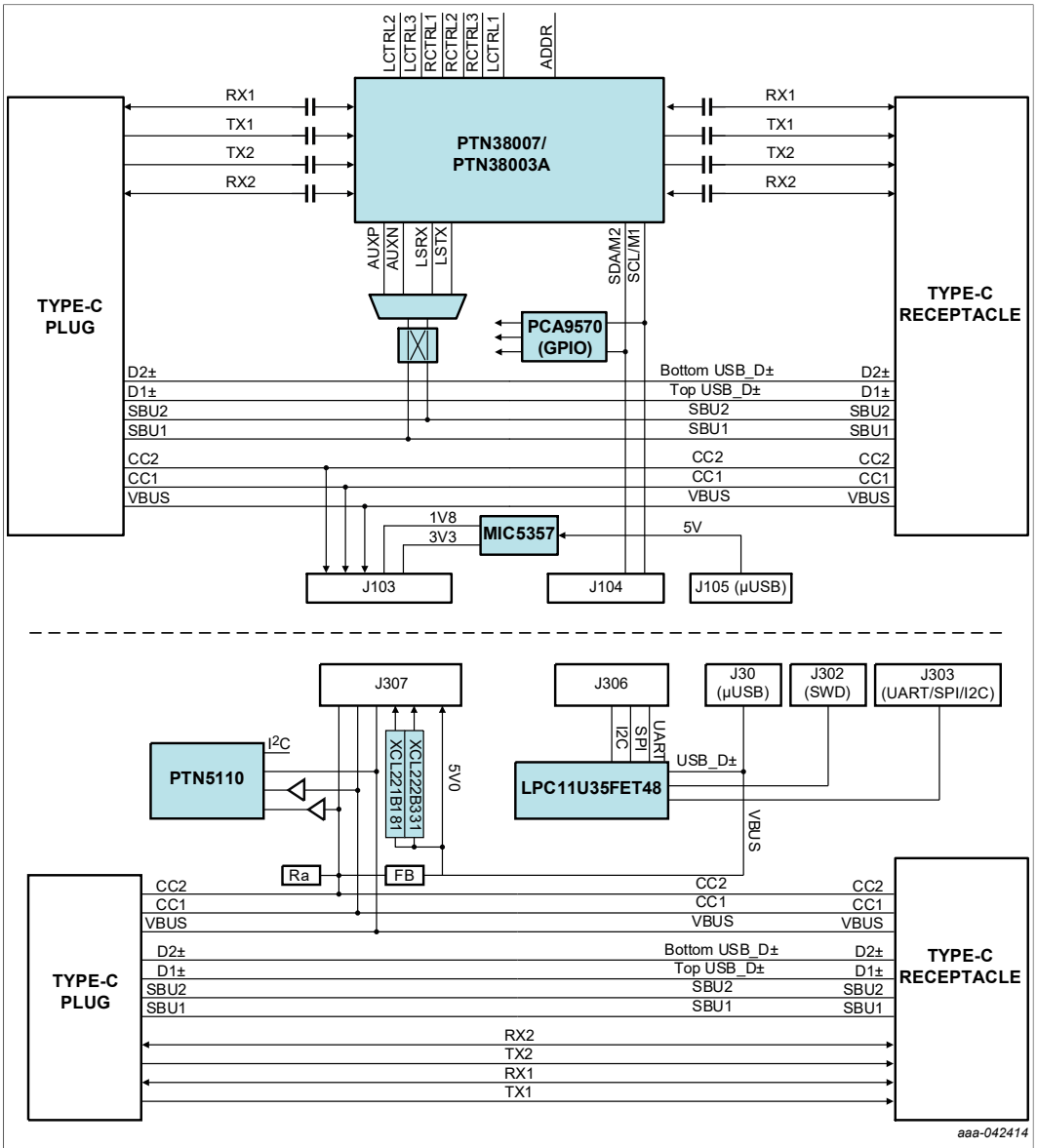



**Figure 13. Block diagram**

## 6.2 PCB photo


**Figure 14. PTN5110 sniffer board; front side**

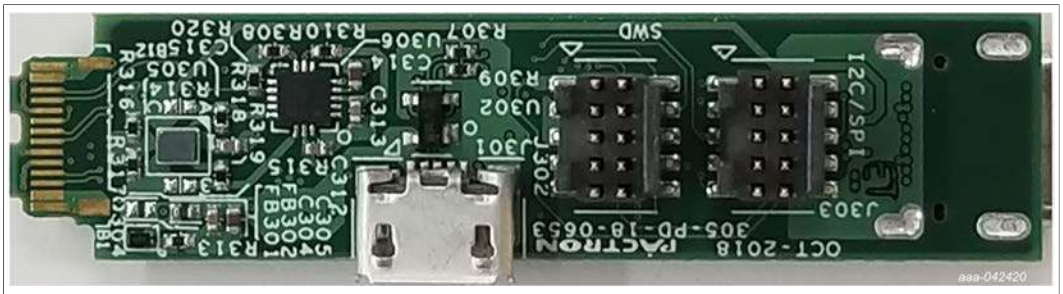



**Figure 15. PTN5110 sniffer board; back side**

## 6.3 Connection

PTN38007/3A-EVM evaluation board and LPCUSBSIO module should be sandwiched together such that J103 is mated with J307, and J104 is mated with J306. There is no Type-C plug installed on the LPCUSBSIO module by default, and J305 (Type-C receptacle) on the LPCUSBSIO module should not be used. This forces the user to use only J101 to connect to host side, and J102 to connect to device side.

A micro-USB cable should be connected to J301 on the LPCUSBSIO module to provide power to the entire setup. This USB cable allows the use of NXP's LPCUSBSIO USB-2-$I^2C$ bridge to communicate with PTN38007/3's $I^2C$ via USB2 interface. The Aardvark I2C/SPI host adapter can be connected to the setup using a 50 mil spacing 10-pin cable on LPCUSBSIO module's J303.

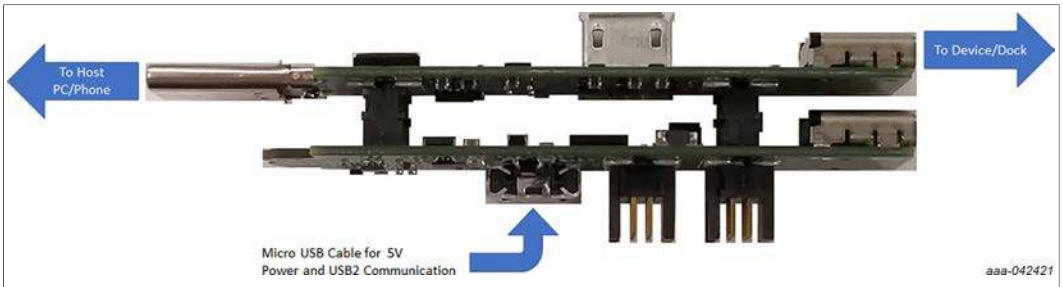


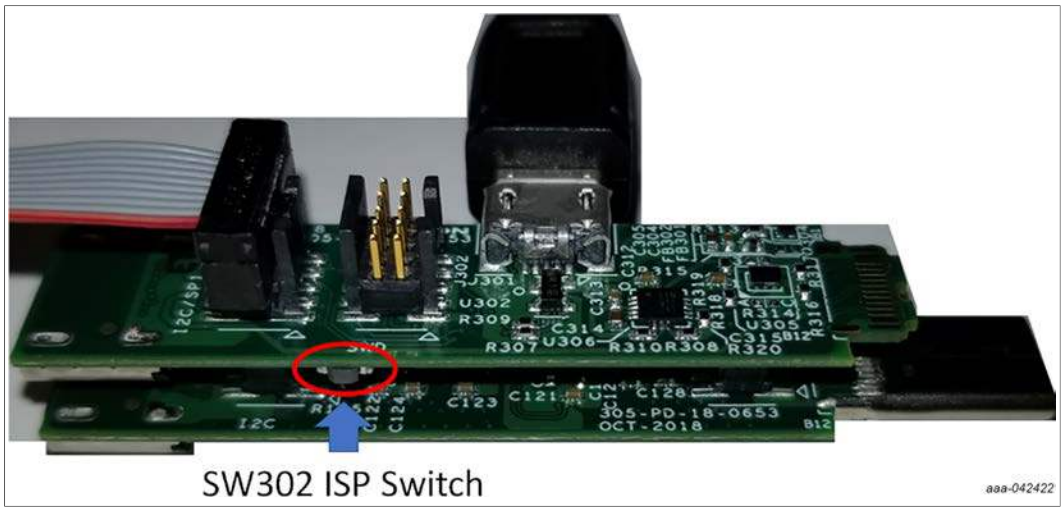

**Figure 16. Connection of PTN38007/3A-EVM evaluation board and LPCUSBSIO module**

## 6.4 Firmware update

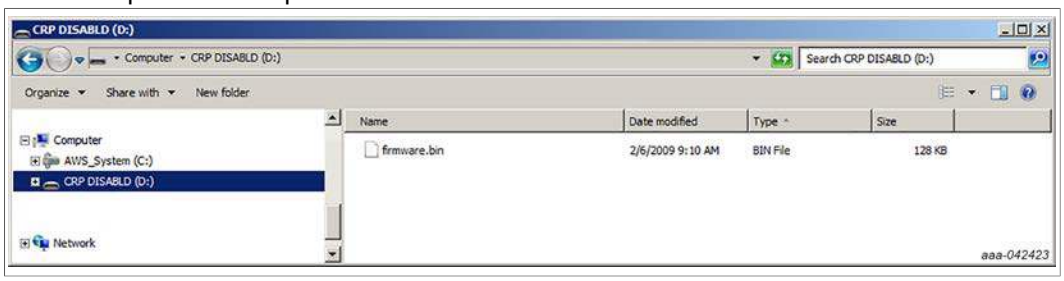
From time to time, NXP provides the latest firmware update for the EVM to fix issues found in the code. Follow these steps to perform the firmware upgrade:

1. Connect a micro-USB cable to J301 first, without plugging into the PC.

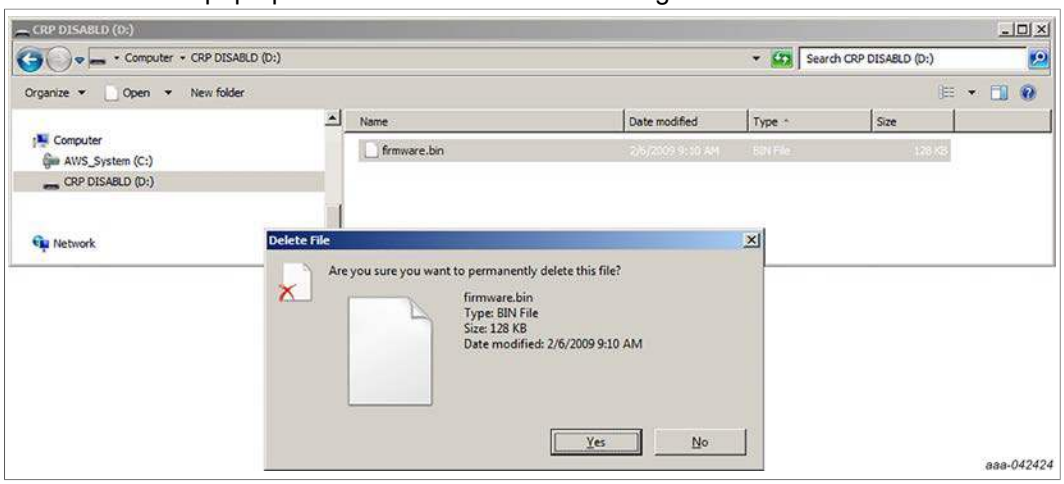
2. Locate SW302 ISP switch on the sniffer board, and hold it down while plugging in the micro-USB cable to the PC.



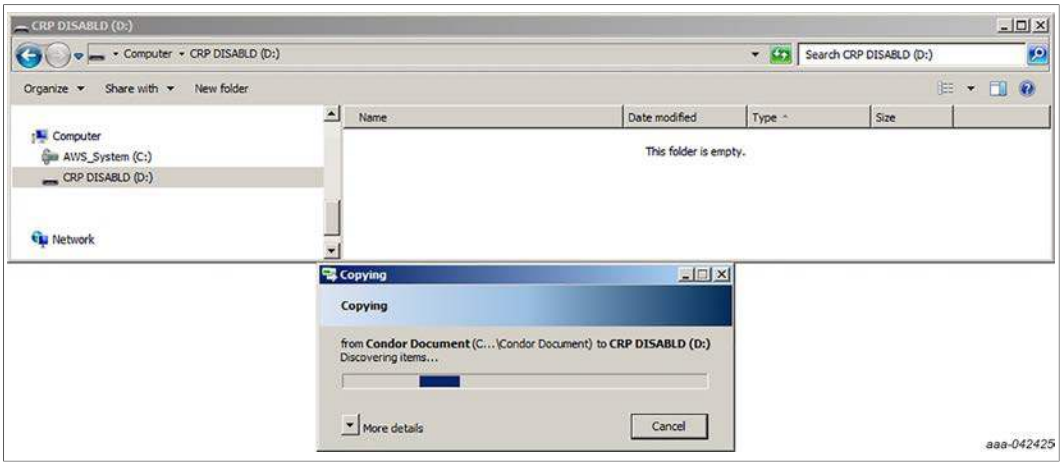

3. Release SW302 switch, and on your PC, you will see a disk drive “CRP DISABLD” show up under “computer.”



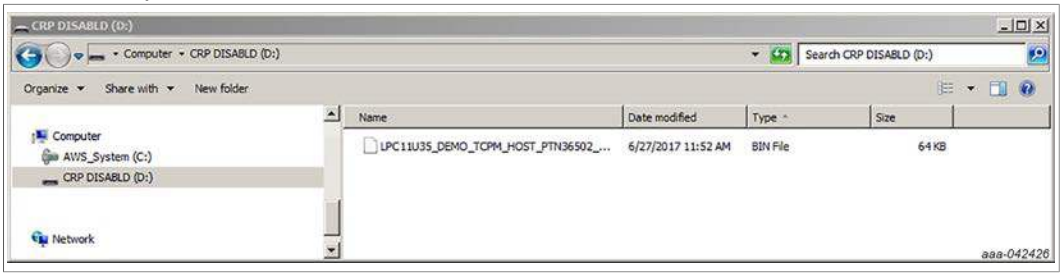

4. Right click “firmware.bin” in the “CRP DISABLD” driver, and select Delete. Select “Yes” when a pop up window asks to confirm deleting the file.



5. Locate the new firmware on your hard drive (with .bin extension), and drag the file into “CRP DISABLD” folder.




6. The new binary file should appear in the “CRP DISABLD” drive. The firmware update is completed. Remove and then reinsert the micro-USB cable from your computer to emulate power on reset condition.




7. The new firmware is now running on the LPCUSBSIO module.

# 7 GUI introduction

The I$^2$C GUI control interface can be used to monitor and change the PTN38007/3A registers, as well as configure the GPIO expander. This tool can be used in stand-alone mode, or concurrently with LPCUSBSIO module plug in.

## 7.1 List of files

The GUI zip file contains the following:

**Table 6. GUI zip file contents**

| | |
|---|---|
| `Drake.exe` | GUI executable. Click on this file to run the GUI. |
| `liblpcusbsio.dll` | LPCUSBSIO library |
| `Script_File.txt` | A list of default script files to be loaded when GUI is open. User may edit this file to change default scripts to be loaded. |
| `PTN38007/3.txt`<br>`PTN38003A.txt` | Default product script file(s). If the file exists, for each matched product type that is found during I$^2$C address search, the corresponding product script is executed once. These script files are useful to set up default equalizer settings. |

**Table 6. GUI zip file contents**...*continued*

| | |
|---|---|
| P2R_DFP_USB_2DP_Normal.txt<br>P2R_DFP_USB_2DP_Reversed.txt<br>P2R_DFP_4DP_Normal.txt<br>P2R_DFP_4DP_Reversed.txt<br>P2R_DFP_TBT_Normal.txt<br>P2R_DFP_TBT_Reversed.txt<br>P2R_DFP_USB4_Normal.txt<br>P2R_DFP_USB4_Reversed.txt | Script files for PTN38007/3/PTN38003A DFP Board<br>P2R_DFP_TBT_Normal/Reversed.txt and P2R_DFP_USB4_Normal/Reversed.txt are only applicable to PTN38007/3 |
| P2R_UFP_USB_2DP_Normal.txt<br>P2R_UFP_USB_2DP_Reversed.txt<br>P2R_UFP_4DP_Normal.txt<br>P2R_UFP_4DP_Reversed.txt<br>P2R_UFP_TBT_Normal.txt<br>P2R_UFP_TBT_Reversed.txt<br>P2R_UFP_USB4_Normal.txt<br>P2R_UFP_USB4_Reversed.txt | Script files for PTN38007/3/PTN38003A UFP Board<br>P2R_UFP_TBT_Normal/Reversed.txt and P2R_UFP_USB4_Normal/Reversed.txt are only applicable to PTN38007/3 |

### 7.1.1 Editing Script_File.txt

The Script_File.txt can be edited to load up to eight script files in the GUI. The list in the GUI is refreshed when the GUI is first executed, or when **I2C Reset** is clicked. Note that the following rules should be applied when editing the file:

- One entry per line.
- A blank line is counted as an entry without any file name loaded.
- Only the first eight lines/entries will be loaded; entries after line eight are discarded.
- When populating entries, it is the user's responsibility to check if these script file entries exist in the current directory. The GUI checks if the entry is valid when clicking the script file name.

## 7.2 GUI fields

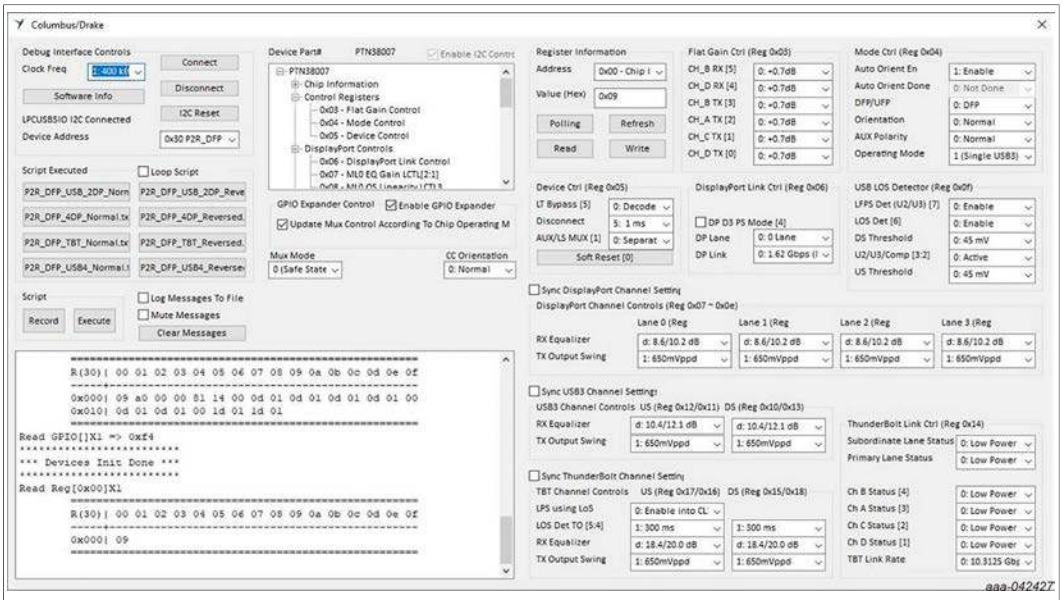



**Figure 17. GUI fields**

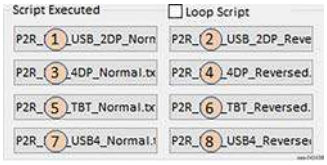
### 7.2.1 Interface

**Table 7. Interface**

| | |
|---|---|
| **Connect / Disconnect** | When the LPCUSBSIO module is disconnected from the PC (in the event of power cycle the evaluation board, or remove USB2 cable from the module), user should first click on **Disconnect** then **Connect** to reinitialize the LPCUSBSIO module. |
| **I2C Reset** | When clicked, all possible $I^2C$ addresses in this product family are rescanned, evaluation board type is determined, the default product script (if present) is executed, and respective register values are updated on the screen. |
| **Clock Freq** | $I^2C$-bus interface clock frequency. Default is set to 400 kHz. The interface frequency can be changed by the user at any time, as long as the clock speed is supported. |
| **Device Address** | This field shows the evaluation board type and/or a list of product $I^2C$ addresses found in the current setup.<br>• 0x30 P2R_DFP – $I^2C$ Address = 0x30<br>• 0x33 P2R_UFP – $I^2C$ Address = 0x33 |

### 7.2.2 Script files

**Table 8. Script files**

| | |
|---|---|
| List of eight script files | The default scripts are populated in the following order:<br>**Script #1** **Script #2**<br>**Script #3** **Script #3**<br>**Script #5** **Script #6**<br>**Script #7** **Script #8**<br>  |
| **Loop Script** | When checked, scripts are executed in the order of #1, #2, #3, #4, #5, #6, #7, #8, and going back to #1. If a certain script file entry is empty, that entry is skipped.<br>Script execution is stopped when it is unchecked. |
| **Execute** | Click on this to load a script that is not on the current populated fields. New script file name is also populated in the order of #1, #2, #3, #4, #5, #6, #7, #8 and going back to #1 again. |
| **Record** | It is possible to record current $I^2C$ register reads/writes into a script file. |

### 7.2.3 Messages

**Table 9. Messages**

| | |
|---|---|
| **Log Messages To File** | When checked, a log file with current date/time stamp is created. All messages will be logged in the file.<br>Uncheck this to cancel file logging function. |
| **Mute Messages** | When checked, most $I^2C$ read/write messages are not displayed in the message window ($I^2C$ read/write errors are always displayed, and can't be turned off). This reduces the time gap between $I^2C$ read/write transactions. |
| **Clear Messages** | Clear messages in the message window. |
| **Message Window** | |

### 7.2.4 Register information

**Table 10. Register information**

| | |
|---|---|
| **Address** | The field indicates the register address to be accessed. User can either select the value from the pull down menu, or click on a register address under the register tree. |
| **Value (Hex)** | Register value read out or to be written from/to the register address above. |
| **Read** | Perform a read operation from register address above. Read out value is populated in the **Value (Hex)** box. |
| **Write** | Perform a write operation to register address above. Value to be written is loaded from the**Value (Hex)** box. |
| **Polling** | When clicked, a repetitive read operation is performed from register address above. Read out value is populated in the **Value (Hex)** box. Click again to stop the repetitive read operation. |

**Table 10. Register information**...*continued*

| | |
|---|---|
| **Refresh** | When clicked, a repetitive read operation is performed across all registers. Read out values are populated in the GUI directly. Click again to stop the repetitive read operation. |

### 7.2.5 GPIO expander control

**Table 11. GPIO expander control**

| | |
|---|---|
| **Enable GPIO Expander** | When checked, Mux Mode and CC Orientation controls are accessible by user. |
| **Update Mux Control According To Chip Operating Mode** | When checked, Mux Mode and CC Orientation are updated to the same value as device register 0x04 bit [2:0] (Operating Mode) and bit [4] (Orientation) when the bit values are updated in the GUI. (When using scripts to update device register 0x04, GPIO expander values are not updated) |
| **Mux Mode** | This controls the state of on-board SBU crossbar control<br>• 0 (Safe State) – SBU crossbar IOs are tri-stated<br>• 1 (USB Only) – SBU crossbar IOs are tri-stated<br>• 2 (USB + 2 Lane DP) – SBU crossbar IOs are selecting AUX signals<br>• 3 (4 Lane DP) – SBU crossbar IOs are selecting AUX signals<br>• 4 (TBT3) – SBU crossbar IOs are selecting LSTX/LSRX signals<br>• 5 (USB4) – SBU crossbar IOs are selecting LSTX/LSRX signals |
| **CC Orientation** | This controls the orientation of on-board SBU crossbar<br>• 0: Normal<br>• 1: Reversed |

## 7.3 PTN38007/3A register fields setup

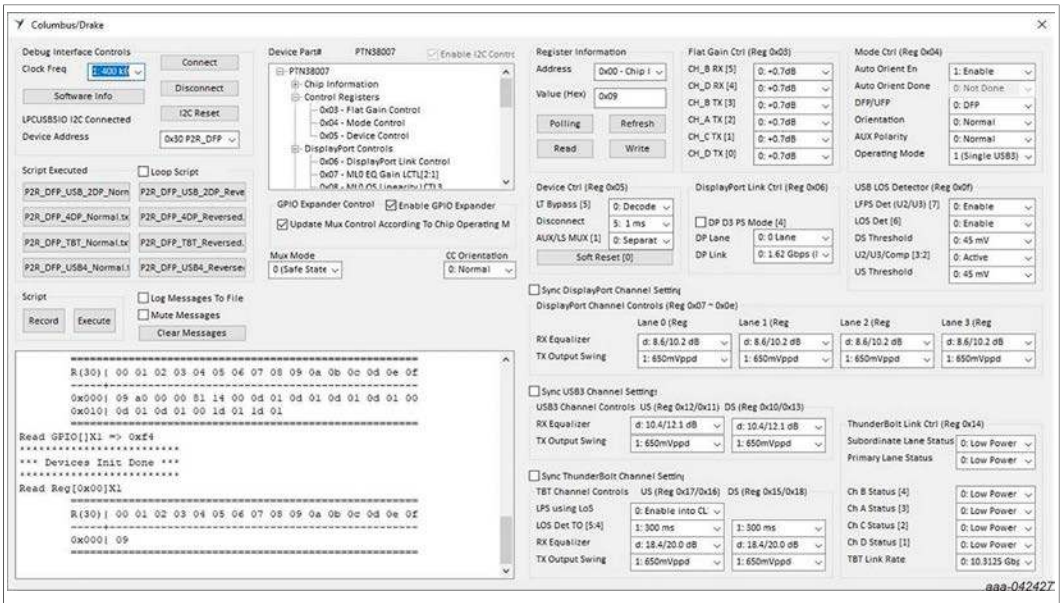



**Figure 18. Register fields setup**

### 7.3.1 Suggested Scrpt_File.txt content

#### 7.3.1.1 DFP board

**Table 12. DFP board**

| | |
|---|---|
| P2R_DFP_USB_2DP_Normal.txt | P2R_DFP_USB_2DP_Reversed.txt |
| P2R_DFP_4DP_Normal.txt | P2R_DFP_4DP_Reversed.txt |
| P2R_DFP_TBT_Normal.txt | P2R_DFP_TBT_Reversed.txt |
| P2R_DFP_USB4_Normal.txt | P2R_DFP_USB4_Reversed.txt |

#### 7.3.1.2 UFP board

**Table 13. UFP board**

| | |
|---|---|
| P2R_UFP_USB_2DP_Normal.txt | P2R_UFP_USB_2DP_Reversed.txt |
| P2R_UFP_4DP_Normal.txt | P2R_UFP_4DP_Reversed.txt |
| P2R_UFP_TBT_Normal.txt | P2R_UFP_TBT_Reversed.txt |
| P2R_UFP_USB4_Normal.txt | P2R_UFP_USB4_Reversed.txt |

## 7.4 Other controls

**Sync DisplayPort Channel Settings**

**Sync USB3 Channel Settings**

**Sync ThunderBolt Channel Settings**

When these options are checked, if one of the Lanes' EQ or OSL (Output Swing Level) settings are changed, the same values (both EQ and OSL) are applied to other lanes.

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## Tables



## Figures

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