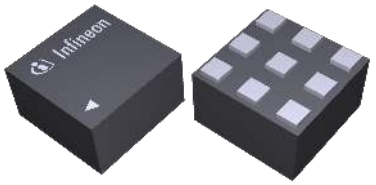
BGS14MPA9

High Linearity, High Power SP4T RF Switch with MIPI 2.0

Key Features

- 0.05 to 6.0 GHz coverage for FM Radio, LTE, LAA and 5G application
- Low Insertion Loss and high isolation up to 6 GHz
- High linearity with ultra low harmonic generation
- Up to 37 dBm operating RF input power
- No decoupling capacitors required if no DC applied on RF lines
- Integrated MIPI RFFE interface
- Software programmable MIPI RFFE USID
- Small form factor 1.1mm x 1.1mm
- Suitable for multi-mode LTE and WCDMA multi antenna applications
- No power supply blocking required
- 50-Ohm termination enabling at isolation mode

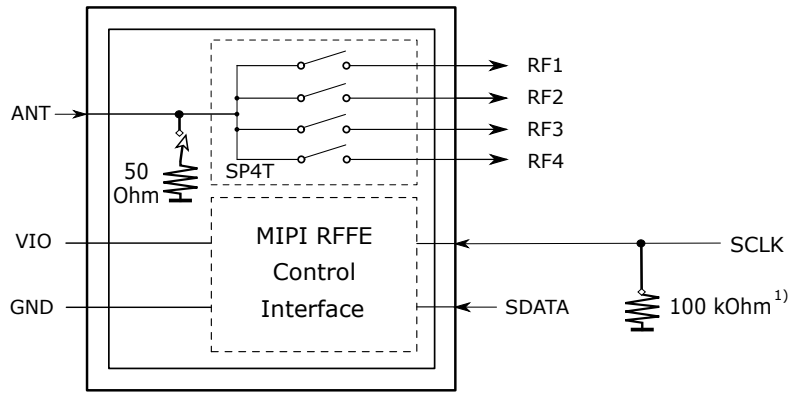


1.1 x 1.1 mm^2

Product Validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Block diagram



1) Pulldown resistor to be used in combination with Qualcomm MIPI interface.
It is also recommended to reserve a footprint for other modem solutions.
For more information, refer to Infineon technical report TR1273: MIPI RFFE Device I/O Structures.

Table of Contents

1 Features

- Ultra low insertion loss 0.3 dB at 2.7 GHz and 1.0 dB at 6 GHz
- High TX Power Handling Capabilities with up to 37 dBm
- 0.05 to 6.0 GHz coverage for FM Radio, LTE, LAA and 5G application
- Low harmonic generation
- High port-to-port-isolation
- On chip control logic including ESD protection
- Fully compatible with MIPI 2.0 RFFE standard operating in 1.65 to 1.95 V voltage range
- Software programmable MIPI RFFE USID
- Small form factor 1.1mm x 1.1mm
- No power supply blocking required
- No decoupling capacitors required (Unless DC applied on RF lines)
- 50-Ohm termination enabling at isolation mode
- High EMI robustness
- RoHS and WEEE compliant package

Description

BGS14MPA9 is a Single Pole Four Throw (SP4T) high power switch in a very compact 9-pin package with very small size of only 1.1x 1.1mm^2 and a maximum thickness of 0.65mm.
Its performance is optimized for 2G / 3G / 4G and 5G cellular applications up to 6.0 GHz. With an ultra low insertion loss, high isolation, high linearity and high power handling, BGS14MPA9 is perfect for LTE 4G applications, such as Uplink-Carrier Aggregation, High Power User Equipment (HPUE Class 2) and 5G sub 6 GHz.
Furthermore the BGS14MPA9 can be applied as 2G / 3G post PA RF-Switch and high-band antenna switch for LTE-U / LAA or LTE band 42 and 43.

Product Name	Marking	Package
BGS14MPA9	C1	ATSLP-9-3

2 Maximum Ratings

Table 1: Maximum Ratings, Table I at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency Range	f	0.05	–	6.0	GHz	[1]
RFFE supply voltage [2]	V_{IO}	-0.5	–	2.2	V	–
Storage temperature range	T_{STG}	-55	–	150	°C	–
RF input power	P_{RF_max}	–	–	38	dBm	At all TRx ports, CW / VSWR 1:1 / 50 Ω
		–	–	25	dBm	50 Ohm Termination / CW
ESD capability, CDM [3]	$V_{ESD_{CDM}}$	-500	–	+500	V	
ESD capability, HBM [4]	$V_{ESD_{HBM}}$	-1	–	+1	kV	
ESD capability, system level[5]	V_{ESD_RF}	-8	–	+8	kV	RF versus system GND, with 27 nH
		-6	–	+6	kV	RF versus system GND, with 56 nH
Junction temperature	T_j	–	–	125	°C	–

[1] Switch has a low-pass response. For higher frequencies, losses have to be considered for their impact on thermal heating. The DC voltage at RF ports V_{RFDC} has to be 0V.
[2] Note: Consider potential ripple voltages on top of V_{IO}. Including RF ripple, V_{IO} must not exceed the maximum ratings: $V_{IO} = V_{DC} + V_{Ripple}$.
[3] Field-Induced Charged-Device Model ANSI/ESDA/JEDEC JS-002. Simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing.
[4] Human Body Model ANSI/ESDA/JEDEC JS-001 (R = 1,5 kΩ, C = 100 pF).
[5] IEC 61000-4-2 (R = 330 Ω, C = 150 pF), contact discharge.

Warning: Stresses above the max. values listed here may cause permanent damage to the device. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. Exposure to conditions at or below absolute maximum rating but above the specified maximum operation conditions may affect device reliability and life time. Functionality of the device might not be given under these conditions.

Table 2: Maximum Ratings, Table II at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance junction - soldering point	R_{thJS}	–	–	70	K/W	–
Maximum DC-voltage on RF-Ports and RF-Ground	V_{RFDC}	0	–	0	V	No DC voltages allowed on RF-Ports

3 Operation range

Table 3: Operation range at T_A = −40 °C to 85 °C

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{IO}	1.65	1.8	1.95	V	–
RFFE input high voltage[1]	V_{IH}	0.7*V_{IO}	–	V_{IO}	V	–
RFFE input low voltage[1]	V_{IL}	0	–	0.3*V_{IO}	V	–
RFFE output high voltage[1]	V_{OH}	0.8*V_{IO}	–	V_{IO}	V	–
RFFE output low voltage[1]	V_{OL}	0	–	0.2*V_{IO}	V	–
RFFE control input capacitance	C_{Ctrl}	–	–	2	pF	–
Supply current	I_{IO}	–	65	150	µA	Operating State
Supply current, stand-by	$I_{IO,sb}$	–	2	–	µA	Idle State, power down mode

[1]SCLK and SDATA

Table 4: RF input power

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RF input power on TRX ports	P_{RF}	–	–	37	dBm	CW / VSWR 1:1 / 50 Ω
RF input power	P_{RF}	–	–	25	dBm	50 Ohm Termination / 0.125 duty cycle

4 RF Characteristics

Table 5: RF Characteristics at T_A = 25 °C, P_{IN} = 0 dBm, Supply Voltage V_{IO} = 1.8V, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Insertion Loss[1]						
All TRx Ports	IL	–	0.18	0.25	dB	50–698 MHz
		–	0.20	0.28	dB	699–960 MHz
		–	0.24	0.35	dB	1200–2170 MHz
		–	0.30	0.45	dB	2171–2690 MHz
		–	0.49	0.75	dB	3300–4200 MHz
		–	0.77	1.05	dB	4400–5000 MHz
		–	1.00	1.50	dB	5150–5925 MHz

[1] On application board without any matching components.

Table 6: RF Characteristics at T_A = −40 °C...85 °C, P_{IN} = 0 dBm, Supply Voltage V_{IO} = 1.65...1.95V, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Insertion Loss[1]						
All TRx Ports	IL	–	0.18	0.3	dB	50–698 MHz
		–	0.20	0.4	dB	699–960 MHz
		–	0.24	0.5	dB	1200–2170 MHz
		–	0.30	0.6	dB	2171–2690 MHz
		–	0.49	0.9	dB	3300–4200 MHz
		–	0.77	1.2	dB	4400–5000 MHz
		–	1.00	1.6	dB	5150–5925 MHz
Return Loss[1]						
All TRx Ports	RL	26	33	–	dB	50–698 MHz
		24	28	–	dB	699–960 MHz
		17	22	–	dB	1200–2170 MHz
		15	19	–	dB	2171–2690 MHz
		10	14	–	dB	3300–4200 MHz
		8	11	–	dB	4400–5000 MHz
		7	10	–	dB	5150–5925 MHz

[1] On application board without any matching components.

Table 7: RF Characteristics at T_A = −40 °C...85 °C, P_{IN} = 0 dBm, Supply Voltage V_{IO} = 1.65...1.95V, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Isolation[1]						
ANT_RF1 vs RFx	ISO	47	59	–	dB	50–698 MHz
		44	51	–	dB	699–960 MHz
		35	42	–	dB	1200–2170 MHz
		32	37	–	dB	2171–2690 MHz
		25	31	–	dB	3300–4200 MHz
		23	28	–	dB	4400–5000 MHz
		22	25	–	dB	5150–5925 MHz
Isolation[1]						
ANT_RF2 vs RFx	ISO	42	53	–	dB	50–698 MHz
		39	46	–	dB	699–960 MHz
		31	39	–	dB	1200–2170 MHz
		29	35	–	dB	2171–2690 MHz
		23	30	–	dB	3300–4200 MHz
		20	27	–	dB	4400–5000 MHz
		18	24	–	dB	5150–5925 MHz
Isolation[1]						
ANT_RF3 vs RFx	ISO	44	55	–	dB	50–698 MHz
		41	47	–	dB	699–960 MHz
		33	39	–	dB	1200–2170 MHz
		31	35	–	dB	2171–2690 MHz
		24	29	–	dB	3300–4200 MHz
		20	26	–	dB	4400–5000 MHz
		18	24	–	dB	5150–5925 MHz
Isolation[1]						
ANT_RF4 vs RFx	ISO	41	55	–	dB	50–698 MHz
		38	47	–	dB	699–960 MHz
		30	38	–	dB	1200–2170 MHz
		27	33	–	dB	2171–2690 MHz
		22	28	–	dB	3300–4200 MHz
		20	25	–	dB	4400–5000 MHz
		18	23	–	dB	5150–5925 MHz
Isolation[1]						
Port to Port	ISO	40	59	–	dB	50–698 MHz
		37	50	–	dB	699–960 MHz
		31	41	–	dB	1200–2170 MHz
		28	36	–	dB	2171–2690 MHz
		22	31	–	dB	3300–4200 MHz
		20	27	–	dB	4400–5500 MHz
		18	25	–	dB	5150–5925 MHz

[1] On application board without any matching components.

Table 8: RF Characteristics at T_A = −40 °C...85 °C, P_{IN} = 0 dBm, Supply Voltage V_{IO} = 1.65...1.95V, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Harmonic Generation[1]						
2nd Harmonic	P_{H2}	–	-70	-60	dBm	35 dBm, 50 Ω, 600–915 MHz
		–	-67	-60	dBm	32 dBm, 50 Ω, 1447–1980 MHz
		–	-80	-75	dBm	26 dBm, 50 Ω, 2300–2690 MHz
3nd Harmonic	P_{H3}	–	-60	-53	dBm	35 dBm, 50 Ω, 600–915 MHz
		–	-63	-59	dBm	32 dBm, 50 Ω, 1447–1980 MHz
		–	-80	-73	dBm	26 dBm, 50 Ω, 2300–2690 MHz
Intermodulation Distortion [1]						
2nd order intermodulation	IMD2	–	-110	-85	dBm	IMD2 Testcases, Tab. 9
3rd order intermodulation	IMD3	–	-95	-85	dBm	IMD3 Testcases, Tab. 10
Intercept point[1]						
2nd order intercept point	IIP2	120	136	–	dBm	IMD2 Testcases, Tab. 9
3rd order intercept point	IIP3	70	77	–	dBm	IMD3 Testcases, Tab. 10

[1] On application board without any matching components.

Table 9: IMD2 Testcases

Band	In-Band Frequency [MHz]	Blocker Frequency 1 [MHz]	Blocker Power 1 [dBm]	Blocker Frequency 2 [MHz]	Blocker Power 2 [dBm]
Band 1	2140	1950	24	4090	-15
Band 2	1960	1880	24	3840	-15
Band 5	881.5	836.5	20	1718	20
Band 7	2652	2535	24	5187	-15
Band 8	942	897	20	1839	20

Table 10: IMD3 Testcases

Band	In-Band Frequency [MHz]	Blocker Frequency 1 [MHz]	Blocker Power 1 [dBm]	Blocker Frequency 2 [MHz]	Blocker Power 2 [dBm]
Band 1	2140	1950	20	1760	20
Band 2	1960	1880	20	1800	20
Band 5	881.5	836.5	20	791.5	20
Band 7	2655	2535	20	2415	20
Band 8	942	897	20	852	20
Band 1	2132	1732	24	1332	-15

Table 11: Switching Time at T_A = 25 °C, P_{IN} = 0 dBm, Supply Voltage V_{IO} = 1.65...1.95V, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Switching Time						
Power Up Settling Time	t_{PUP}	–	10	20	µs	After power down mode
Switching Time	t_{ST}	–	3.5	4.5	µs	50% last SCLK falling edge to 90% RF signal, ref. to Fig. 1
RF Rise Time	t_{RT}	–	–	1	µs	10 % to 90 % RF signal

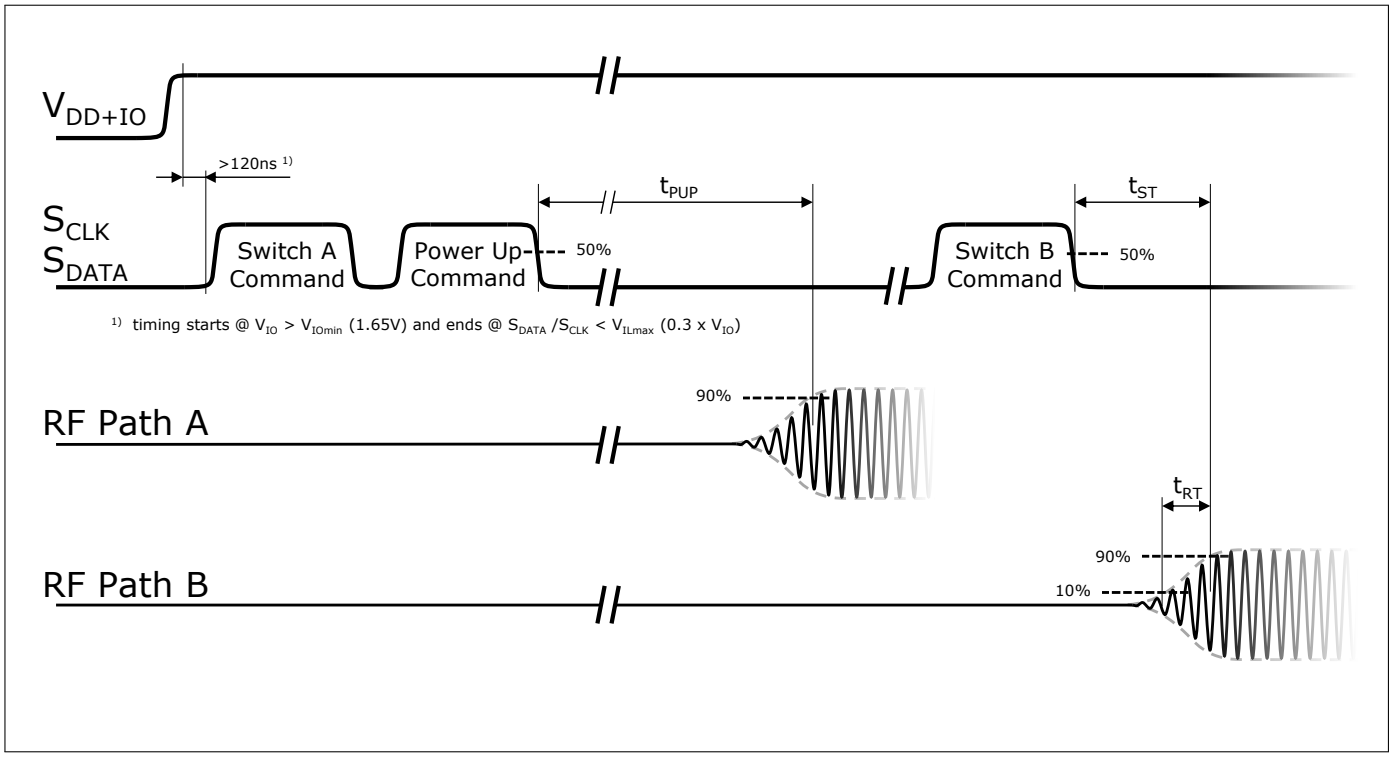


Figure 1: MIPI to RF time

5 MIPI RFFE Specification

The MIPI RFFE interface is working in systems following the 'MIPI Alliance Specification for RF Front-End Control Interface version 2.0 - 25. September 2014' as well as the 'Qualcomm RFFE Vendor specification 80-N7876-1 Rev. T'

Table 12: MIPI Features

Feature	Supported	Comment
MIPI RFFE 1.10 and 2.0 standards	Yes	
Register 0 write command sequence	Yes	
Register read and write command sequence	Yes	
Extended register read and write command sequence	Yes	
Support for standard frequency range operations for SCLK	Yes	Up to 26 MHz for read and write
Support for extended frequency range operations for SCLK	Yes	Up to 52 MHz for write[1)]
Half speed read	Yes	
Full speed read	Yes	
Full speed write	Yes	
Programmable Group SID	Yes	
Trigger functionality	Yes	
Broadcast / GSID write to PM TRIG register	Yes	
Reset	Yes	Via VIO, PM TRIG or software register[1)]
Status / error sum register	Yes	
Extended product ID register	Yes	
Revision ID register	Yes	
Group SID register	Yes	
USID_Sel pin	No	External pin for changing USID is not implemented
SDATA / SCLK swap	Yes	0xA or 0xB depending on the SCLK/SDATA connection

[1)] only supported by MIPI 2.0 Standard

Table 13: Startup Behavior

Feature	State	Comment
Power status	Power down mode	Power down mode after start-up
Trigger function	Enabled	Enabled after start-up. Programmable via behavior control register

Table 14: Register Mapping, Table I

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x00	SW_CTRL0	6:0	SW_CTRL0	RF Switch Control	0	No	Yes, Trigger0/1/2	R/W
0x1C	PM_TRIG	7	PWR_MODE(1), Operation Mode	0: Normal operation (ACTIVE)	1	Yes	No	R/W
				1: Low Power Mode (LOW POWER)				
		6	PWR_MODE(0), State Bit Vector	0: No action (ACTIVE)	0			
				1: Powered Reset (STARTUP to ACTIVE to LOW POWER)				
		5	TRIGGER_MASK_2	0: Data masked (held in shadow REG)	0	No		
				1: Data not masked (ready for transfer to active REG)				
		4	TRIGGER_MASK_1	0: Data masked (held in shadow REG)	0			
				1: Data not masked (ready for transfer to active REG)				
		3	TRIGGER_MASK_0	0: Data masked (held in shadow REG)	0			
				1: Data not masked (ready for transfer to active REG)				
		2	TRIGGER_2	0: No action (data held in shadow REG)	0	Yes		
				1: Data transferred to active REG				
		1	TRIGGER_1	0: No action (data held in shadow REG)	0			
				1: Data transferred to active REG				
		0	TRIGGER_0	0: No action (data held in shadow REG)	0			
				1: Data transferred to active REG				
0x1D	PRODUCT_ID	7:0	PRODUCT_ID	This is a read-only register. However, during the programming of the USID a write command sequence is performed on this register, even though the write does not change its value.	0x1A	No	No	R
0x1E	MAN_ID	7:0	MANUFACTURER_ID [7:0]	This is a read-only register. However, during the programming of the USID, a write command sequence is performed on this register, even though the write does not change its value.	0x1A	No	No	R
0x1F	MAN_USID	7:6	RESERVED	Reserved for future use	00	No	No	R
		5:4	MANUFACTURER_ID [9:8]	These bits are read-only. However, during the programming of the USID, a write command sequence is performed on this register even though the write does not change its value.	01			
		3:0	USID[3:0]	Programmable USID. Performing a write to this register using the described programming sequences will program the USID in devices supporting this feature. These bits store the USID of the device.	**USID:0xA** Nominal SCLK & SDATA **USID:0xB** Swap SCLK & SDATA	No	No	R/W

Table 15: Register Mapping, Table II

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x20	EXT_PROD_ID[1)]	7:0	EXT_PRODUCT_ID		0x00	No	No	R
0x21	REV_ID	7:4	MAIN_REVISION		0x4	No	No	R/W
		3:0	SUB_REVISION		0x0			
0x22	GSID[1)]	7:4	GSID0[3:0]	Primary Group Slave ID.	0x0	No	No	R/W
		3:0	RESERVED	Reserved for secondary Group Slave ID.	0x0			
0x23	UDR_RST	7	UDR_RST	Reset all configurable non-RFFE Reserved registers to default values. 0: Normal operation 1: Software reset	0	No	No	R/W
		6:0	RESERVED	Reserved for future use	0000000			
0x24	ERR_SUM[1)]	7	RESERVED	Reserved for future use	0	No	No	R
		6	COMMAND_FRAME_PAR_ERR	Command Sequence received with parity error — discard command.	0			
		5	COMMAND_LENGTH_ERR	Command length error.	0			
		4	ADDRESS_FRAME_ PAR_ERR	Address frame with parity error.	0			
		3	DATA_FRAME_PAR_ERR	Data frame with parity error.	0			
		2	READ_UNUSED_REG	Read command to an invalid address.	0			
		1	WRITE_UNUSED_REG	Write command to an invalid address.	0			
		0	BID_GID_ERR	Read command with a BROADCAST_ID or GROUP_ID.	0			
0x2B	BUS_LD	7:4	RESERVED	Reserved for future use	0x0	No	No	R/W
		3:0	Set approximate bus load	0x0: 5 pF	0x7			
				0x1: 7 pF				
				0x2: 10 pF				
				0x3: 15 pF				
				0x4: 20pF				
				0x5: 30 pF				
				0x6: 40 pF				
				0x7: 50pF				
				0x8-0xF: Spare				

[1)] Only supported by MIPI 2.0 Standard

Table 16: Modes of Operation (Truth Table, Register_0)

			REGISTER Bits							
State	**Value (Hex.)**	**Mode**	**D7**[1)]	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	0x00	ALL OFF (Isolation)	0	0	0	0	0	0	0	0
2	0x01	RF1 ON	0	0	0	0	0	0	0	1
3	0x02	RF2 ON	0	0	0	0	0	0	1	0
4	0x04	RF3 ON	0	0	0	0	0	1	0	0
5	0x08	RF4 ON	0	0	0	0	1	0	0	0
6	0x10	ALL OFF (Isolation) with 50 Ohm termination	0	0	0	1	0	0	0	0

[1)] Reserved

6 Package related information

The switch has a package size of 1100 µm in x-dimension and 1100 µm in y-dimension with a maximum deviation of ±50 µm in each dimension. Fig. 2 shows the footprint from top view. The definition of each pin can be found in Tab. 18.

Table 17: Mechanical Data

Parameter	Symbol	Value	Unit
Package X-Dimension	X	1100 ± 50	µm
Package Y-Dimension	Y	1100 ± 50	µm
Package Height	H	650 max	µm

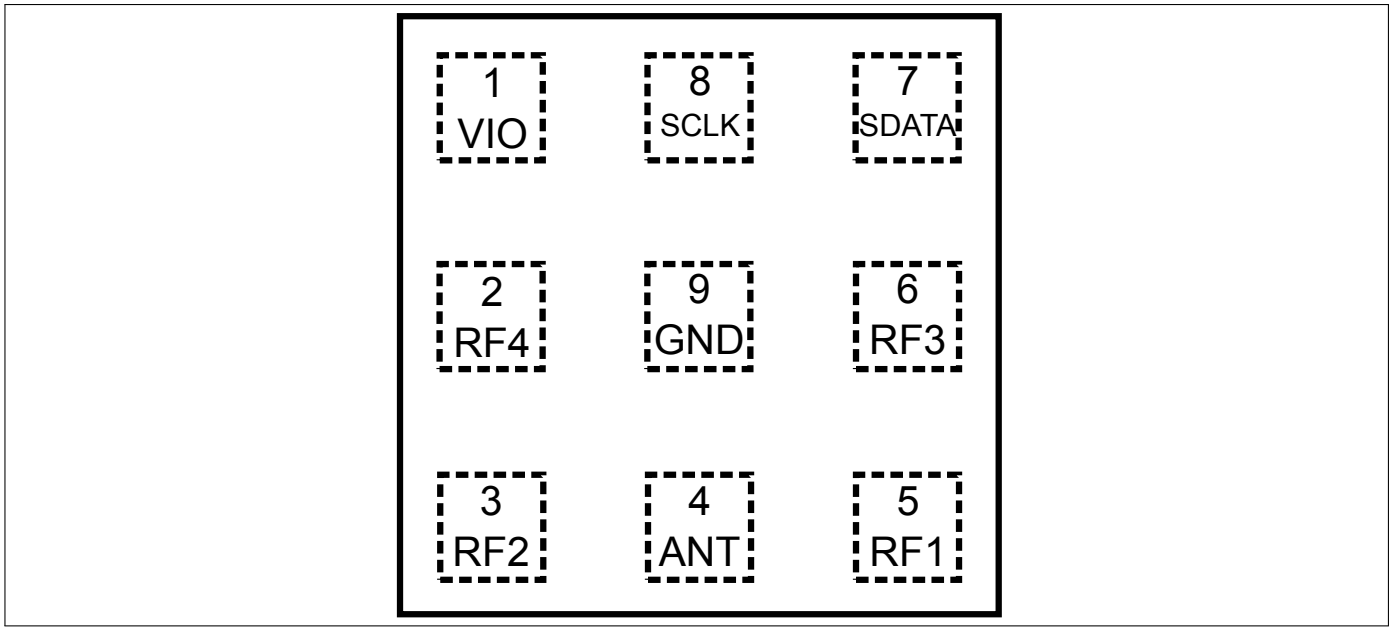


Figure 2: Footprint, top view

Table 18: Pin Definition

No.	Name	Pin Type	Function
1	VIO	Power	Power Supply
2	RF4	RF	Rx port
3	RF2	RF	Rx port
4	ANT	RF	RF Input
5	RF1	RF	Rx port
6	RF3	RF	Rx port
7	SDATA	I/O	MIPI RFFE
8	SCLK	I/O	MIPI RFFE Clock (Input)
9	GND	Ground	Ground

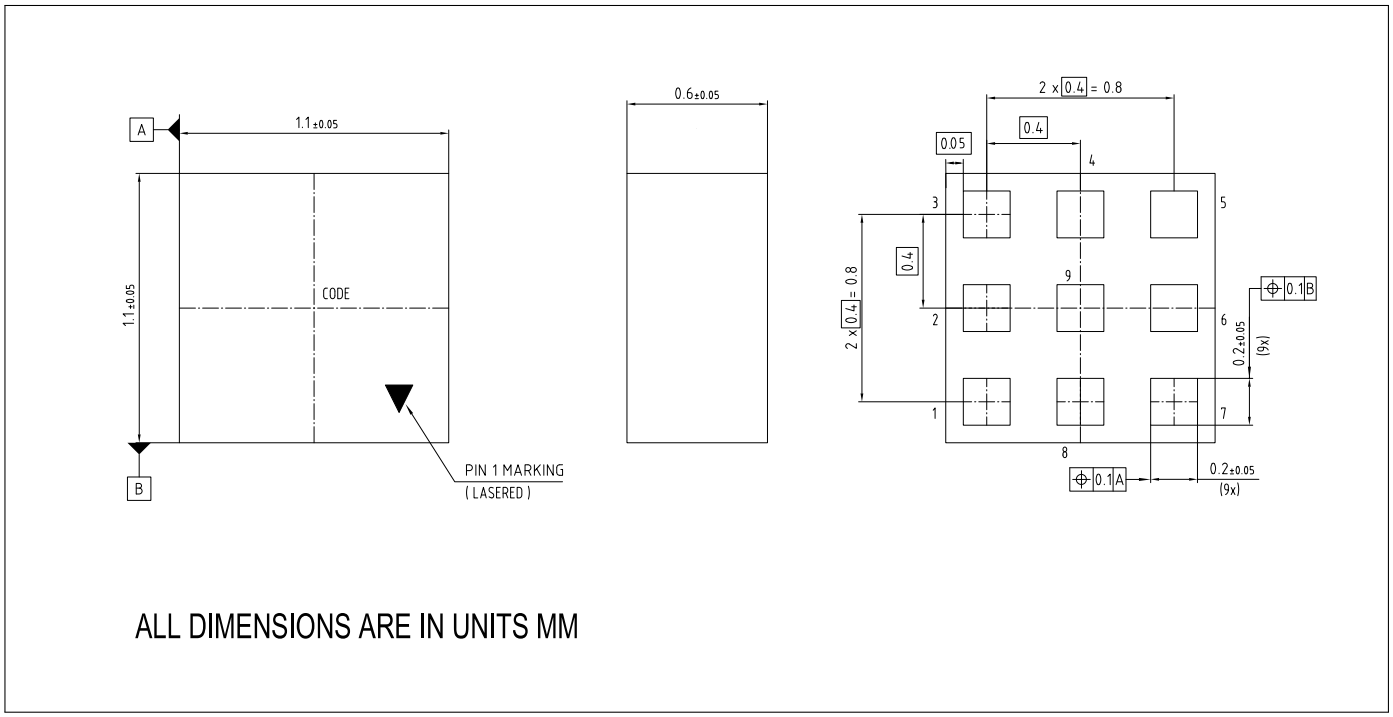


Figure 3: Package Outline Drawing (top, side and bottom views)

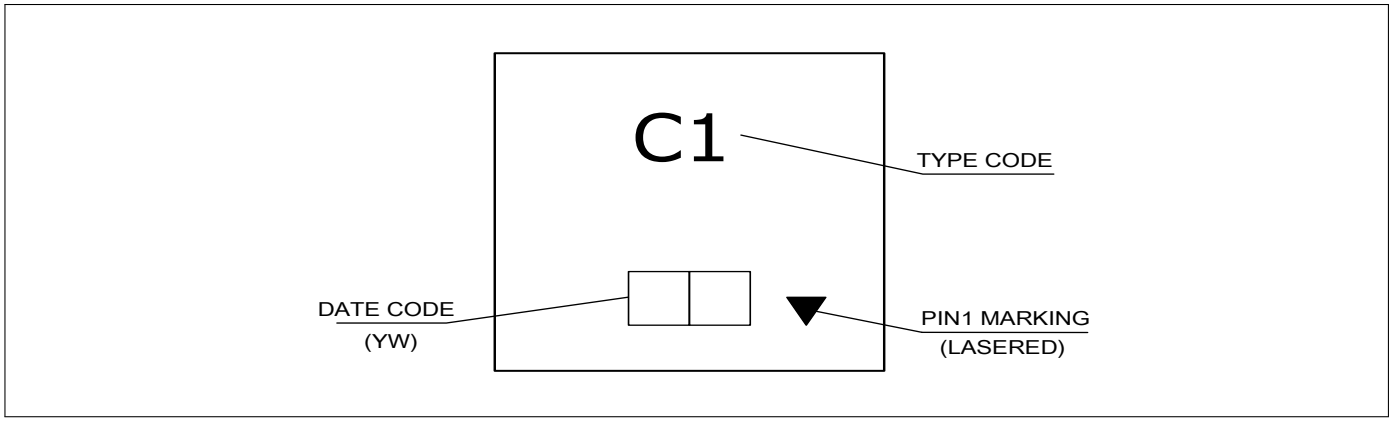


Figure 4: Marking Specification (top view): Date code digits Y and W defined in Table 19/20

Table 19: Year date code marking - digit "Y"

Year	"Y"	Year	"Y"	Year	"Y"
2010	0	2020	0	2030	0
2011	1	2021	1	2031	1
2012	2	2022	2	2032	2
2013	3	2023	3	2033	3
2014	4	2024	4	2034	4
2015	5	2025	5	2035	5
2016	6	2026	6	2036	6
2017	7	2027	7	2037	7
2018	8	2028	8	2038	8
2019	9	2029	9	2039	9

Table 20: Week date code marking - digit "W"

Week	"W"	Week	"W"	Week	"W"	Week	"W"	Week	"W"
1	A	12	N	23	4	34	h	45	v
2	B	13	P	24	5	35	j	46	x
3	C	14	Q	25	6	36	k	47	y
4	D	15	R	26	7	37	l	48	z
5	E	16	S	27	a	38	n	49	8
6	F	17	T	28	b	39	p	50	9
7	G	18	U	29	c	40	q	51	2
8	H	19	V	30	d	41	r	52	3
9	J	20	W	31	e	42	s		
10	K	21	Y	32	f	43	t		
11	L	22	Z	33	g	44	u		

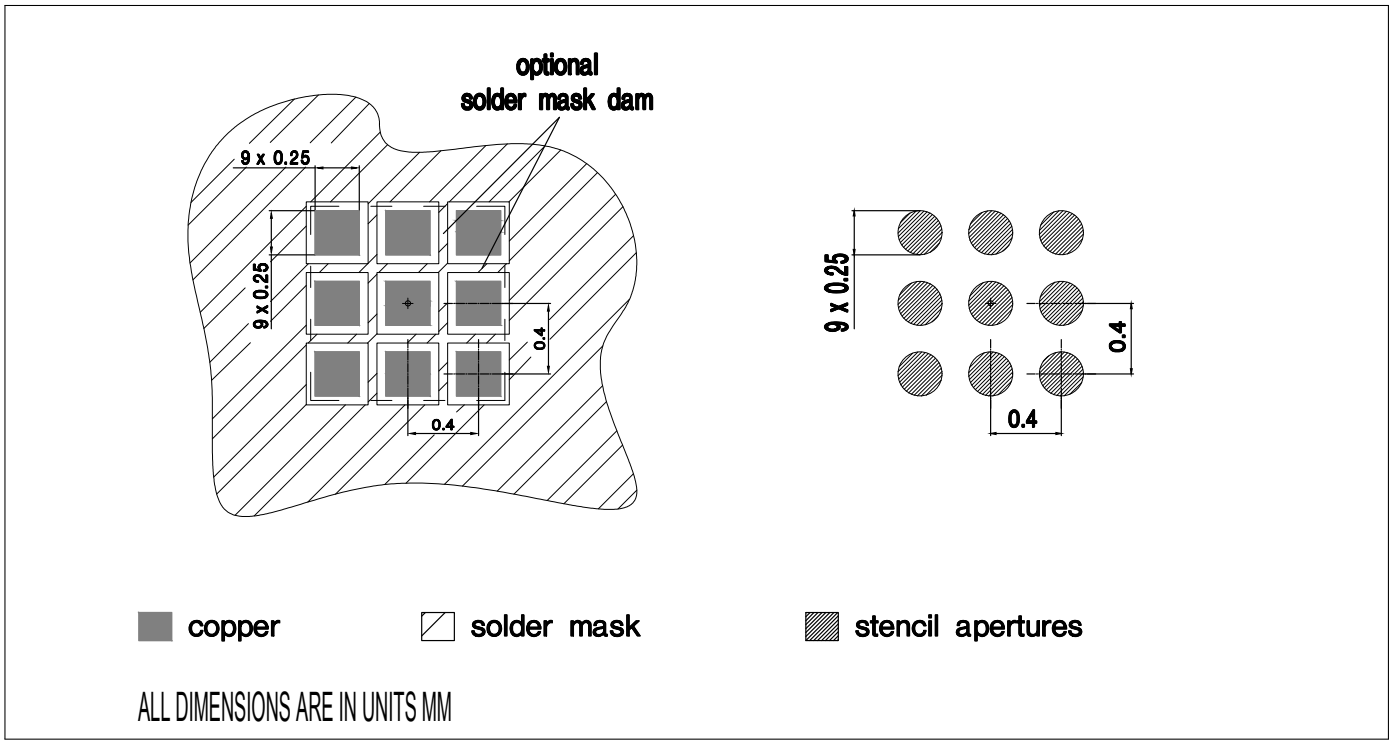


Figure 5: Footprint Recommendation

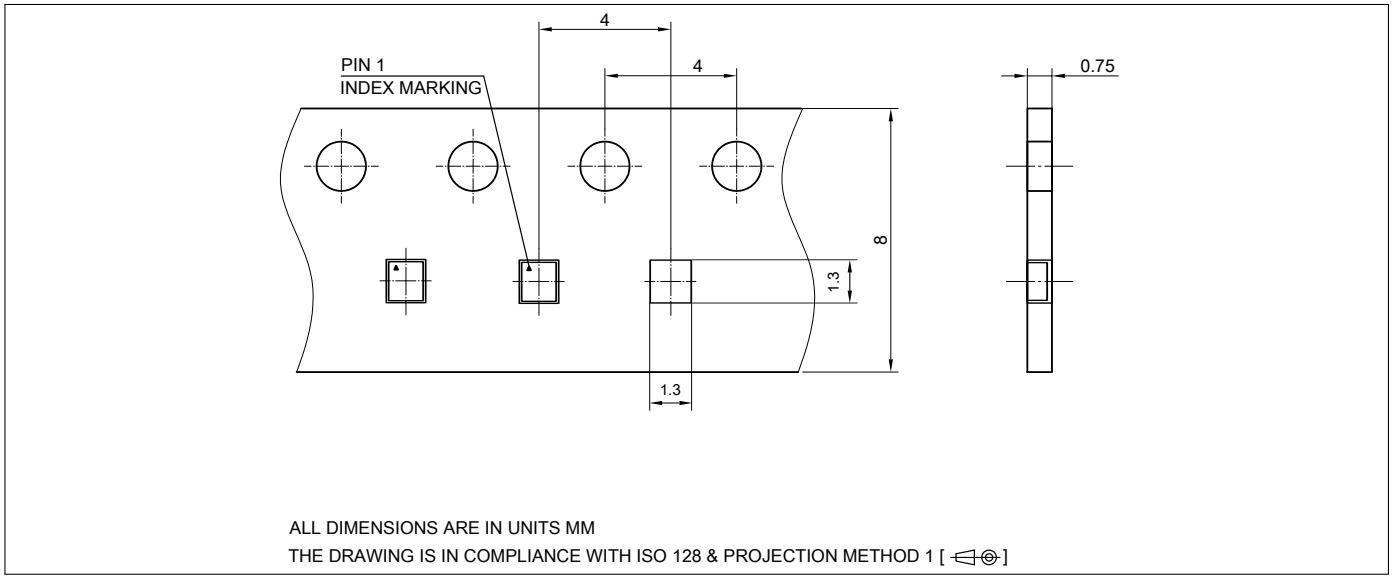


Figure 6: Carrier Tape

Revision History	
Revision 2.11, 2018-12-27	
Page or Item	**Subjects (major changes since previous revision)**
Revision 2.12, 2020-12-17	
Title page	Block diagram with note

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