

MOSFET – Power, Single N-Channel 40 V, 1.07 mΩ, 531 A

NVMJSTOD9N04C

Features

- Small Footprint (5x7 mm) for Compact Design
- Low R_{DS(on)} to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- TCPAK57 Top Cool Package (TCPAK10)
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V _{DSS}	40	٧
Gate-to-Source Voltage			V _{GS}	±20	V
Continuous Drain Current R _{B.IC}	Steady State	T _C = 25°C	I _D	531	Α
(Notes 1, 3)	State	T _C = 100°C		376	
Power Dissipation		T _C = 25°C	P _D	555	W
R _{θJC} (Note 1)		T _C = 100°C		278	
Pulsed Drain Current	$T_A = 25^{\circ}C, t_p = 10 \ \mu s$		I _{DM}	900	Α
Operating Junction and Storage Temperature Range			T _J , T _{stg}	–55 to + 175	ç
Source Current (Body Diode)			Is	463	Α
Single Pulse Drain-to-Source Avalanche Energy (I _{L(pk)} = 34 A)			E _{AS}	578	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			TL	260	°C

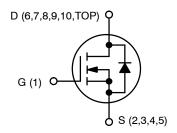
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State	$R_{\theta JC}$	0.27	°C/W
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	28.5	
Junction-to-Drain Lead	$\Psi_{\sf JL}$	4.7	
Junction-to-Source Lead	$\Psi_{\sf JL}$	5.1	
Junction-to-Heatsink Top (Note 2)	Ψ_{JH}	1.3	

- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- 2s2p JEDEC51-7 standard PCB mounted to a 25x25x3 (mm) aluminum heatsink with a 12 w/mK TIM interface.
- Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

V _{(BR)DSS}	R _{DS(ON)} MAX	I _D MAX
40 V	1.07 mΩ @ 10 V	531 A

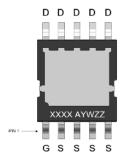


N-CHANNEL MOSFET



TCPAK10 5.1x7.5 CASE 760AG

MARKING DIAGRAM



XXXX = Specific Device Code A = Assembly Location

Y = Year W = Work Week

ZZ = Assembly Lot Code

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

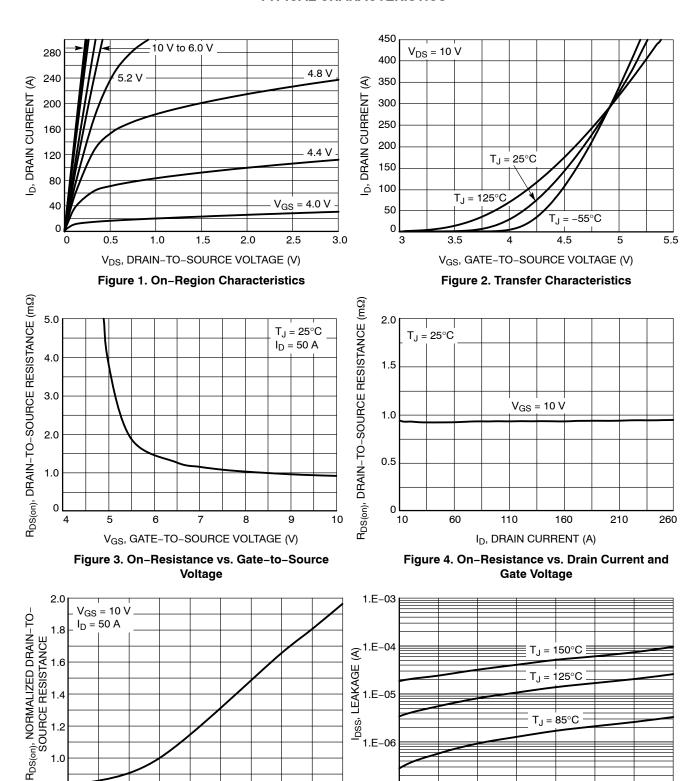
ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}C$ unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS				•	•	•	•
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} / T _J				16		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V,	T _J = 25 °C			10	μΑ
		$V_{DS} = 40 \text{ V}$	T _J = 125°C			100	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = 20 V				100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}, I_D =$	= 190 μΑ	2.5		3.5	V
Threshold Temperature Coefficient	V _{GS(TH)} /T _J				-7		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 50 A		0.92	1.07	mΩ
Forward Transconductance	9 _{FS}	V _{DS} =15 V, I _D	= 50 A		190		S
CHARGES, CAPACITANCES & GATE RE	SISTANCE						
Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1 MHz, V _{DS} = 25 V			6100		pF
Output Capacitance	C _{OSS}				3400		1
Reverse Transfer Capacitance	C _{RSS}				70		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 32 V; I _D = 50 A			86		nC
Threshold Gate Charge	Q _{G(TH)}	V _{GS} = 10 V, V _{DS} = 32 V; I _D = 50 A			18		
Gate-to-Source Charge	Q _{GS}				28		
Gate-to-Drain Charge	Q_{GD}				14		
Plateau Voltage	V _{GP}				4.9		V
SWITCHING CHARACTERISTICS (Note 5	5)						
Turn-On Delay Time	t _{d(ON)}	V_{GS} = 10 V, V_{DS} = 32 V, I_{D} = 50 A, R_{G} = 2.5 Ω			54		ns
Rise Time	t _r				162		
Turn-Off Delay Time	t _{d(OFF)}				227		
Fall Time	t _f				173		
DRAIN-SOURCE DIODE CHARACTERIS	TICS						
Forward Diode Voltage	V_{SD}	V _{GS} = 0 V,	T _J = 25°C		0.8	1.2	V
		I _S = 50 A	T _J = 125°C		0.65		
Reverse Recovery Time	t _{RR}	V_{GS} = 0 V, dIS/dt = 100 A/ μ s, I_{S} = 50 A			91		ns
Charge Time	ta				42		
Discharge Time	t _b				49		
Reverse Recovery Charge	Q _{RR}				159		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions. 4. Pulse Test: pulse width \leq 300 μ s, duty cycle \leq 2%.

^{5.} Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS



T_J, JUNCTION TEMPERATURE (°C)

Figure 5. On-Resistance Variation with

Temperature

8.0

-50 -25

V_{DS}, DRAIN-TO-SOURCE VOLTAGE (V)

Figure 6. Drain-to-Source Leakage Current
vs. Voltage

1.E-07

TYPICAL CHARACTERISTICS

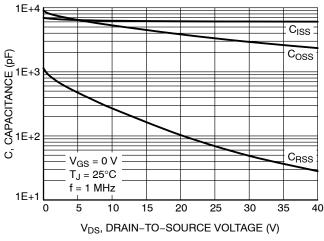


Figure 7. Capacitance Variation

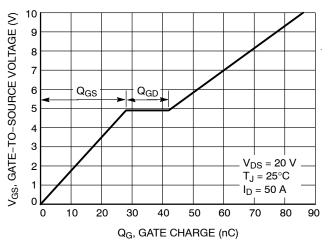


Figure 8. Gate-to-Source Voltage vs. Charge

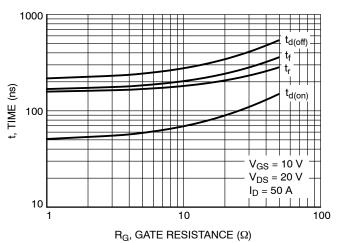


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

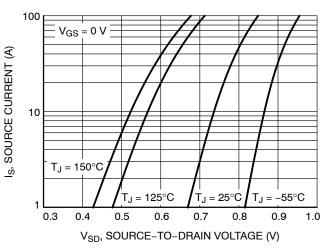


Figure 10. Diode Forward Voltage vs. Current

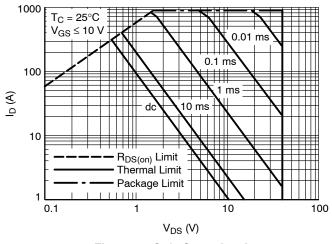


Figure 11. Safe Operating Area

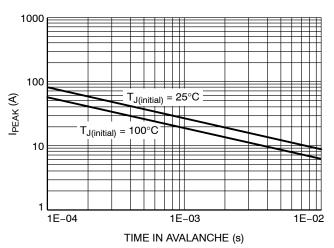


Figure 12. I_{PEAK} vs. Time in Avalanche

TYPICAL CHARACTERISTICS

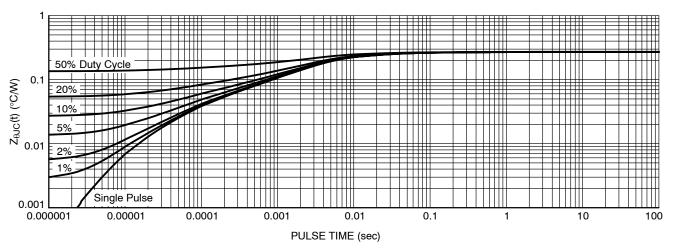


Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

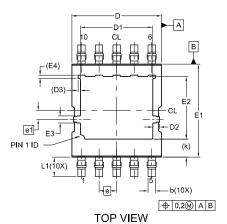
Device	Marking	Package	Shipping [†]
NVMJST0D9N04CTXG	0D94C	TCPAK10 (Pb-Free)	3000 / Tape & Reel

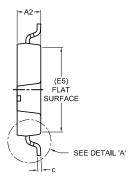
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

TCPAK10 5.1x7.5, 1.0P CASE 760AG

CASE 760AG ISSUE D

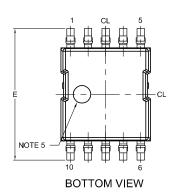


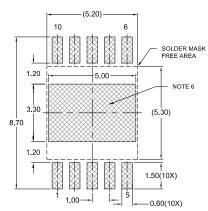


SIDE VIEW

NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- 2. UNIT DIMENSION: MILLIMETERS
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.150mm PER SIDE.
- 4. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- OPTIONAL MOLD FEATURE.
- LAND PAD UNDER THE PACKAGE BODY IS FOR MECHANICAL SUPPORT ONLY. SOLDER CONNECTION IS NOT REQUIRED.
- DIMENSION A1 IS THE LEAD STAND-OFF FROM THE BOTTOM SURFACE OF THE PACKAGE BODY.

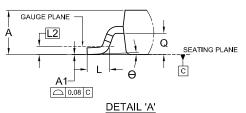




LAND PAD RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

MILLIMETERS					
DIM	MIN	NOM	MAX		
Α	1.30	1.35	1.45		
A1	-0.05	0.00	0.05		
A2	1.30	1.35	1.40		
b	0.36	0.41	0.46		
С	0.16	0.21	0.26		
D	5.00	5.10	5.20		
D1	4.02	4.12	4.22		
D2	0.30	0.40	0.50		
D3	0.14 REF				
E	7.40	7.50	7.60		
E1	5.20	5.30	5.40		
E2	3.47	3.57	3.67		
E3	0.30	0.40	0.50		
E4	0.17 REF				
E5	4.82 REF				
е	1.00 BSC				
e1	0.50 BSC				
k	1.03 REF				
L	0.49	0.69	0.89		
L1	0.90	1.10	1.30		
L2	0.25 BSC				
Q	0.60	0.65	0.70		
θ	0°	2.5°	5°		



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