Features

- Very low output resistance
- Extended supply voltage range: 12.5V to 24V
- TTL/CMOS compatible inputs
- CMOS Schmitt-triggered inputs
- Matched propagation delay for both channels
- Outputs in phase with inputs
- Enable function
- Under Voltage Lock Out function
- Automotive Qualified
- Leadfree, RoHS compliant

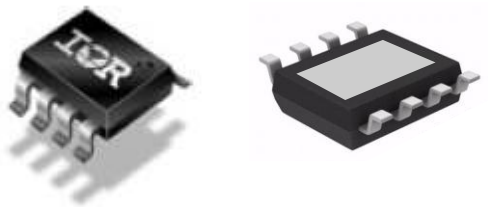
Typical Applications

- Automotive General Purpose Dual Low Side Driver
- Gate transformer driver
- Bridge Tied Gate Transformer Driver
- DC-DC converters secondary side driver
- Hybrid Power Train Driver

Product Summary

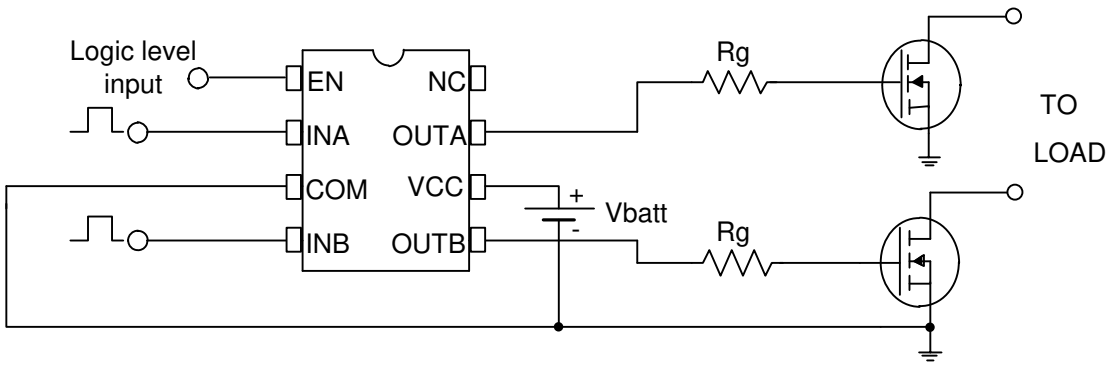
Topology	Dual Low Side Driver
V_{OUT}	12.5 V – 24 V
I_{o+} & I_{o-} (VCC=15V)	> 6 A
Output Resistance (max)	0.65 Ohm
t_{ON} & t_{OFF} (max)	55ns

Package



PSOIC-8N

Typical Connection Diagram



Orderable Part Number	Package Type	Standard Pack		Note
		Form	Quantity	
AUIRB24427STR	PSOIC8-N	Tape & Reel	2500	

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM lead. Stresses beyond those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the “Recommended Operating Conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (T_A) is 25°C, unless otherwise specified.

Symbol	Definition	Min.	Max.	Units
V_{cc}	Fixed supply voltage	-0.3	24	V
V_O	Output voltage	-0.3	24	
V_{IN}	Logic input voltage	-0.3	5.5	
V_{EN}	Logic enable voltage	-0.3	5.5	
Rth_{Jc}	Thermal resistance, junction to case	—	4	°C/W
T_J	Junction temperature	—	150	°C
T_S	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds)	—	300	

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions.
All voltage parameters are absolute voltage referenced to COM.

Symbol	Definition	Min.	Max.	Units
V_{cc}	Fixed supply voltage	5	20	V
V_O	Output voltage	0	V_{CC}	
V_{IN}	Logic input voltage	0	5	
V_{EN}	Logic enable voltage	0	5	
T_A	Ambient temperature	-40	125	°C
R_g	External gate resistance	2.5		Ω
C_{BP}	VCC to COM bypass capacitance – X7R dielectric type.	1		µF

Static Electrical Characteristics

Unless otherwise specified, these specifications apply for an operating junction temperature range of -40°C≤Ta≤125°C and power supply V_{CC}=15 V. The V_{IN} and I_{IN} parameters are referenced to COM and are applicable to input leads: INA and INB. The V_O and I_O parameters are referenced to COM and are applicable to the output leads: OUTA and OUTB.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
V_{IL}	Logic "0" input voltage			0.8	V	
V_{IH}	Logic "1" input voltage	2.5				
V_{HYS-IN}	Input voltage hysteresis	0.8				
V_{ENL}	Logic "0" enable voltage			0.8		
V_{ENH}	Logic "1" enable voltage	2.5				
V_{HYS-EN}	Enable voltage hysteresis	0.8				
ROH_{+25}	Source Output resistance			450	mΩ	Ta=+25C
ROL_{+25}	Sink Output resistance			450		
ROH_{+125}	Source Output resistance			650		Ta=+125C
ROL_{+125}	Sink Output resistance			650		
VOH_{+25}	Output high level voltage Vcc-Vo			450	mV	Ta=+25C, Iout=100mA
VOL_{+25}	Output low level voltage Vo			450		
VOH_{+125}	Output high level voltage Vcc-Vo			650		Ta=+125C, Iout=100mA
VOL_{+125}	Output low level voltage Vo			650		
I_{IN+}	Logic "1" input bias current		25	50	µA	VIN=5V, VCC=15V
I_{IN-}	Logic "0" input bias current			1		VIN=0V, VCC=15V
I_{QB}	Quiescent supply current	0.5	1.2	2.5	mA	VCC=15V, INA & INB not switching
$V_{CCUVHYS}$	Vcc supply undervoltage hysteresis		1.5		V	
V_{CCUV+}	Vcc supply undervoltage turn on threshold	10.5	11.5	12.6		
V_{CCUV-}	Vcc supply undervoltage turn off threshold	9.0	10.0	11		
I_{O+}	Output high short circuit pulsed current(†)	6			A	VCC=15V, PW<10us
I_{O-}	Output high short circuit pulsed current(†)	6				VCC=15V, PW<10us

(†) Guaranteed by design

Dynamic Electrical Characteristics

Unless otherwise noted, these specifications apply for an operating junction temperature range of -40°C≤Ta≤125°C with bias conditions of V_{CC} = 15 V, CL = 4700pF. Refer to Figure T2 for switching time definition and to Figure T3 for switching time test circuit (page 15).

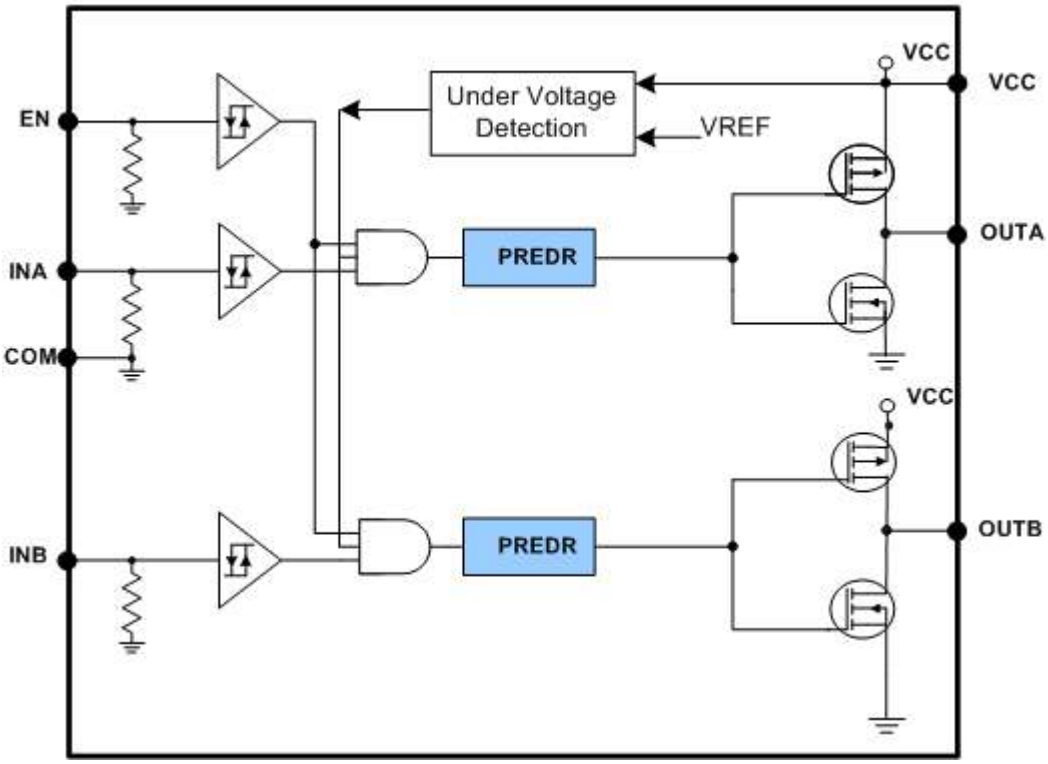
Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Propagation delay characteristics					ns	C_{BP}=10uF
T_{ON}	Turn-on propagation delay	—		40		
T_{OFF}	Turn-off propagation delay	—		55		
T_{ON-EN}	Enable Turn-on propagation delay	—		40		
T_{OFF-EN}	Enable Turn-off propagation delay	—		55		
t_r	Turn-on rise time	—		33		
t_f	Turn-off fall time	—		33		

Input/Output table

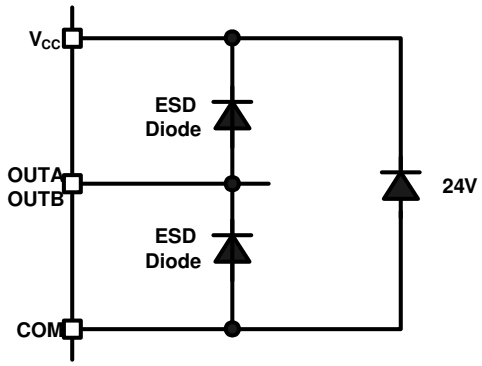
EN	INA	INB	OUTA	OUTB
L	X		L	L
L	X		L	L
H	L	L	L	L
H	H	H	H	H

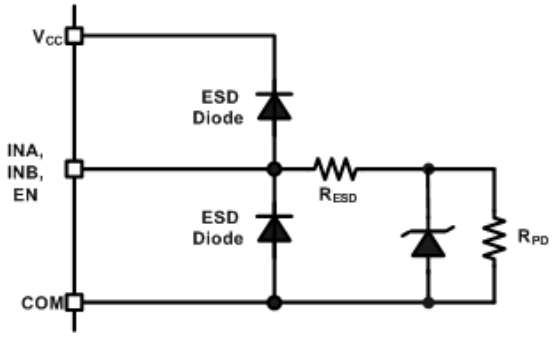
This table is held true in the voltages ranges defined in the recommended conditions section.
See also Fig. T1 on page 14.

Functional Block Diagram:



Input/Output/Enable Pin Equivalent Circuit Diagrams

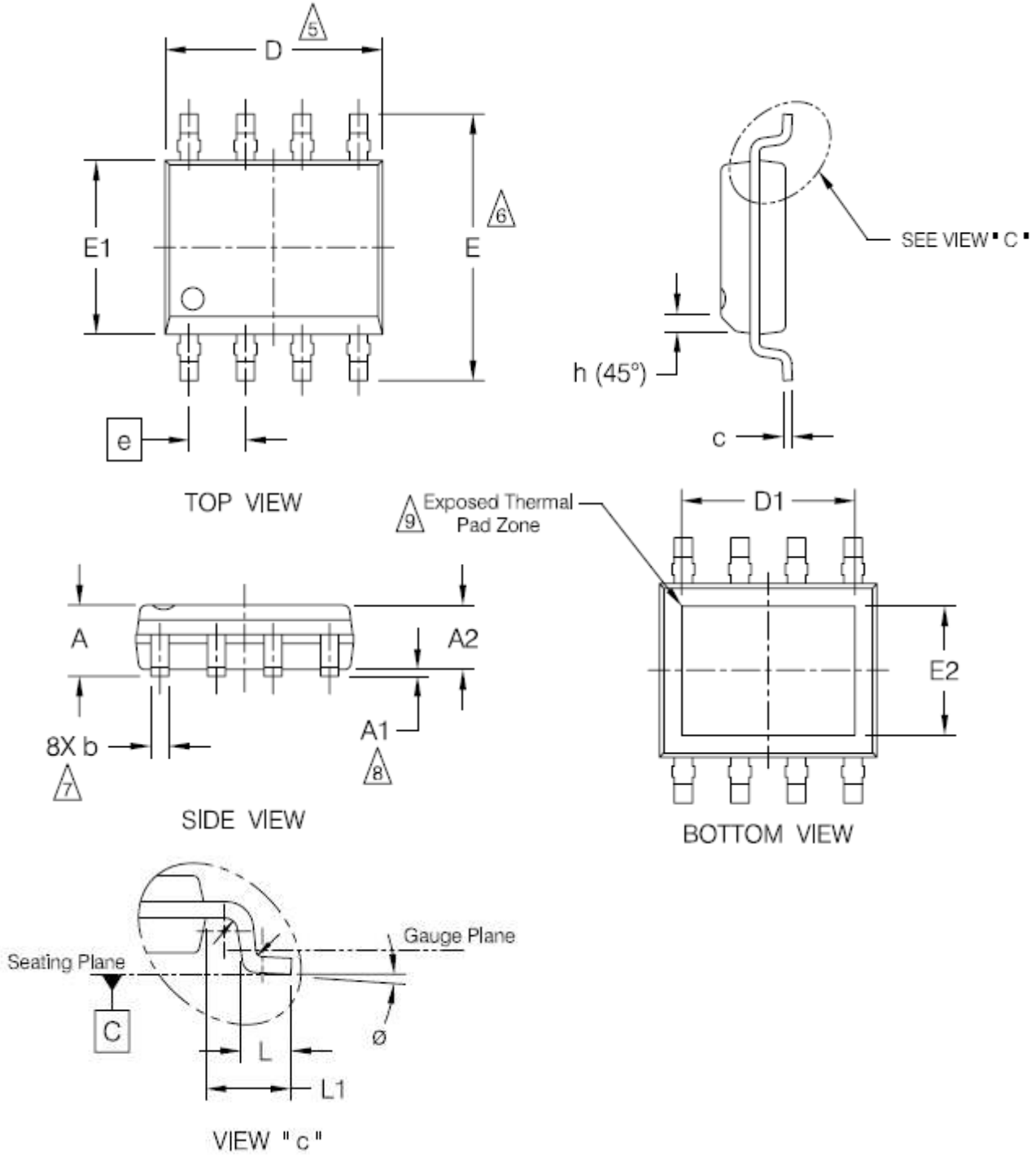




Lead Definitions

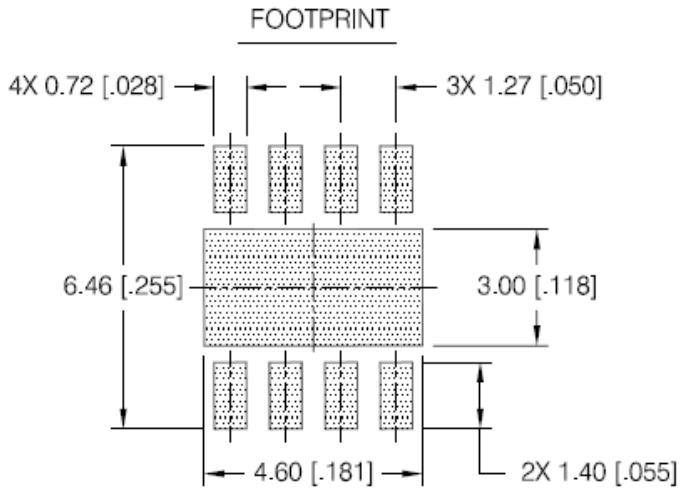
PIN	Symbol	Description
1	EN	Enable pin
2	INA	Logic input for gate driver output (OUTA), in phase
3	COM	Ground
4	INB	Logic input for gate driver output (OUTB), in phase
5	OUTB	Gate drive output B
6	VCC	Supply voltage
7	OUTA	Gate drive output A
8	NC	No connection

Package Information



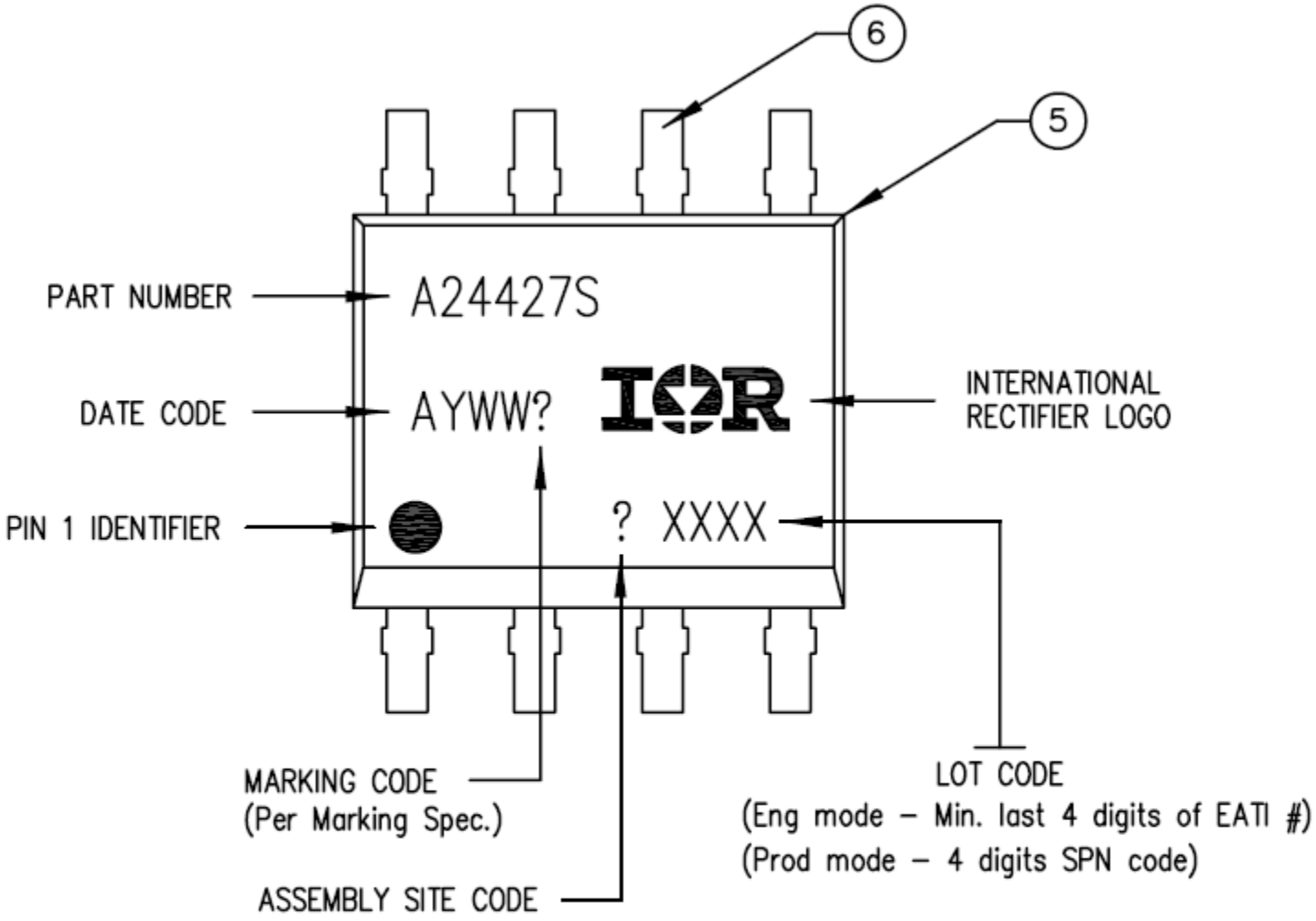
Symbols	Dimensions			
	Millimiter		Inches	
	MIN	MAX	MIN	MAX
A	---	1.70	---	.067
A1	0	0.10	0	.004
A2	1.25	---	.049	---
b	0.31	0.51	.012	.020
c	0.17	0.25	.007	.010
D	4.90		.193	
D1	3.20	3.40	.126	.134
E	6.00 BSC		.236 BSC	
E1	3.90 BSC		.153 BSC	
E2	1.00	---	.039	---
e	1.27 BSC		.050 BSC	
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
L1	1.04 REF		.041 REF	
L2	0.25 BSC		.010 BSC	
Θ	0	8	0	8

Recommended PCB footprint



NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012BA.
5. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS AND SHALL NOT EXCEED 0.15MM [.006] PER END.
6. DIMENSION "E" DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15MM [.006] PER END.
7. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSIONS SHALL BE 0.10 [.0039] TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION.
8. "A1" IS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
9. "D1" and "E2" MINIMUM DIMENSIONS ARE VARIABLE DEPENDING ON DIE PADDLE SIZE. END USER SHOULD VERIFY ACTUAL SIZE OF EXPOSED THERMAL PAD FOR SPECIFIC DEVICE APPLICATION.

Part Marking Information



TOP MARKING (LASER)

Application Information

1. Gate Driver

The AUIRB24427S has been designer as a high current gate driver for single ended applications. Thanks to its very high output current and low thermal resistance vs. pcb, it is capable to drive Mosfets with very large input capacitance at frequencies up to fsw=200kHz or higher without the need of negative supply. The following figure 1 shows the typical device application schematic:

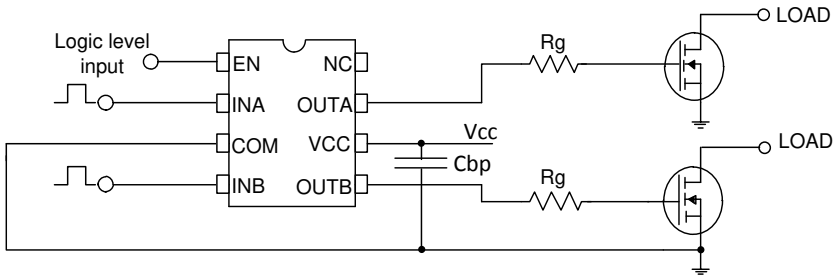


Figure 1: typical gate driver application

Rg values have to be selected based on the requested tr and tf of the application and may vary between 2.5Ω and 20Ω, while the input capacitance of the Fets can go up to 20nF or more depending on fsw. Since the very high peak output current, the bypass capacitor Cpb has to be mounted in the close proximity of the Vcc and COM pins and a ceramic type with low ESR has to be chosen.

2. BT-GTD (Bridge Tied Gate Transformer Driver)

This is a popular configuration that allows driving high side Fets using a low side gate driver, the Fig. 2 shows the typical schematic for a single Fet drive:

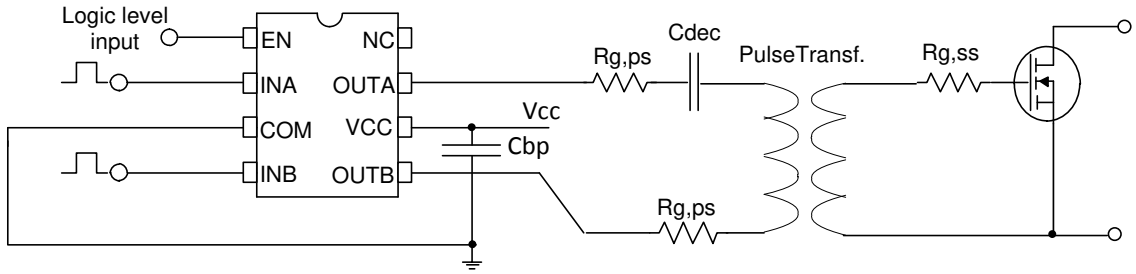


Figure 2: Bridge Tied Gate Driver configuration

In this configuration the gate transformer parameters have a very important role, most manufacturers indicate the following in their datasheets:

- V*µs ratings: this factor must be respected, in bipolar drive application (like the one shown in Fig.2) a maximum of up to twice that parameter is still acceptable for most manufacturers, this factor then must be chosen accordingly to the following formula:

$$V * \mu s\ rating\ (*2) \geq \frac{Vprim * \delta}{fsw} \quad (1)$$

where Vprim is the voltage applied to the primary, δ is the duty cycle and fsw the switching frequency of the application;

- N, turns ratio: usually 1:1, in some cases 1:2 or 1:1:1 (dual driver) this determines the voltage ratio between primary and secondary;
- Lp, primary inductance: this value determines the magnetizing inductance as follows:

$$Lm = Lp * K \quad (2)$$

where K is the coupling factor between primary and secondary windings.

- L_{LK}, leakage inductance: this parameter, usually indicated at primary, is equal to:

$$L_{LK} = Lp * (1 - K) \quad (3)$$

The higher is Lm, the lower is the magnetizing current flowing into the transformer and consequent power losses into the driver. On the other hand the lower is L_{LK}, the lower and shorter will be the ringing of the secondary LC network created by $L_{LK,}$ and Ciss of the Fet, damped by Rg,ss and much lower overshot will appear on the Vgs across the Fet during transition. Then a too high Lm requires a very good mechanical construction of the gate transformer to achieve high K and consequent low L_{LK}.

In a gate driver application running in the range of 50kHz-200kHz and using the AUIRB24427S, a good choice is usually a Lm between 300uH and 2mH and a L_{LK} < 1uH. This translate for the formula (2) and (3) above in a coupling factor K between 0.9940 and 0.9995

For good operation and to reduce unneeded power losses into the AUIRB24427S driver, the magnetizing current has to be kept I_{LM} < 0.5A, from this then derives a minimum Lm to be calculated as follows:

$$Lm_{min} = \frac{Vg}{0.5} * \frac{\delta}{fsw} \quad (4)$$

Where Vg is the gate driving voltage of the Fet

Fig. 2.a show a good design waveform obtained with the following parameters:
Vg=+/-15V, Lm=400uH, L_{LK}=0.4uH, N=1, fsw=100kHz, $Ciss_{FET}$ =10nF, Rg,ps=3Ω, Rg,ss=4Ω, Cdec=1uF

Cdec is the AC coupling capacitor needed to reset the driver transformer flux, its value has to be calculated in a way that the voltage across it can be considered constant during normal operation. The higher the fsw the smaller will be Cdec. A ceramic capacitor is normally used.

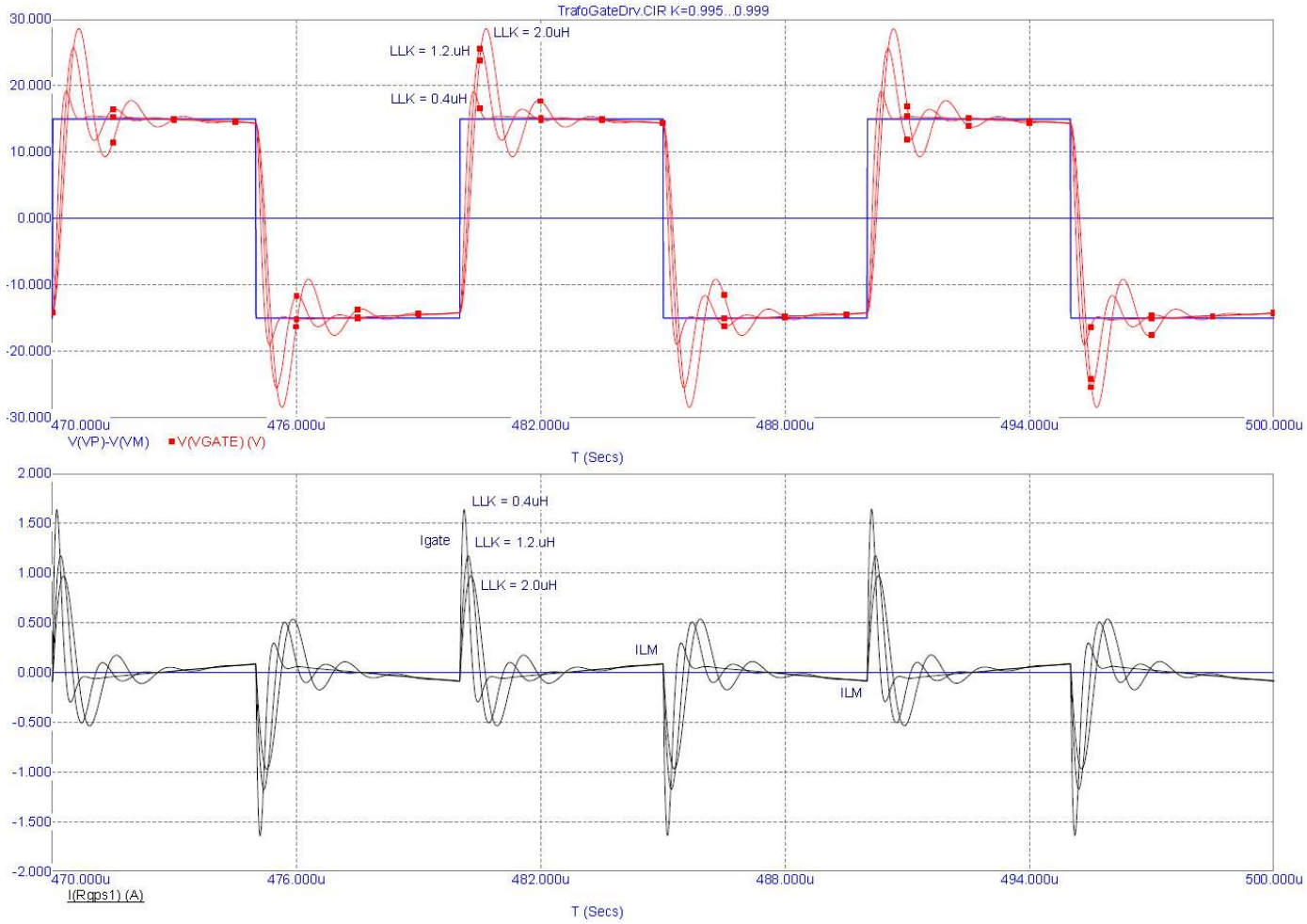


Figure 3a: Bridge Tied Gate Driver waveforms

The waveforms in Fig. 2a show that:

- The lower is $L_{LK,}$ the lower and shorter is the ringing on the Fets gate voltage, particular care must be paid to guarantee that the max Vgs voltage of the Fet is not exceeded during operation;
- The lower is L_{LK}, the shorter is the propagation delay from the driver to the gate of the Fet and the higher is the peak current into its gate;
- The higher is Lm, the lower is $I_{LM;}$ at the primary side the gate peak current, summed to I_{LM}, constitute the total current flowing out of the gate driver.

3. Driving circuitry design: thermal considerations

The following design example shows how to get a proper design of the gate driving circuitry considering the following target application data:

- Switching frequency 150kHz.
- Load capacitance range [10-100] nF.
- Supply voltage Vcc=12V.

The switching losses due to the charge/discharge of the capacitive load CL represent the main component of the IC power dissipation. These losses are proportionally shared between the IC output resistance and the external gate resistance Rg.

As a consequence the thermal behavior of the IC, with the constraint of a maximum junction temperature equal to 150°C, is one of the key points in dimensioning the system parameters. Figure 3 shows the power that is dissipated inside the IC as a function of load capacitance CL. The external resistance Rg has been chosen in order to keep the product RL*Cg as constant and equal to 300ns (refer to Figure 4 for switching circuit schematic).

For a given parameter sizing the value of Pow allows to calculate the junction temperature Tj as:

$$T_J = T_A + Pow \times R_{th-JA} \quad (1)$$

Where T_A is the ambient temperature and Rth_{JA} is the junction to ambient thermal resistance.

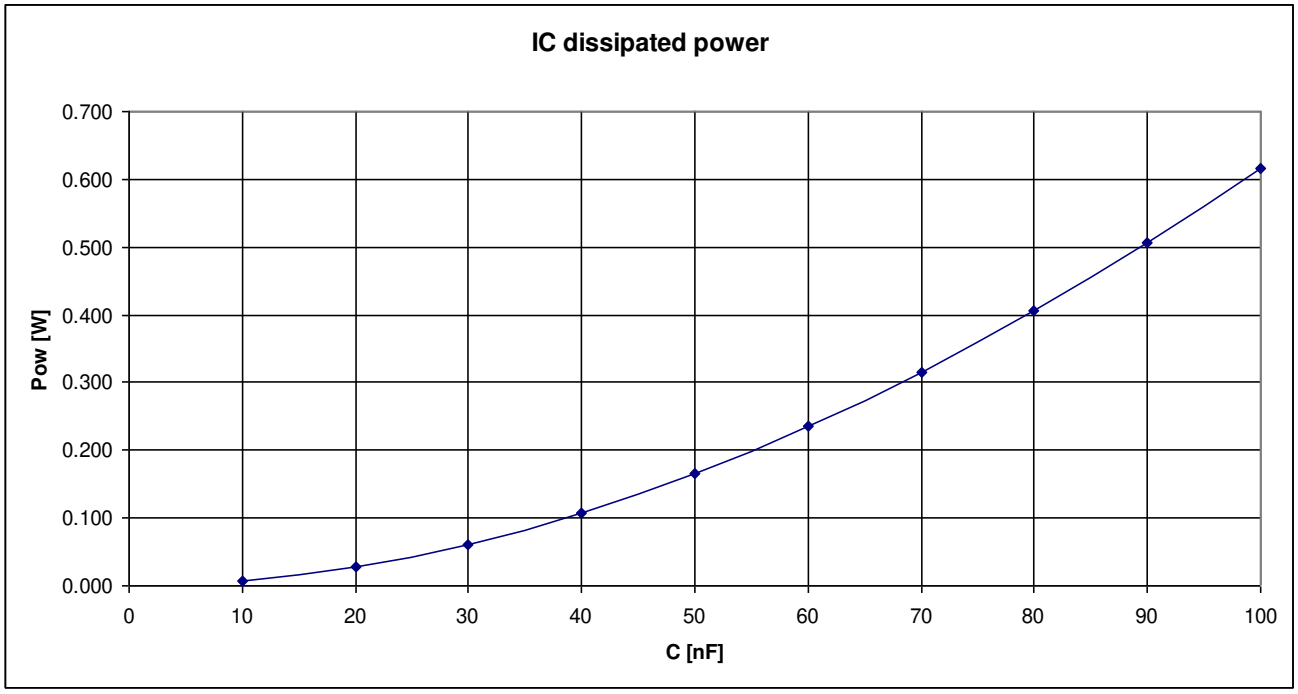


Figure 3: Simulated IC power dissipation as a function of load capacitance.

4. Bias and Transient Conditions

The input pins of the IC are protected by ESD events with the circuitry shown into "Functional block diagram" section at par.: Input/Output/Enable Pin Equivalent Circuit Diagrams. This shows that an ESD diode is placed in between each of these pins and Vcc.
In case Vcc voltage will be lower than one of the voltage applied to these pins the diode will conduct. Because of its power dissipation the junction temperature will increase. In order to avoid dangerous working conditions it is recommended to keep the Vcc voltage always higher or equal to the INA/INB/Enable pin voltages; it is remind that input voltage must respect the defined absolute maximum rating limits.

5. System functionality with improved thermal behavior.

The PSOIC8N package is characterized by a metal thermal pad whose functionality is to reduce the junction to case thermal resistance. In order to better exploit this feature it is necessary to reduce as much as possible the thermal pad to PCB thermal resistance (RthTP-PCB in. Fig. 4).
Two possible ways are suggested:
a- Foresee a footprint on layout that allows to solder the thermal pad to the PCB.
b- Use thermal material filling the air gap in between the thermal pad and the PCB.

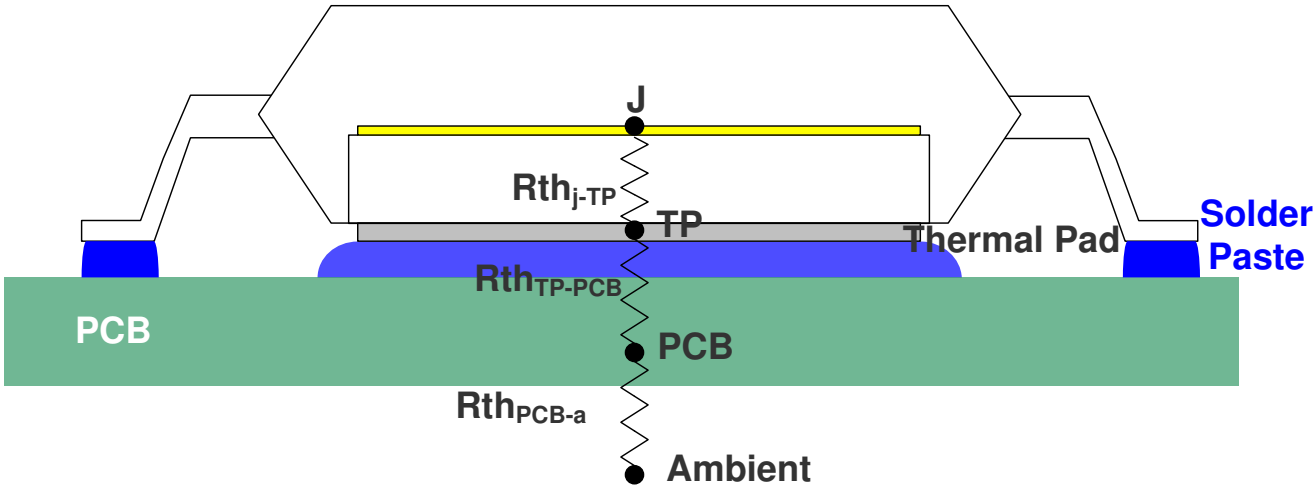


Figure 4: Steady state equivalent thermal circuit.

6. Square input pulse distortion

The following chapter provides a characterization of pulse width distortion. This is defined as the ratio between the output pulse width with respect to input pulse width. Characterization is done with no load on OUTA and OUTB and it is applicable to both INA, INB and EN input pulses.
Fig. 5a and 5b show the output pulse length with respect to input pulse length. In particular, Fig. 5a describes the pulse distortion in case of a short turn-on input pulse (e.g. low duty cycle condition); while Fig. 5b shows the pulse distortion in case of a turn-off input pulse (e.g. high duty cycle condition).

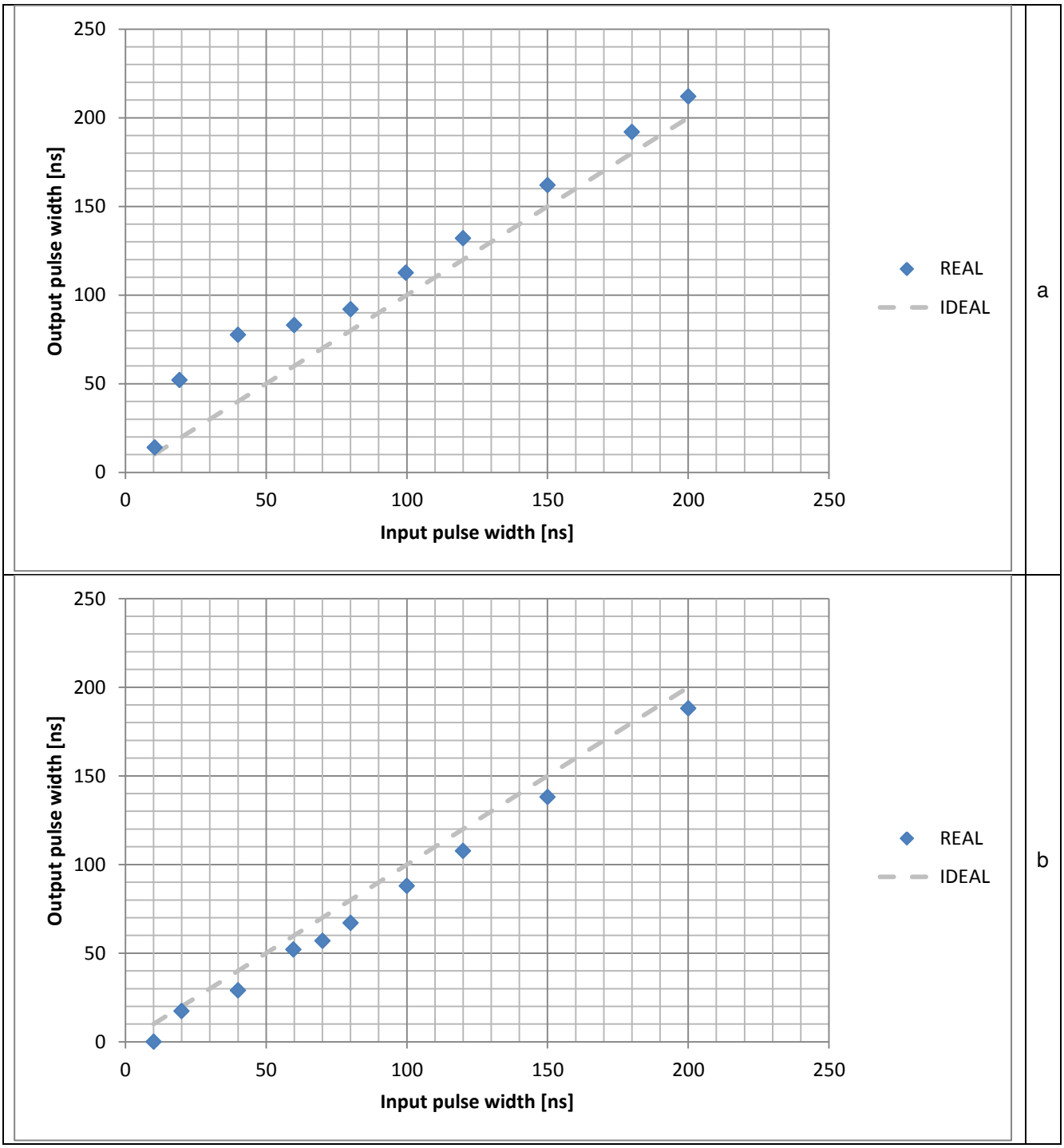


Fig. 5 Output pulse distortion in case of a short turn-on input pulse (a) and turn-off input pulse (b).

7. Bypass capacitor

The bypass capacitor stores an electrical charge that is released to the power line whenever a transient voltage spike occurs. It provides a low-impedance supply source and it minimizes the noise generated by the switching of the outputs.

It is recommended to place the bypass capacitor as close as possible to the gate driver in order to improve its effectiveness by reducing the effect of parasitic inductance of PCB lines.

The value of bypass capacitor is related to:

a- the current that the gate driver has to provide to the OUTA/B loads during turn-on switching condition;
b- the speed at which the output pin is driven;
c- the maximum allowed drop on power supply pins.

For instance, if it considered that outputs OUTA and OUTB provide 6A source current with 20ns rise time and the maximum wished drop on VCC pin is 0.1V, then the bypass capacitance can be calculated as:

$$C = n * I \frac{\Delta T}{\Delta V} = 2 * 6A \frac{20ns}{0.1V} = 2.4\mu F \quad (1)$$

Where n is the number of outputs that are switching at the same time. In this case it has been considered that OUTA and OUTB are driven in phase.

Equation 1 does not contain the information about capacitance ESR that introduces a further drop in the power supply voltage. As a consequence it is recommended to use low ESR capacitances (e.g. X7R dielectric material).

Additional Details

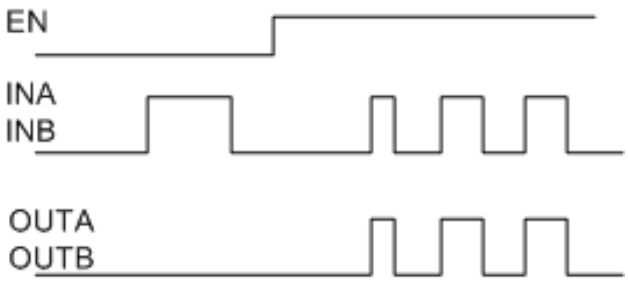


Figure T1: Input/output Timing Diagram

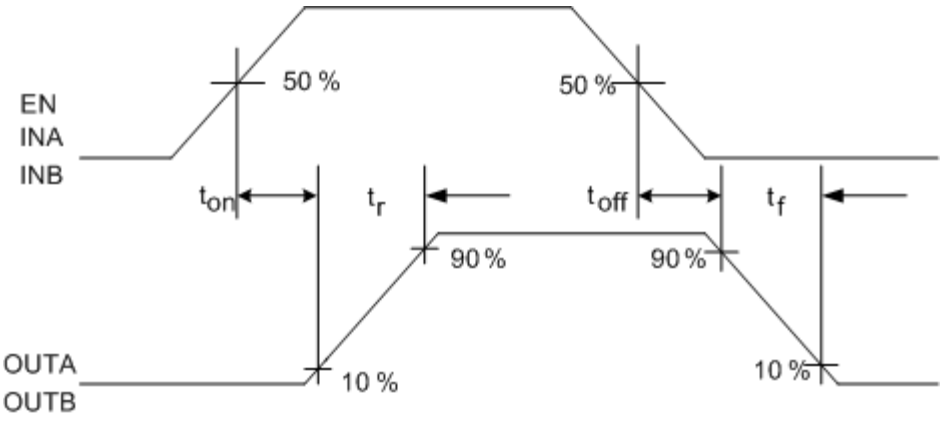
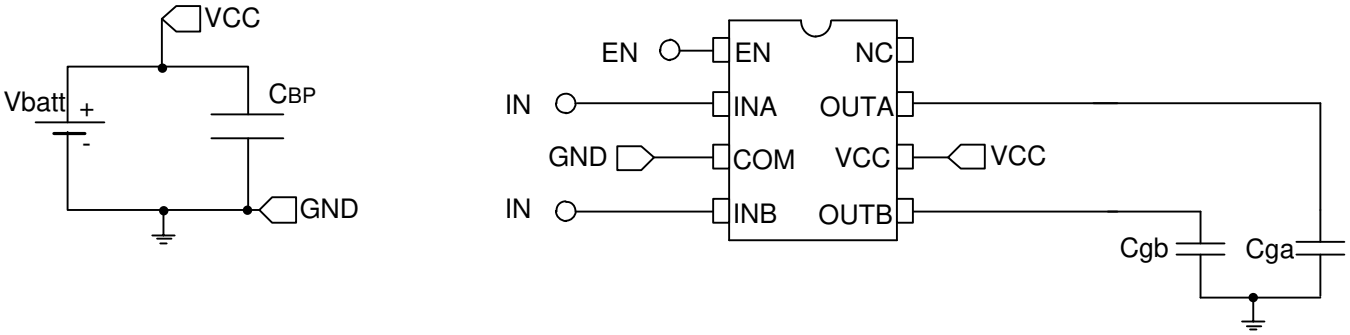


Figure T2: Switching Time Waveform Definitions



Parameter	Definitio	EN	IN
T_{ON}	Turn-on propagation delay	5V	Pulse 0V to 5V
T_{OFF}	Turn-off propagation delay	5V	Pulse 5V to 0V
T_{ON-EN}	Enable Turn-on propagation delay	Pulse 0V to 5V	5V
T_{OFF-EN}	Enable Turn-off propagation delay	Pulse 5V to 0V	5V

Figure T3: Switching Time Test Circuit and test conditions

Qualification Information

Qualification Level		Automotive (per AEC-Q100)	
		Comments: This family of ICs has passed an Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		PSOIC8-N	MSL3, 260°C (per IPC/JEDEC J-STD-020)
ESD	Machine Model	Class M2 (+/-150V) (per AEC-Q100-003)	
	Human Body Model	Class H2 (+/-2500 V) (per AEC-Q100-002)	
	Charged Device Model	Class C4 (+/-1000 V) (per AEC-Q100-011)	
IC Latch-Up Test		Class II, Level A (per AEC-Q100-004)	
RoHS Compliant		Yes	

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/

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Rev	Description
1v7 June, 26th 2013	Updated datasheet parameters according to standard lots test results. OUTx_x splitted overt UVLO+ increased the max to 12.6V Toff increased to 45ns from 40ns Toff-EN increased to 48ns from 40ns Introduced VOH/L parameters Changed Fig. T2. Added application sections: 1- pulse width distortion 2- Bypass capacitance
1v8 September, 23rd 2013	Updated pulse width distortion section based on new R0E silicon. Added min VCC in recommended table. Updated Toff delay page 4 Added CBP min in recommended table.
1v9 Nov. 15th	Updated comments on page 13 and 3 Updated Rdson Max on page 1
2v0 Dec 2013	Updated Vhys on page 3, removed tube packaging and updated typical applications on page 1, updated qualification information Updated date, added Important Notice page, DR3 version
2v1 Mar 18th 2014	Updated Ton & Toff value on page 1, updated Toff limits on page 4
2v2 Mar 24th 2014	Updated Tr & Tf value on page 4. Last DR3 version
2V3 May 23rd 2014	Updated application sections adding typical and BT-GTD circuits. Updated typical application list on page 1
Sept.29,2104	Part Marking drawing updated

