

BUK6246-75C

N-channel TrenchMOS intermediate level FET

Rev. 1 — 13 July 2011

Product data sheet

1. Product profile

1.1 General description

Intermediate level gate drive N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using advanced TrenchMOS technology. This product has been designed and qualified to the appropriate AEC Q101 standard for use in high performance automotive applications.

1.2 Features and benefits

- AEC Q101 compliant
- Suitable for standard and logic level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

1.3 Applications

- 12 V and 24 V Automotive systems
- Electric and electro-hydraulic power steering
- Motors, lamps and solenoid control
- Start-Stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{DS}	drain-source voltage	$T_j \ge 25 \text{ °C}; T_j \le 175 \text{ °C}$	-	-	75	V
I _D	drain current	$V_{GS} = 10 \text{ V}; T_{mb} = 25 \text{ °C};$ see <u>Figure 1</u>	-	-	22	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; see Figure 2	-	-	60	W
Static characteristics						
R _{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A};$ $T_j = 25 \text{ °C};$ see Figure 11	-	39	46	mΩ



Table 1. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Avalanche	ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I_D = 22 A; $V_{sup} \le 75$ V; R_{GS} = 50 Ω ; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped	-	-	25	mJ
Dynamic ch	Dynamic characteristics					
Q_{GD}	gate-drain charge	$I_D = 25 \text{ A}; V_{DS} = 60 \text{ V};$ $V_{GS} = 10 \text{ V};$ see <u>Figure 13</u> ; see <u>Figure 14</u>	-	6.84	-	nC

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		-
2	D	drain	mb	D
3	S	source		
mb			1 3	mbb076 S
			SOT428 (DPAK)	

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK6246-75C	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C		-	75	V
V_{GS}	gate-source voltage	DC	<u>[1]</u>	-16	16	V
		Pulsed	[2]	-20	20	V
I _D	drain current	T_{mb} = 25 °C; V_{GS} = 10 V; see <u>Figure 1</u>		-	22	Α
		T_{mb} = 100 °C; V_{GS} = 10 V; see <u>Figure 1</u>		-	16	Α
I _{DM}	peak drain current	T_{mb} = 25 °C; pulsed; $t_p \le 10 \mu s$; see <u>Figure 3</u>		-	89	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>		-	60	W
T _{stg}	storage temperature			-55	175	°C
T _j	junction temperature			-55	175	°C
Source-drain	diode					
Is	source current	T _{mb} = 25 °C		-	22	Α
I _{SM}	peak source current	pulsed; $t_p \le 10 \mu s$; $T_{mb} = 25 \text{ °C}$		-	89	Α
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I_D = 22 A; $V_{sup} \le 75$ V; R_{GS} = 50 Ω ; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped		-	25	mJ
E _{DS(AL)R}	repetitive drain-source avalanche energy		[3][4][5]	-	-	J

^{[1] -16}V accumulated duration not to exceed 168 hrs.

^[2] Accumulated pulse duration not to exceed 5 mins.

^[3] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.

^[4] Repetitive avalanche rating limited by an average junction temperature of 170 °C.

^[5] Refer to application note AN10273 for further information.

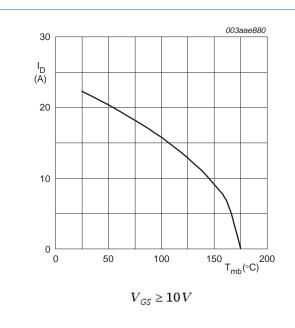


Fig 1. Continuous drain current as a function of mounting base temperature

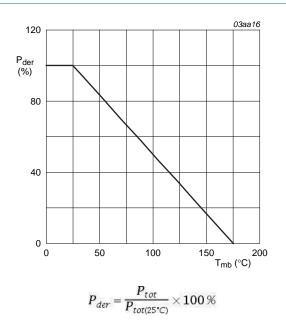
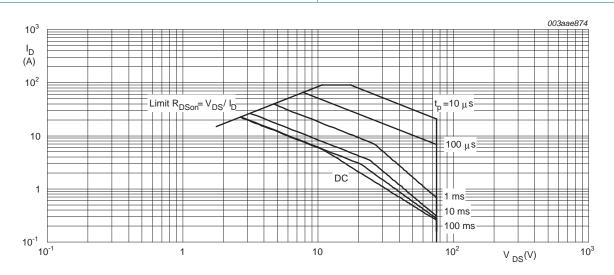


Fig 2. Normalized total power dissipation as a function of mounting base temperature



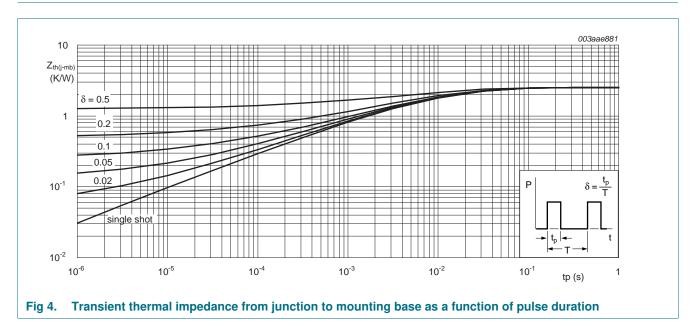
 $T_{mb} = 25$ °C; I_{DM} is a single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	2.52	K/W



6. Characteristics

Table 6. Characteristics

Table 6.	Characteristics					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static cha	aracteristics					
$V_{(BR)DSS}$	drain-source	$I_D = 250 \ \mu A; \ V_{GS} = 0 \ V; \ T_j = 25 \ ^{\circ}C$	75	-	-	V
	breakdown voltage	$I_D = 250 \ \mu A; \ V_{GS} = 0 \ V; \ T_j = -55 \ ^{\circ}C$	68	-	-	V
V _{GS(th)} gate-source threshold voltage	gate-source threshold voltage	$I_D = 1$ mA; $V_{DS} = V_{GS}$; $T_j = 25$ °C; see Figure 9; see Figure 10	1.8	2.3	2.8	V
		$I_D = 1$ mA; $V_{DS} = V_{GS}$; $T_j = -55$ °C; see Figure 9	-	-	3.3	V
		$I_D = 1$ mA; $V_{DS} = V_{GS}$; $T_j = 175$ °C; see Figure 9	0.8	-	-	V
I _{DSS}	drain leakage current	$V_{DS} = 75 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ °C}$	-	-	500	μΑ
		$V_{DS} = 75 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	0.02	1	μΑ
I _{GSS}	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	2	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	2	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ °C};$ see <u>Figure 11</u>	-	39	46	mΩ
		$V_{GS} = 4.5 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ °C};$ see Figure 11	-	47.2	64	mΩ
		$V_{GS} = 5 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ °C};$ see <u>Figure 11</u>	-	44.4	56	mΩ
		V_{GS} = 10 V; I_D = 10 A; T_j = 175 °C; see <u>Figure 11</u> ; see <u>Figure 12</u>	-	-	120	mΩ
Dynamic	characteristics					
$Q_{G(tot)}$ total gate charge		$I_D = 25 \text{ A}$; $V_{DS} = 60 \text{ V}$; $V_{GS} = 10 \text{ V}$; see Figure 13; see Figure 14	-	21.4	-	nC
		$I_D = 25 \text{ A}$; $V_{DS} = 60 \text{ V}$; $V_{GS} = 5 \text{ V}$; see Figure 13; see Figure 14	-	11.8	-	nC
Q_{GS}	gate-source charge	$I_D = 25 \text{ A}; V_{DS} = 60 \text{ V}; V_{GS} = 10 \text{ V};$	-	3.76	-	nC
Q_{GD}	gate-drain charge	see Figure 13; see Figure 14	-	6.84	-	nC
C _{iss}	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$	-	955	1280	pF
C _{oss}	output capacitance	T _j = 25 °C; see <u>Figure 15</u>	-	84	101	pF
C_{rss}	reverse transfer capacitance		-	63	86	pF
t _{d(on)}	turn-on delay time	V_{DS} = 55 V; R_L = 2.2 Ω ; V_{GS} = 10 V;	-	9.5	-	ns
t _r	rise time	$R_{G(ext)} = 10 \Omega$	-	17.8	-	ns
$t_{d(off)}$	turn-off delay time		-	37	-	ns
t _f	fall time		-	35	-	ns
L _D	internal drain inductance	from upper edge of drain mounting base to centre of die; $T_j = 25$ °C	-	3.5	-	nΗ
L _S	internal source inductance	from source lead to source bond pad; $T_j = 25 ^{\circ}\text{C}$	-	7.5	-	nΗ

Table 6. Characteristics ... continued

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Source-drai	n diode					
V _{SD}	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C};$ see <u>Figure 16</u>	-	0.9	1.2	V
t _{rr}	reverse recovery time	$I_S = 20 \text{ A}$; $dI_S/dt = -100 \text{ A/}\mu\text{s}$; $V_{GS} = 0 \text{ V}$;	-	42	-	ns
Q _r	recovered charge	$V_{DS} = 25 \text{ V}$	-	64	-	nC

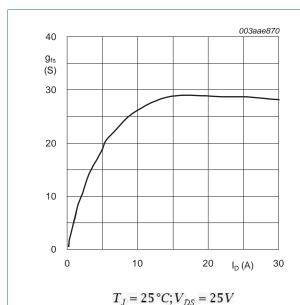


Fig 5. Forward transconductance as a function of drain current; typical values

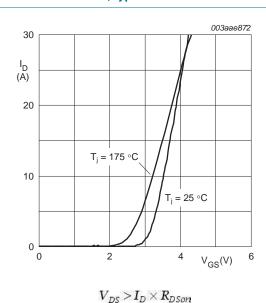
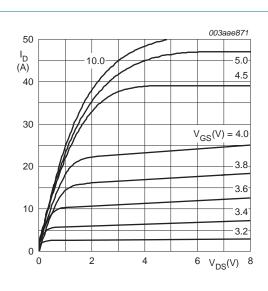
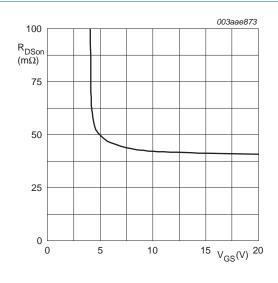


Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



 $T_j = 25 \,^{\circ}C$

Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values



 $T_j = 25 \,^{\circ}C; I_D = 10A$

Fig 8. Drain-source on-state resistance as a function of gate-source voltage; typical values

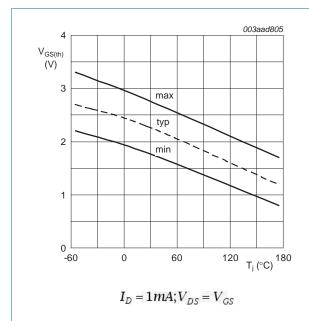


Fig 9. Gate-source threshold voltage as a function of junction temperature

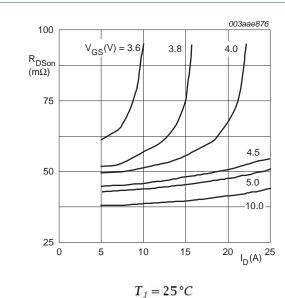


Fig 11. Drain-source on-state resistance as a function of drain current; typical values

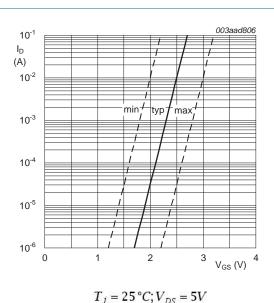


Fig 10. Sub-threshold drain current as a function of gate-source voltage

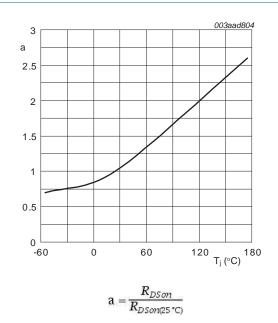


Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature

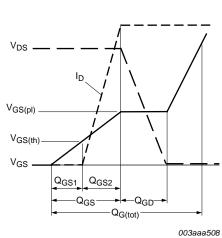


Fig 13. Gate charge waveform definitions



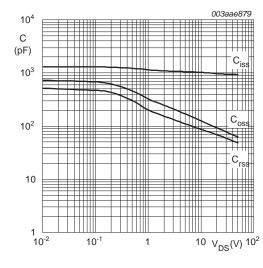
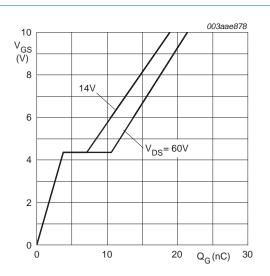


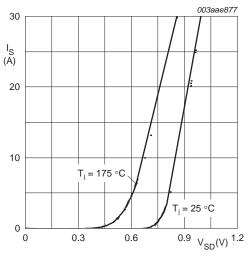
Fig 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

 $V_{GS} = 0V; f = 1MHz$



 $T_j = 25 \,^{\circ}C; I_D = 25A$

Fig 14. Gate-source voltage as a function of gate charge; typical values



 $V_{GS} = 0 V$

Fig 16. Source current as a function of source-drain voltage; typical values

7. Package outline

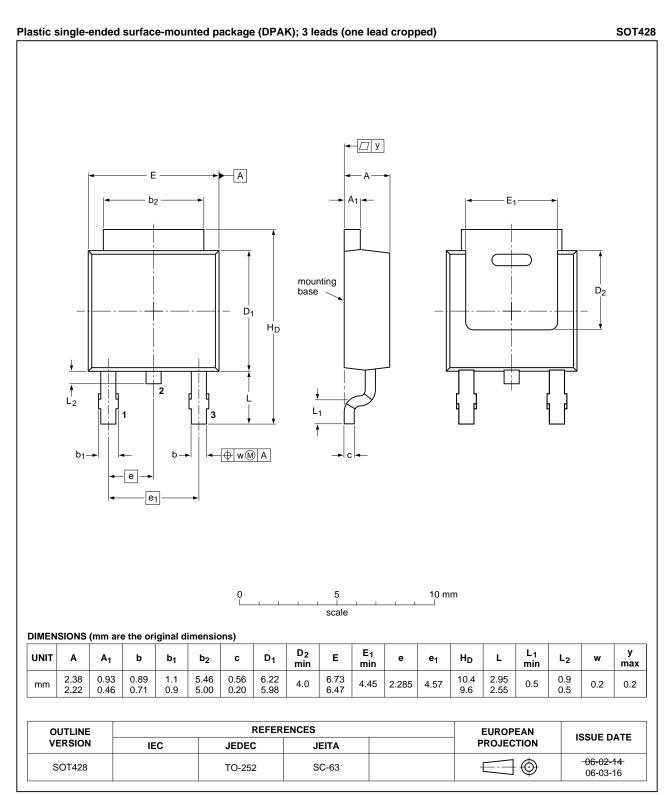


Fig 17. Package outline SOT428 (DPAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK6246-75C v.1	20110713	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status [1] [2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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Nexperia

N-channel TrenchMOS intermediate level FET

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