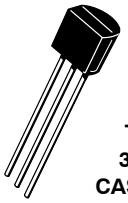
ASM1816

Low Power, 3.3 V/3.0 V, μP Reset, Active LOW, Open-Drain Output

ON Semiconductor®

http://onsemi.com

SOT−23
3 LEAD
CASE 527AG



TO−92
3 LEAD
CASE 29−11

Description

The ASM1816 is a voltage supervisory device with low−power, 3.3 V/3 V μP Reset, active LOW, open−drain output. Maximum supply current over temperature is a low 15 μA (at 3.6 V).

The ASM1816 generates an active LOW reset signal whenever the monitored supply is out of tolerance. A precision reference and comparator circuit monitor power supply (V_{CC}) level. Tolerance level options are 5%, 10%, 15% and 20%. When an out−of−tolerance condition is detected, an internal power−fail signal is generated which forces an active LOW reset signal. After V_{CC} returns to an in−tolerance condition, the reset signal remains active for 150 ms to allow the power supply and system microprocessor to stabilize.

The ASM1816 is designed with a open−drain output stage and operates over the extended industrial temperature range. Devices are available in TO−92 and compact surface mount SOT−23 packages.

Other low power products in this family include the ASM1810/11/12/15/17, ASM1233D and ASM1233M.

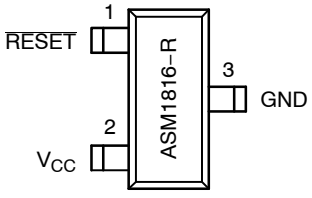
Features

- Low Supply Current
  - 20 μA Maximum (5.5 V)
  - 15 μA Maximum (3.6 V)
- Automatically Restarts a Microprocessor after Power Failure
- 150 ms Reset Delay after V_{CC} Returns to an In−tolerance Condition
- Active LOW Power−up Reset
- Precision Temperature−compensated Voltage Reference and Comparator
- Eliminates External Components
- TO−92 and Compact Surface Mount SOT−23 Package
- Operating Temperature −40°C to +85°C

Applications

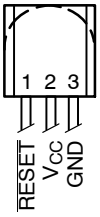
- Set−top Boxes
- Cellular Phones
- PDAs
- Energy Management Systems
- Embedded Control Systems
- Printers
- Single Board Computers

PIN CONFIGURATIONS



SOT−23
(Top View)

(Top View)



TO−92
ASM1816

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

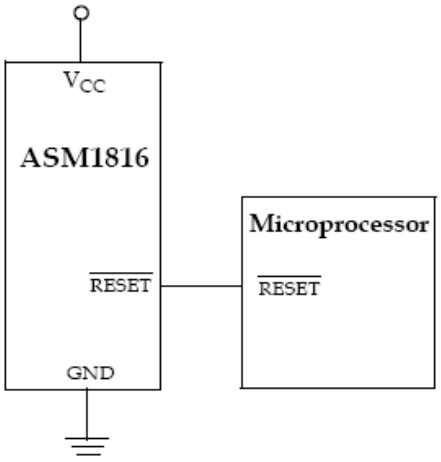


Figure 1. Typical Application

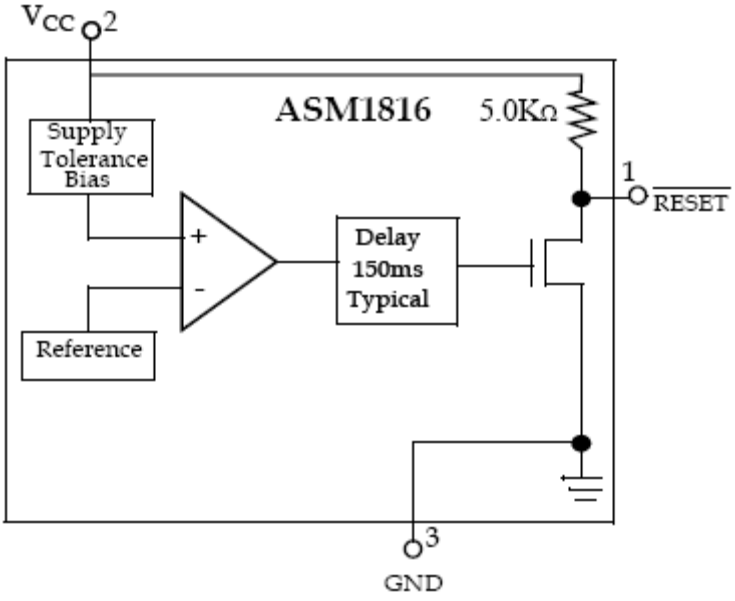


Figure 2. Block Diagram

Table 1. PIN DESCRIPTION

TO−92	SOT−23		
Pin #	**Pin #**	**Pin Name**	**Description**
1	1	$\overline{\text{RESET}}$	Active LOW reset output
2	2	V_{CC}	Power supply input
3	3	GND	Ground

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter		Min	Max	Unit
Voltage on V_{CC} (Note 1)		−0.5	7	V
Voltage on $\overline{RESET}$ (Note 1)		−0.5	V_{CC} + 0.5	V
Operating Temperature Range		−40	+85	°C
Soldering Temperature (for 10 sec)			+260	°C
Storage Temperature		−55	+125	°C
ESD rating	HBM		2	KV
	MM		200	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Voltages are measured with respect to ground.

Table 3. DC ELECTRICAL CHARACTERISTICS (Unless otherwise noted, V_{CC} = 1.2 V to 5.5 V and specifications are over the operating temperature range of −40°C to +85°C. All voltages are referenced to ground.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		1.2		5.5	V
Output Current	I_{OL}	Output = 0.4 V, V_{CC} > 2.7 V	10			mA
Operating Current	I_{CC}	V_{CC} < 5.5 V, $\overline{RESET}$ output open		8	20	μA
		$V_{CC} \leq$ 3.6 V, $\overline{RESET}$ output open		6	15	
V_{CC} Trip Point	V_{CCTP}	ASM1816R−5	2.98	3.06	3.15	V
		ASM1816R−10	2.80	2.88	2.97	
		ASM1816R−15	2.635	2.72	2.805	
		ASM1816R−20	2.47	2.55	2.64	
Internal Pull−up Resistor	R_P		3.5	5.5	7.5	KΩ
Output Capacitance	C_{OUT}				10	pF
V_{CC} Detect to $\overline{RESET}$ Low	t_{RPD}			2	5	μs
V_{CC} Slew Rate (V_{CCTP} (MAX) to V_{CCTP} (MIN)	t_F (Note 2)		300			μs
V_{CC} Slew Rate (V_{CCTP} (MIN) to V_{CCTP} (MAX)	t_R		0			ns
V_{CC} Detect to $\overline{RESET}$ High	t_{RPU}	t_r = 5 μs	100	150	250	ms

2. The t_F value is for reference in defining values for t_{RPD} and should not be considered for proper operation or use.

Application Information

Operation − Power Monitor

The ASM1816 detects out−of−tolerance power supply conditions. It resets a processor during power−up, power down and issues a reset to the system processor when the monitored power supply voltage is below the reset threshold. When an out−of−tolerance V_{CC} voltage is detected, the $\overline{RESET}$ signal is asserted. On power−up, $\overline{RESET}$ is kept active (LOW) for approximately 150 ms after the power supply voltage has reached the selected tolerance. This allows the power supply and microprocessor to stabilize before $\overline{RESET}$ is released.

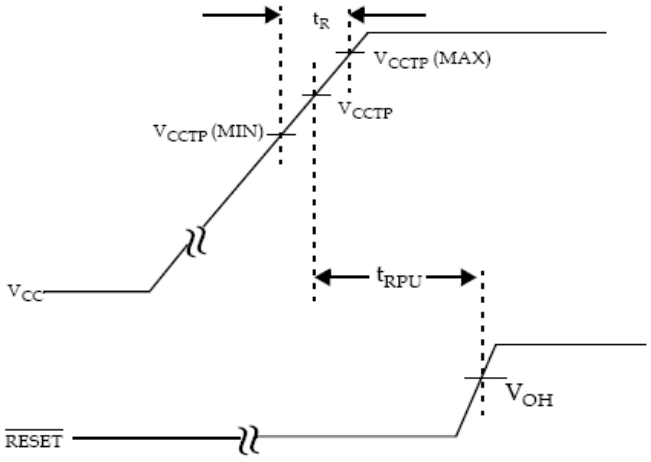


Figure 3. Timing Diagram: Power−Up

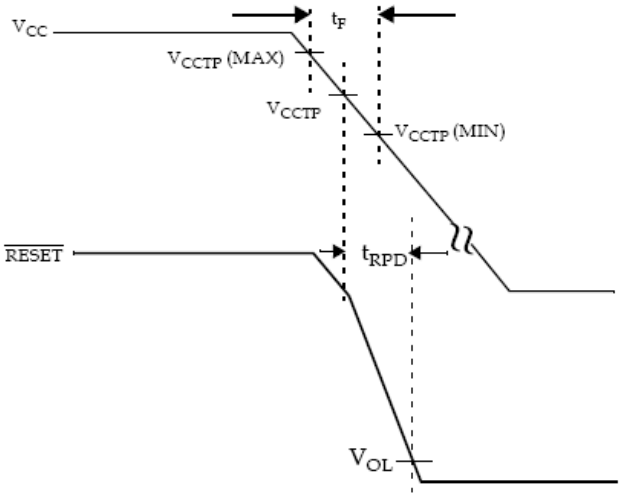


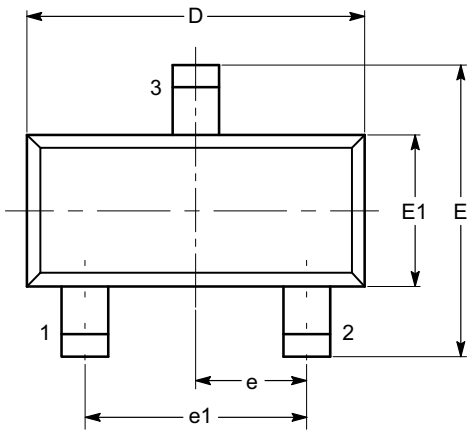
Figure 4. Timing Diagram: Power−Down

Table 4. FAMILY SELECTION GUIDE

Part #	RESET Voltage (V)	RESET Time (ms)	Output Stage	RESET Polarity
ASM1810	4.620, 4.370, 4.120	150	Push−Pull	LOW
ASM1811	4.620, 4.350, 4.130	150	Open−Drain	LOW
ASM1812	4.620, 4.350, 4.130	150	Push−Pull	HIGH
ASM1815	3.060, 2.880, 2.550	150	Push−Pull	LOW
ASM1816	3.060, 2.720, 2.880, 2.550	150	Open−Drain	LOW
ASM1817	3.060, 2.880, 2.550	150	Push−Pull	HIGH
ASM1233D	4.625, 4.375, 4.125	350	Open−Drain	LOW
ASM1233M	4.625, 4.375, 2.720	350	Open−Drain	LOW

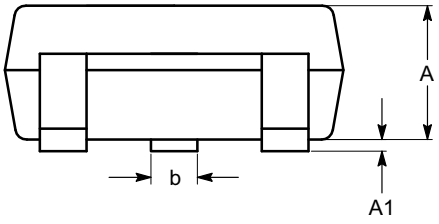
PACKAGE DIMENSIONS

SOT−23, 3 Lead
CASE 527AG−01
ISSUE O

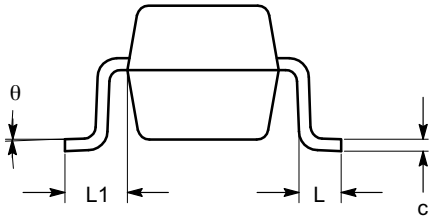


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	0.89		1.12
A1	0.013		0.10
b	0.37		0.50
c	0.085		0.18
D	2.80		3.04
E	2.10		2.64
E1	1.20		1.40
e	0.95 BSC		
e1	1.90 BSC		
L	0.40 REF		
L1	0.54 REF		
θ	0°		8°



SIDE VIEW

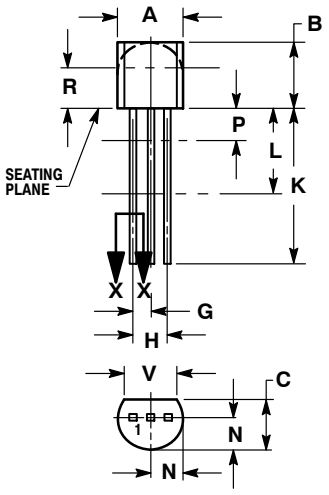


END VIEW

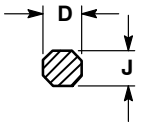
Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC TO-236.

PACKAGE DIMENSIONS

TO−92 (TO−226)
CASE 29−11
ISSUE AM



STRAIGHT LEAD
BULK PACK



SECTION X−X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.021	0.407	0.533
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.115	---	2.93	---
V	0.135	---	3.43	---

Table 5.

Part Number (Note 3)	RESET Output Voltage	RESET Tolerance	RESET Time	Open Drain Output (Note 4)	RESET Polarity	Package	Package Marking (Note 5)
TIN − LEAD DEVICES							
ASM1233D−L−5 (ASM1233A−5)	3.06	5%	350 ms	♦	LOW	3L TO−92	ASM1233D−L−5
ASM1233D−L−10 (ASM1233A−10)	2.88	10%	350 ms	♦	LOW	3L TO−92	ASM1233D−L−10
ASM1233D−L−15 (ASM1233A−15)	2.72	15%	350 ms	♦	LOW	3L TO−92	ASM1233D−L−15
ASM1233D−LZ−5 (ASM1233AZ−5)	3.06	5%	350 ms	♦	LOW	4L SOT−223	RVLL
ASM1233D−LZ−10 (ASM1233AZ−10)	2.88	10%	350 ms	♦	LOW	4L SOT−223	RWLL
ASM1233D−LZ−15 (ASM1233AZ−15)	2.72	15%	350 ms	♦	LOW	4L SOT−223	RXLL
ASM1233D−5	4.625	5%	350 ms	♦	LOW	3L TO−92	ASM1233D−5
ASM1233D−10	4.375	10%	350 ms	♦	LOW	3L TO−92	ASM1233D−10
ASM1233D−15	4.125	15%	350 ms	♦	LOW	3L TO−92	ASM1233D−15
ASM1233DZ−5	4.625	5%	350 ms	♦	LOW	4L SOT−223	RSLL
ASM1233DZ−10	4.375	10%	350 ms	♦	LOW	4L SOT−223	RTLL
ASM1233DZ−15	4.125	15%	350 ms	♦	LOW	4L SOT−223	RULL
ASM1233M−55	4.625	5%	350 ms	♦	LOW	3L TO−92	ASM1233M−55
ASM1233M−5	4.375	10%	350 ms	♦	LOW	3L TO−92	ASM1233M−5
ASM1233M−3	2.72	15%	350 ms	♦	LOW	3L TO−92	ASM1233M−3
ASM1233MS−55	4.625	5%	350 ms	♦	LOW	8L SOIC	ASM1233MS−55
ASM1233MS−5	4.38	10%	350 ms	♦	LOW	8L SOIC	ASM1233MS−5
ASM1233MS−3	2.72	15%	350 ms	♦	LOW	8L SOIC	ASM1233MS−3
LEAD FREE DEVICES							
ASM1233D−L−5F	3.06	5%	350 ms	♦	LOW	3L TO−92	ASM1233D−L−5F
ASM1233D−L−10F	2.88	10%	350 ms	♦	LOW	3L TO−92	ASM1233D−L−10F
ASM1233D−L−15F	2.72	15%	350 ms	♦	LOW	3L TO−92	ASM1233D−L−15F
ASM1233D−LZ−5F	3.06	5%	350 ms	♦	LOW	4L SOT−223	KVLL
ASM1233D−LZ−10F	2.88	10%	350 ms	♦	LOW	4L SOT−223	KWLL
ASM1233D−LZ−15F	2.72	15%	350 ms	♦	LOW	4L SOT−223	KXLL
ASM1233D−5F	4.625	5%	350 ms	♦	LOW	3L TO−92	ASM1233D−5F
ASM1233D−10F	4.375	10%	350 ms	♦	LOW	3L TO−92	ASM1233D−10F
ASM1233D−15F	4.125	15%	350 ms	♦	LOW	3L TO−92	ASM1233D−15F
ASM1233DZ−5F	4.625	5%	350 ms	♦	LOW	4L SOT−223	KSLL
ASM1233DZ−10F	4.375	10%	350 ms	♦	LOW	4L SOT−223	KTLL
ASM1233DZ−15F	4.125	15%	350 ms	♦	LOW	4L SOT−223	KULL
ASM1233M−5F	4.375	5%	350 ms	♦	LOW	3L TO−92	ASM1233M−5F
ASM1233M−55F	4.625	10%	350 ms	♦	LOW	3L TO−92	ASM1233M−55F
ASM1233M−3F	2.72	15%	350 ms	♦	LOW	3L TO−92	ASM1233M−3F
ASM1233MS−5F	4.38	5%	350 ms	♦	LOW	8L SOIC	ASM1233MS−5F
ASM1233MS−55F	4.625	10%	350 ms	♦	LOW	8L SOIC	ASM1233MS−55F
ASM1233MS−3F	2.72	15%	350 ms	♦	LOW	8L SOIC	ASM1233MS−3F

3. Add /T to Part Number for Tape and Reel (i.e., ASM18xx−x/T)
4. Internal 5.5 kΩ resistor pull−up
5. LL = Lot Code

Table 6. ORDERING INFORMATION

Device Summary							
Part Number (Note 6)	**RESET Output Voltage (V)**	**RESET Tolerance (%)**	**RESET Time (ms)**	**Open−Drain Output Stage** (Note 7)	**SOT−23 Package**	**RESET Polarity**	**Package Marking** (Note 8)
TIN − LEAD DEVICES							
ASM1816R−5	3.06	5	150	♦	♦	LOW	RMLL
ASM1816R−10	2.88	10	150	♦	♦	LOW	RNLL
ASM1816R−15	2.72	15	150	♦	♦	LOW	RZLL
ASM1816R−20	2.55	20	150	♦	♦	LOW	ROLL
LEAD FREE DEVICES							
ASM1816R−5F	3.06	5	150	♦	♦	LOW	KMLL
ASM1816R−10F	2.88	10	150	♦	♦	LOW	KNLL
ASM1816R−15F	2.72	15	150	♦	♦	LOW	KZLL
ASM1816R−20F	2.55	20	150	♦	♦	LOW	KOLL
Part Number (Note 6)	**RESET Output Voltage (V)**	**RESET Tolerance (%)**	**RESET Time (ms)**	**Open−Drain Output Stage** (Note 7)	**TO−92 Package**	**RESET Polarity**	**Package Marking**
TIN − LEAD DEVICES							
ASM1816−5	3.06	5	150	♦	♦	LOW	ASM1816−5
ASM1816−10	2.88	10	150	♦	♦	LOW	ASM1816−10
ASM1816−20	2.55	20	150	♦	♦	LOW	ASM1816−20
LEAD FREE DEVICES							
ASM1816−5F	3.06	5	150	♦	♦	LOW	ASM1816−5F
ASM1816−10F	2.88	10	150	♦	♦	LOW	ASM1816−10F
ASM1816−20F	2.55	20	150	♦	♦	LOW	ASM1816−20F

6. Add /T to Part Number for Tape and Reel (i.e., ASM18xx−x/T)
7. Internal 5.5 kΩ resistor pull−up
8. LL = Lot Code

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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