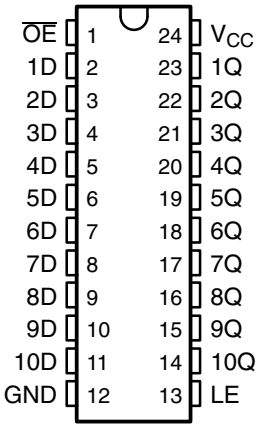
# CD74FCT841A
# BiCMOS 10-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

SCBS725 – JULY 2000

- **BiCMOS Technology With Low Quiescent Power**
- **Buffered Inputs**
- **Noninverted Outputs**
- **Input/Output Isolation From $V_{CC}$**
- **Controlled Output Edge Rates**
- **48-mA Output Sink Current**
- **Output Voltage Swing Limited to 3.7 V**
- **SCR Latch-Up-Resistant BiCMOS Process and Circuit Design**
- **Package Options Include Plastic Small-Outline (M) Package and Standard Plastic (EN) DIP**

**EN OR M PACKAGE**
**(TOP VIEW)**




## description

The CD74FCT841A is a 10-bit, D-type latch with 3-state outputs, designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. The device provides extra data width for wider address/data paths or buses carrying parity. The latches are transparent D-type latches. The device provides noninverted outputs.

The device uses a small-geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output high level to two diode drops below $V_{CC}$. This resultant lowering of output swing (0 V to 3.7 V) reduces power-bus ringing [a source of electromagnetic interference (EMI)] and minimizes $V_{CC}$ bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 48 mA.

The CD74FCT841A outputs are transparent to the inputs when the latch enable (LE) is high. When LE goes low, the data is latched. The output-enable ($\overline{OE}$) input controls the 3-state outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state. The latch operation is independent of the state of $\overline{OE}$.

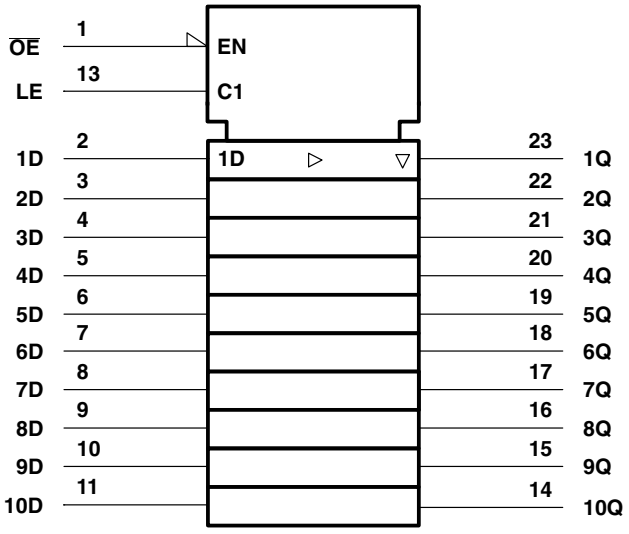
$\overline{OE}$ does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

The CD74FCT841A is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**
**(each latch)**

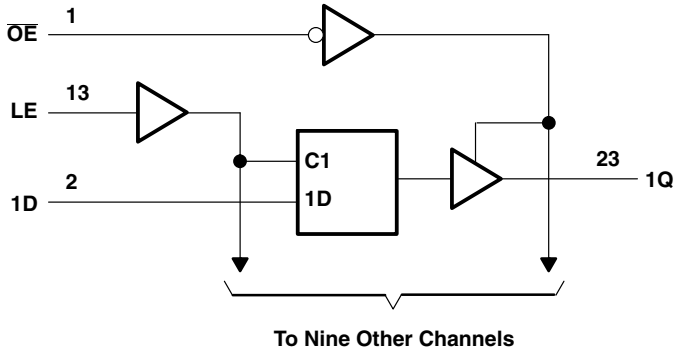
| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE}$ | LE | D | Q |
| L | H | H | H |
| L | H | L | L |
| L | L | X | $Q_0$ |
| H | X | X | Z |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

DC supply voltage range, $V_{CC}$ . . . . . –0.5 V to 6 V
DC input clamp current, $I_{IK}$ ($V_I$ < –0.5 V) . . . . . –20 mA
DC output clamp current, $I_{OK}$ ($V_O$ < –0.5 V) . . . . . –50 mA
DC output sink current per output pin, $I_{OL}$ . . . . . 70 mA
DC output source current per output pin, $I_{OH}$ . . . . . –30 mA
Continuous current through $V_{CC}$, ($I_{CC}$) . . . . . 260 mA
Continuous current through GND . . . . . 500 mA
Package thermal impedance, $\theta_{JA}$ (see Note 1): EN package . . . . . 67°C/W
M package . . . . . 46°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51.

## recommended operating conditions (see Note 2)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.75 | 5.25 | V |
| $V_{IH}$ | High-level input voltage | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | V |
| $V_I$ | Input voltage | 0 | $V_{CC}$ | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –15 | mA |
| $I_{OL}$ | Low-level output current | | 48 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | 0 | 10 | ns/V |
| $T_A$ | Operating free-air temperature | 0 | 70 | °C |

NOTE 2: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | $V_{CC}$ | $T_A$ = 25°C | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | | | |
| $V_{IK}$ | $I_I$ = –18 mA | | 4.75 V | | –1.2 | | –1.2 | V |
| $V_{OH}$ | $I_{OH}$ = –15 mA | | 4.75 V | 2.4 | | 2.4 | | V |
| $V_{OL}$ | $I_{OL}$ = 48 mA | | 4.75 V | | 0.55 | | 0.55 | V |
| $I_I$ | $V_I = V_{CC}$ or GND | | 5.25 V | | ±0.1 | | ±1 | μA |
| $I_{OZ}$ | $V_O = V_{CC}$ or GND | | 5.25 V | | ±0.5 | | ±10 | μA |
| $I_{OS}$† | $V_I = V_{CC}$ or GND, | $V_O$ = 0 | 5.25 V | –75 | | –75 | | mA |
| $I_{CC}$ | $V_I = V_{CC}$ or GND, | $I_O$ = 0 | 5.25 V | | 8 | | 80 | μA |
| $\Delta I_{CC}$‡ | One input at 3.4 V,<br>Other inputs at $V_{CC}$ or GND | | 5.25 V | | 1.6 | | 1.6 | mA |
| $C_i$ | $V_I = V_{CC}$ or GND | | | | 10 | | 10 | pF |
| $C_o$ | $V_O = V_{CC}$ or GND | | | | 15 | | 15 | pF |

† Not more than one output should be tested at a time, and the duration of the test should not exceed 100 ms.
‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

## timing requirements over recommended operating temperature conditions (unless otherwise noted) (see Figure 1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $t_w$ | Pulse duration | | 4 | | ns |
| $t_{su}$ | Setup time | Data before LE↓ | 2.5 | | ns |
| $t_h$ | Hold time | Data after LE↓ | 2.5 | | ns |

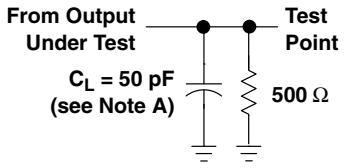
## switching characteristics over recommended operating temperature conditions (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $T_A$ = 25°C | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| | | | TYP | | | |
| $t_{pd}$ | D | Q | 6.8 | 1.5 | 9 | ns |
| | LE | | 9 | 2 | 12 | |
| $t_{en}$ | $\overline{OE}$ | Q | 8.6 | 1.5 | 11.5 | ns |
| $t_{dis}$ | $\overline{OE}$ | Q | 6 | 1.5 | 8 | ns |

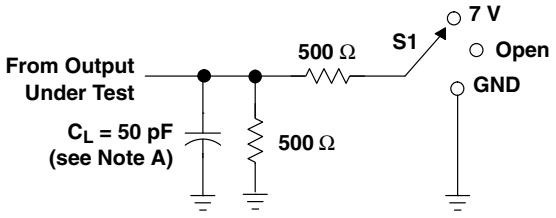
## noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 1 | | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | 0.5 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.8 | V |

## PARAMETER MEASUREMENT INFORMATION

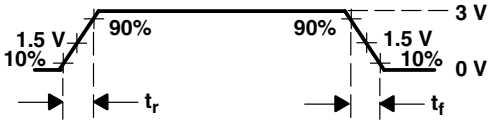



LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

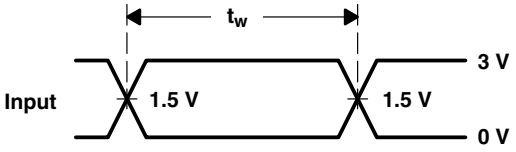



LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

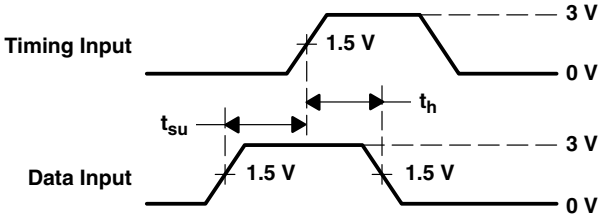
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V |
| $t_{PHZ}/t_{PZH}$ | Open |
| Open Drain | 7 V |



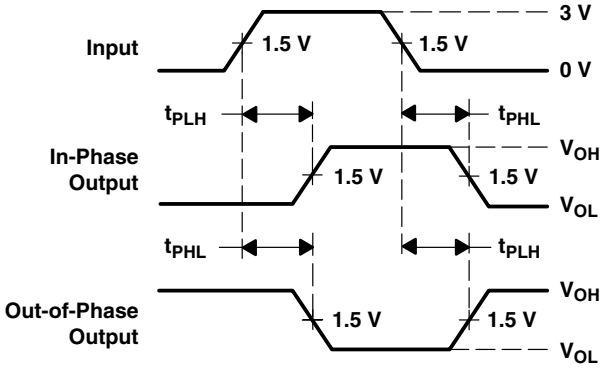

VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



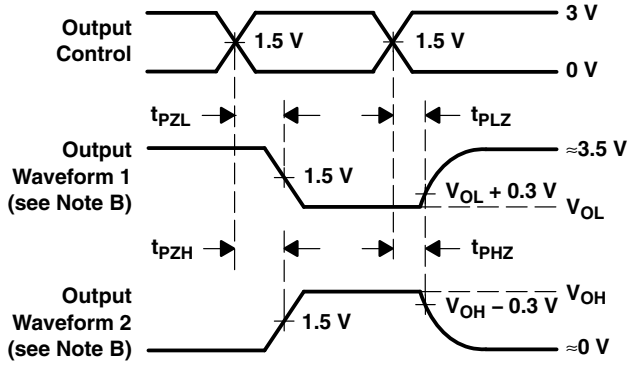

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ and $t_f$ = 2.5 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PHL}$ and $t_{PLH}$ are the same as $t_{pd}$.

**Figure 1. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CD74FCT841AEN | OBSOLETE | PDIP | NT | 24 | | TBD | Call TI | Call TI | 0 to 70 | | |
| CD74FCT841AM | OBSOLETE | SOIC | DW | 24 | | TBD | Call TI | Call TI | 0 to 70 | | |
| CD74FCT841AM96 | OBSOLETE | SOIC | DW | 24 | | TBD | Call TI | Call TI | 0 to 70 | | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

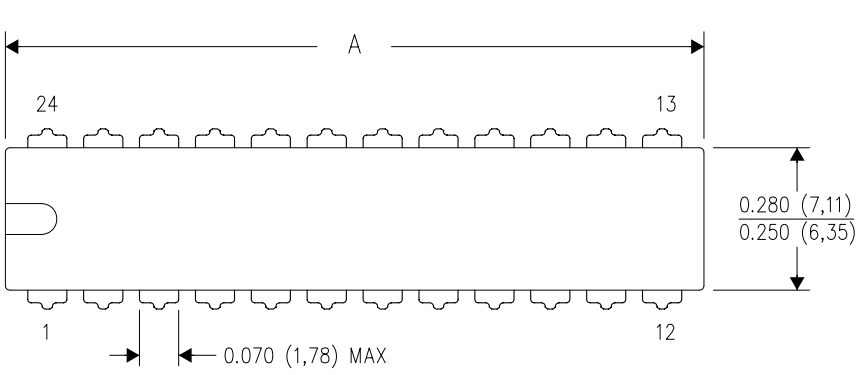
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

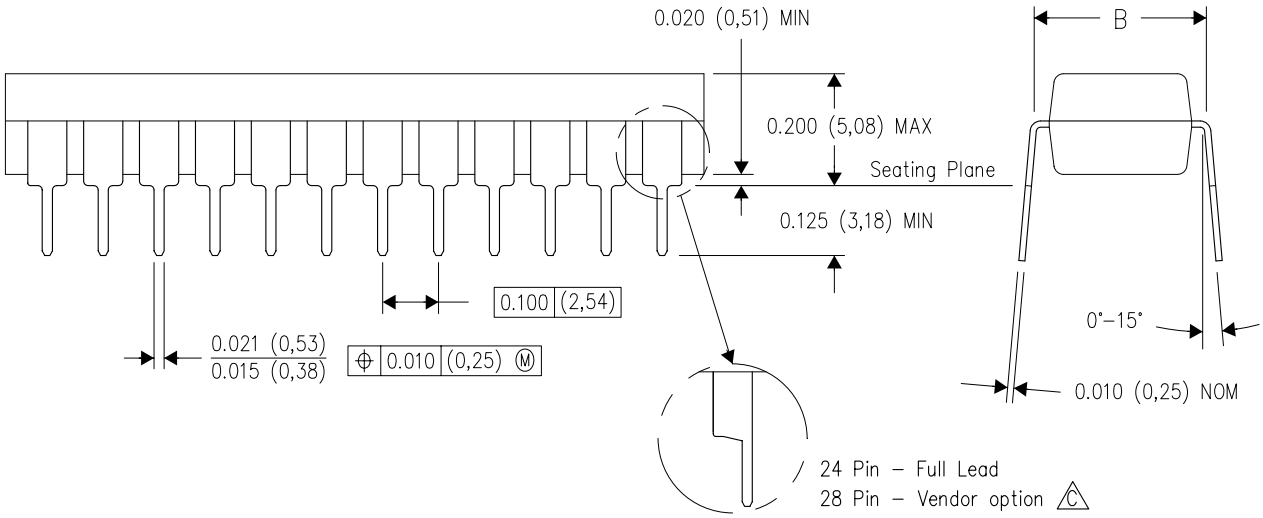
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

NT (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

24 PINS SHOWN



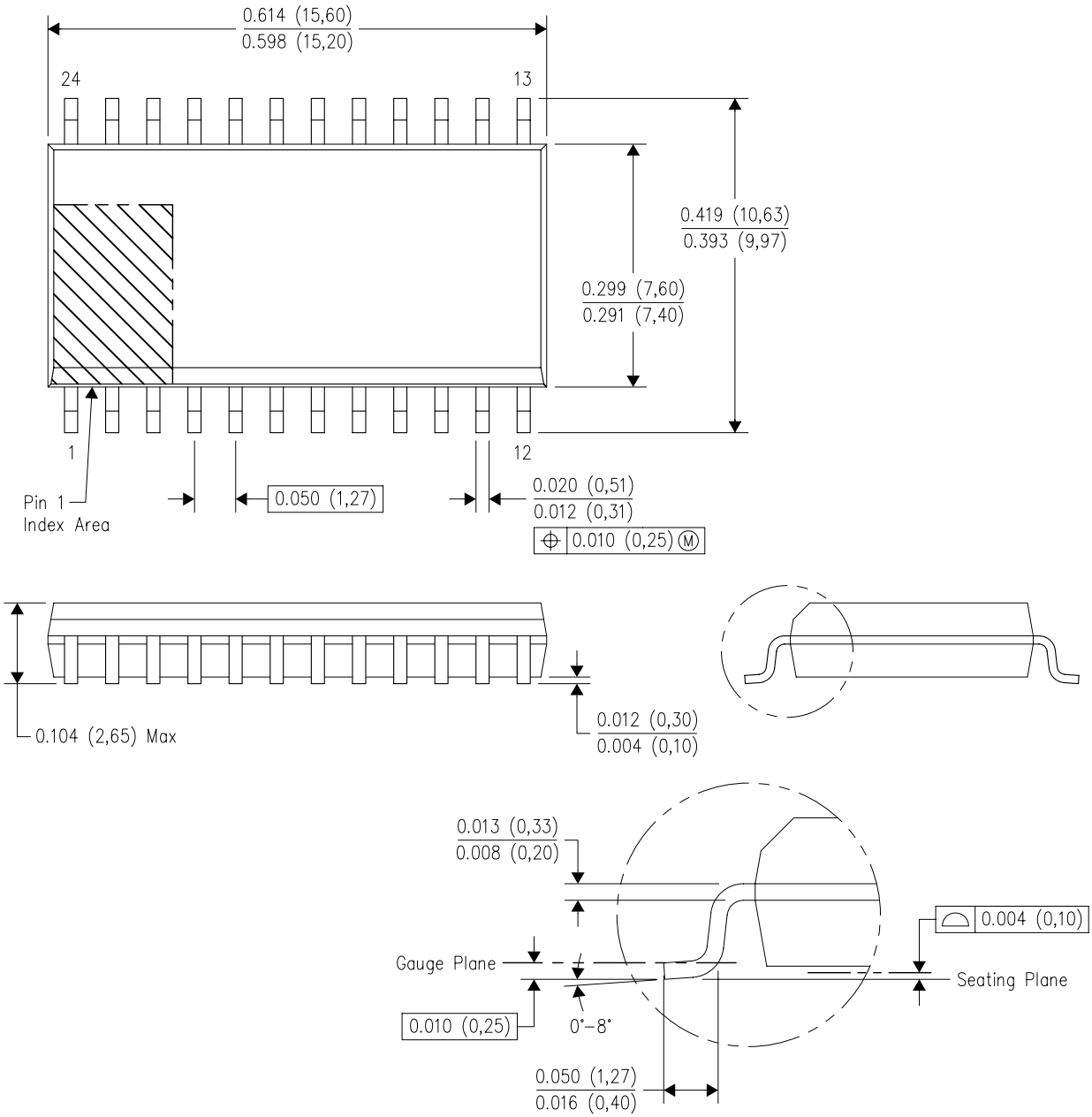

| DIM \ PINS ** | 24 | 28 |
|---|---|---|
| A MAX | 1.260 (32,04) | 1.425 (36,20) |
| A MIN | 1.230 (31,24) | 1.385 (35,18) |
| B MAX | 0.310 (7,87) | 0.315 (8,00) |
| B MIN | 0.290 (7,37) | 0.295 (7,49) |




4040050/C 04/09

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. The 28 pin end lead shoulder width is a vendor option, either half or full width.

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

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