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NTE4051B & NTE4051BT
Integrated Circuit
CMOS, Analog, Single 8–Channel
Multiplexer/Demultiplexer

Description:

The NTE4051B (16–Lead DIP) and NTE4051BT (SOIC–16) analog multiplexers are digitally–controlled analog switches. These devices effectively implement an SP8T solid state switch and feature low ON impedance and very low OFF leakage current. Control of analog signals up to the complete supply voltage range can be achieved.

Features:

- Triple Diode Protection on Control Inputs
- Switch Function is Break Before make
- Supply Voltage Range: 3Vdc to 18Vdc
- Analog Voltage Range ($V_{DD} - V_{EE}$): 3Vdc to 18Vdc (Note: V_{EE} must be $\leq V_{SS}$)
- Linearized Transfer Characteristics
- Low–Noise – 12nV / $\sqrt{\text{Cycle}}$, f $\geq$ 1kHz Typ

Absolute Maximum Ratings: (Voltages referenced to V_{SS}, Note 1, Note 2)

DC Supply Voltage, V_{DD} . . . . . –0.5 to +18.0V

Input Voltage (DC or Transient), V_{in}
(Referenced to V_{SS} for Control Inputs and V_{EE} for Switch I/O) . . . . . –0.5 to V_{DD} to +0.5V

Output Voltage (DC or Transient), V_{out}
(Referenced to V_{SS} for Control Inputs and V_{EE} for Switch I/O) . . . . . –0.5 to V_{DD} to +0.5V

Input Current (DC or Transient, Per Pin), I_{in} . . . . . ±10mA

Switch Through Current, I_{SW} . . . . . ±25mA

Power Dissipation (Per Package), P_D 500mW
Temperature Derating (from +65° to +125°C) . . . . . –7.0mW/°C

Ambient Temperature Range, T_A . . . . . –55° to +125°C

Storage Temperature Range, T_{stg} . . . . . –65° to +150°C

Lead Temperature (During Soldering, 8sec max), T_L . . . . . +260°C

Note 1. Stresses exceeding maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Note 2. These devices contain protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g. eiher V_{SS}, V_{EE} or V_{DD}), Unused outputs must be left open.

Electrical Characteristics: (Note 3)

Parameter	Symbol	V_{DD} Vdc	Test Conditions	−55°C		+25°C			+125°C		Unit
				Min	Max	Min	Typ	Max	Min	Max	
Supply Requirements (Voltages Referenced to V_{EE})											
Power Supply Voltage Range	V_{DD}	–	V_{DD} −3.0 ≥ V_{SS} ≥ V_{EE}	3	18	3	–	18	3	18	V
Quiescent Current Per Package	I_{DD}	5	Control Inputs: V_{in} = V_{SS} or V_{DD}, Switch I/O: V_{EE} ≤ $V_{I/O}$ ≤ V_{DD}, and ΔV_{switch} ≤ 500mV, Note 4	–	5	–	0.005	5	–	150	μA
		10		–	10	–	0.010	10	–	300	μA
		15		–	20	–	0.015	20	–	600	μA
Total Supply Current (Dynamic Plus Quiescent, Per Package)	$I_{D(AV)}$	5	T_A = +25°C only (The channel component, (V_{in} − V_{out}) / R_{on}, is not included)	Typical			(0.07μA/kHz) f + I_{DD}				μA
		10		Typical			(0.20μA/kHz) f + I_{DD}				μA
		15		Typical			(0.36μA/kHz) f + I_{DD}				μA
Control Inputs – INHIBIT, A, B, C (Voltages Referenced to V_{SS})											
Low−Level Input Voltage	V_{IL}	5	R_{on} = per spec, I_{off} = per spec	–	1.5	–	2.25	1.5	–	1.5	V
		10		–	3.0	–	4.50	3.0	–	3.0	V
		15		–	4.0	–	6.75	4.0	–	4.0	V
High−Level Input Voltage	V_{IH}	5	R_{on} = per spec, I_{off} = per spec	3.5	–	3.5	2.75	–	3.5	–	V
		10		7.0	–	7.0	5.50	–	7.0	–	V
		15		11.0	–	11.0	8.25	–	11.0	–	V
Input Leakage Current	I_{in}	15	V_{in} = 0 or V_{DD}	–	±0.1	–	±0.00001	±0.1	–	±1.0	μA
Input Capacitance	C_{in}	–		–	–	–	5.0	7.5	–	–	pF
Switches In/Out and Commons Out/In – X, Y, Z (Voltages Referenced to V_{EE})											
Recommended Peak−to−Peak Voltage Into or Out of the Switch	$V_{I/O}$	–	Channel On or Off	0	V_{DD}	0	–	V_{DD}	0	V_{DD}	V_{PP}
Recommended Static or Dynamic Voltage Across the Switch (Note 4)	ΔV_{switch}	–	Channel On	0	600	0	–	600	0	300	mV
Output Offset Voltage	V_{OO}	–	V_{in} = 0V, No Load	–	–	–	10	–	–	–	μV
On Resistance	R_{on}	5	ΔV_{switch} ≤ 500mV (Note 4) V_{in} = V_{IL} or V_{IH} (Control), and V_{in} = 0 to V_{DD} (Switch)	–	800	–	250	1050	–	1200	Ω
		10		–	400	–	120	500	–	520	Ω
		15		–	220	–	80	280	–	300	Ω
ΔOn Resistance between any Two Channels in the Same Package	ΔR_{on}	5		–	70	–	25	70	–	135	Ω
		10		–	50	–	10	50	–	95	Ω
		15		–	45	–	10	45	–	65	Ω
Off−Channel Leakage Current	I_{off}	15	V_{in} = V_{IL} or V_{IH} (Control) Channel to Channel or Any One Channel	–	±100	–	±0.05	±100	–	±1000	nA
Capacitance, Switch I/O	$C_{I/O}$	–	INHIBIT = V_{DD}	–	–	–	10	–	–	–	pF
Capacitance, Common O/I	$C_{O/I}$	–	INHIBIT = V_{DD}	–	–	–	60	–	–	–	pF
Capacitance, Feedthrough (Channel Off)	$C_{I/O}$	–	Pin Not Adjacent	–	–	–	0.15	–	–	–	pF
		–	Pin Adjacent	–	–	–	0.47	–	–	–	pF

Note 3. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

Note 4. For voltage drops across the switch (ΔV_{switch}) > 600mV (> 300mV at high temperatures), excessive V_{DD} current may be drawn, i.e. the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded (See the first page of this data sheet).

Electrical Characteristics: (C_L = 50pF, T_A = +25°C, $V_{EE} \le V_{SS}$, Note 5 unless otherwise specified)

Parameter	Symbol	$V_{DD} - V_{EE}$ Vdc	Min	Typ	Max	Unit
Propagation Delay Time Switch Input to Switch Output (R_L = 1kΩ) t_{PLH}, t_{PHL} = (0.17ns/pf) C_L + 26.5ns	t_{PLH}, t_{PHL}	5.0	–	35	90	ns
t_{PLH}, t_{PHL} = (0.08ns/pf) C_L + 11ns		10	–	15	40	ns
t_{PLH}, t_{PHL} = (0.06ns/pf) C_L + 9ns		15	–	12	30	ns
INHIBIT to Output (R_L = 10kΩ, $V_{EE} = V_{SS}$) Output "1" or "0" to High Impedance, or High Impedance to "1" or "0" Level	t_{PHZ}, t_{PLZ}, t_{PZH}, t_{PZL}	5.0	–	350	700	ns
		10	–	170	340	ns
		15	–	140	280	ns
Control Input to Output (R_L = 1kΩ, $V_{EE} = V_{SS}$)	t_{PLH}, t_{PHL}	5.0	–	360	720	ns
		10	–	160	320	ns
		15	–	120	240	ns
Second Harmonic Distortion (R_L = 10KΩ, f = 1kHz) $V_{in} = 5V_{PP}$	–	10	–	0.07	–	%
Bandwidth (R_L = 50Ω, V_{in} = 1/2 ($V_{DD} - V_{EE}$) p-p, C_L = 50pF 20 Log (V_{out}/V_{in}) = -3dB	BW	10	–	17	–	MHz
Off Channel Feedthrough Attenuation (R_L = 1KΩ, V_{in} = 1/2 ($V_{DD} - V_{EE}$) p-p, f_{in} = 4.5MHz	–	10	–	-50	–	dB
Channel Separation (R_L = 1kΩ, V_{in} = 1/2 ($V_{DD} - V_{EE}$) p-p, f_{in} = 3.0MHz	–	10	–	-50	–	dB
Crosstalk, Control Input to Common I/O (R_1 = 1kΩ, R_L = 10kΩ, Control $t_{TLH} = t_{THL}$ = 20ns, INHIBIT = V_{SS})	–	10	–	75	–	mV

Note 3. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the device's potential performance.

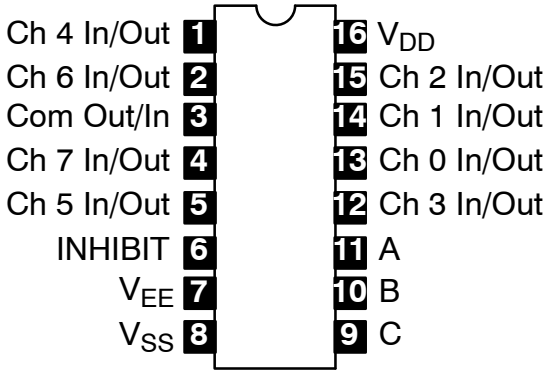
Note 5. The formulas given are for the typical characteristics only at +25°C.

Truth Table:

Control Inputs				ON Switches
Inhibit	Select			
	C	B	A	
0	0	0	0	X0
0	0	0	1	X1
0	0	1	0	X2
0	0	1	1	X3
0	1	0	0	X4
0	1	0	1	X5
0	1	1	0	X6
0	1	1	1	X7
1	X	X	X	None

X = Don't Care

Pin Connection Diagram



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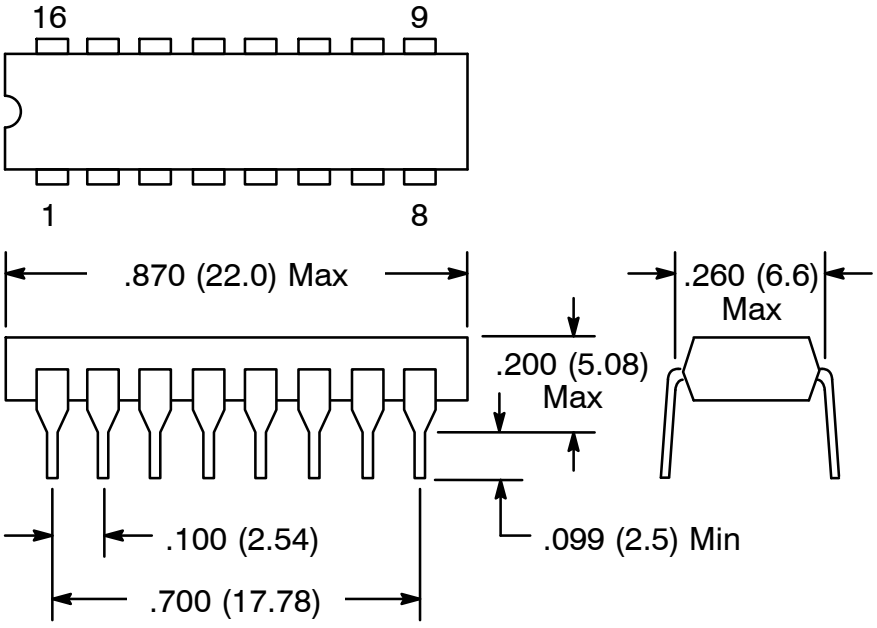

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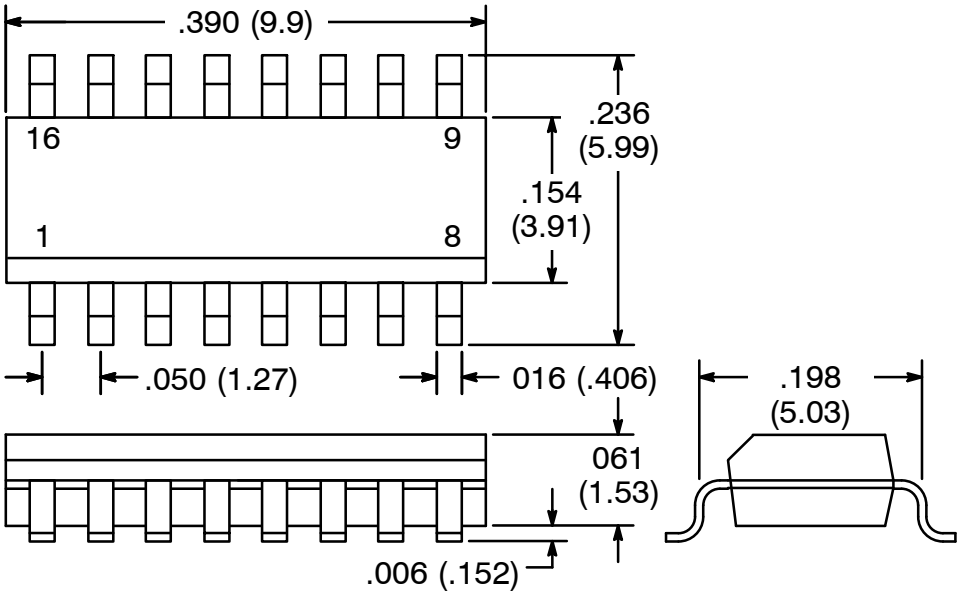

NOTE: Pin1 on Beveled Edge