

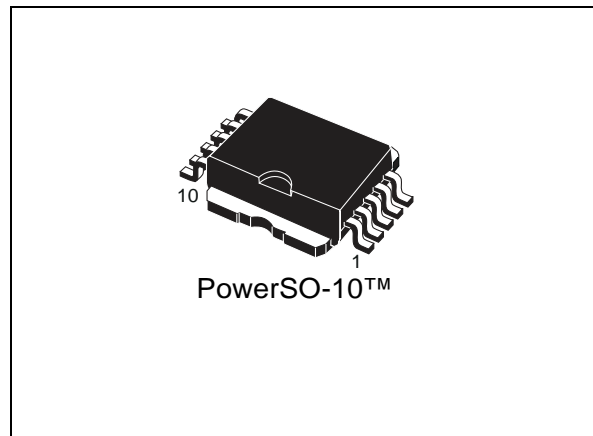
Double channel high-side driver

Features

Type	$R_{DS(on)}$	I_{out}	V_{CC}
VND810SP-E	160 m Ω ⁽¹⁾	3.5 A ⁽¹⁾	36 V

1. Per each channel.

- ECOPACK[®]: lead free and RoHS compliant
- Automotive Grade: compliance with AEC guidelines
- Very low standby current
- CMOS compatible input
- On-state open-load detection
- Off-state open-load detection
- Thermal shutdown protection and diagnosis
- Undervoltage shutdown
- Overvoltage clamp
- Output stuck to V_{CC} detection
- Load current limitation
- Reverse battery protection
- Electrostatic discharge protection



Description

The VND810SP-E is a monolithic device made by using STMicroelectronics[™] VIPower[™] M0-3 technology, intended for driving any kind of load with one side connected to ground.

Active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table).

Active current limitation combined with thermal shutdown and automatic restart protects the device against overload. The device detects open-load condition both in on-state and off-state. Output shorted to V_{CC} is detected in the off-state. Device automatically turns-off in case of ground pin disconnection.

Table 1. Order codes

Package	Order code	
	Tube	Tape and reel
PowerSO-10 [™]	VND810SP-E	VND810SPTR-E

Contents

1	Block diagram and pin description	5
2	Electrical specifications	6
2.1	Absolute maximum ratings	6
2.2	Thermal data	7
2.3	Electrical characteristics	7
2.4	Electrical characteristics curves	14
3	Application information	17
3.1	GND protection network against reverse battery	17
3.1.1	Solution 1: a resistor in the ground line (RGND only)	17
3.1.2	Solution 2: a diode (D_{GND}) in the ground line	18
3.1.3	Load dump protection	18
3.2	MCU I/O protection	18
3.2.1	Open-load detection in off-state	18
3.3	Maximum demagnetization energy	20
4	Package and PCB thermal data	21
4.1	PowerSO-10 thermal data	21
5	Package and packing information	24
5.1	ECOPACK [®] packages	24
5.2	PowerSO-10 mechanical data	24
5.3	PowerSO-10 packing information	26
6	Revision history	27

List of tables

Table 1.	Order codes	1
Table 2.	Suggested connections for unused and not connected pins	5
Table 3.	Absolute maximum ratings	6
Table 4.	Thermal data	7
Table 5.	Power output	7
Table 7.	V _{CC} output diode	8
Table 8.	Status pin	8
Table 6.	Protection	8
Table 9.	Switching (V _{CC} = 13 V)	9
Table 10.	Open-load detection	9
Table 11.	Logic input	9
Table 12.	Truth table	11
Table 13.	Electrical transient requirements on V _{CC} pin (part 1)	12
Table 14.	Electrical transient requirements on V _{CC} pin (part 2)	12
Table 15.	Electrical transient requirements on V _{CC} pin (part 3)	12
Table 16.	Thermal parameter	23
Table 17.	PowerSO-10 mechanical data	25
Table 18.	Document revision history	27

List of figures

Figure 1.	Block diagram	5
Figure 2.	Configuration diagram (top view)	5
Figure 3.	Current and voltage conventions	6
Figure 4.	Status timing	10
Figure 5.	Switching time waveforms	10
Figure 6.	Waveforms	13
Figure 7.	Off-state output current.	14
Figure 8.	High level input current.	14
Figure 9.	Input clamp voltage.	14
Figure 10.	Status leakage current	14
Figure 11.	Status low output voltage	14
Figure 12.	Status clamp voltage	14
Figure 13.	On-state resistance vs T_{case}	15
Figure 14.	On-state resistance vs V_{CC}	15
Figure 15.	Open-load on-state detection threshold	15
Figure 16.	Open-load off-state detection threshold	15
Figure 17.	Input high level	15
Figure 18.	Input low level	15
Figure 19.	Input hysteresis voltage	16
Figure 20.	Overvoltage shutdown	16
Figure 21.	Turn-on voltage slope	16
Figure 22.	Turn-off voltage slope	16
Figure 23.	I_{LIM} vs T_{case}	16
Figure 24.	Application schematic.	17
Figure 25.	Open-load detection in off-state	19
Figure 26.	Maximum turn-off current versus load inductance	20
Figure 27.	PowerSO-10 PC board.	21
Figure 28.	PowerSO-10 $R_{thj-amb}$ vs PCB copper area in open box free air condition	21
Figure 29.	PowerSO-10 thermal impedance junction ambient single pulse.	22
Figure 30.	Thermal fitting model of a double channel HSD in PowerSO-10	22
Figure 31.	PowerSO-10 package dimensions	24
Figure 32.	PowerSO-10 suggested pad layout and tube shipment (no suffix).	26
Figure 33.	Tape and reel shipment (suffix "TR")	26

1 Block diagram and pin description

Figure 1. Block diagram

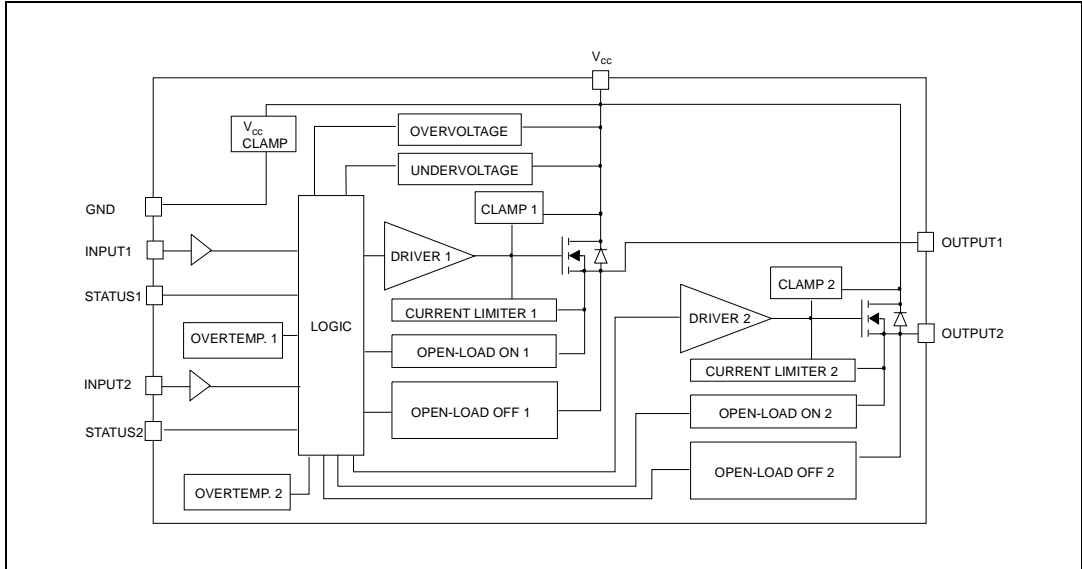


Figure 2. Configuration diagram (top view)

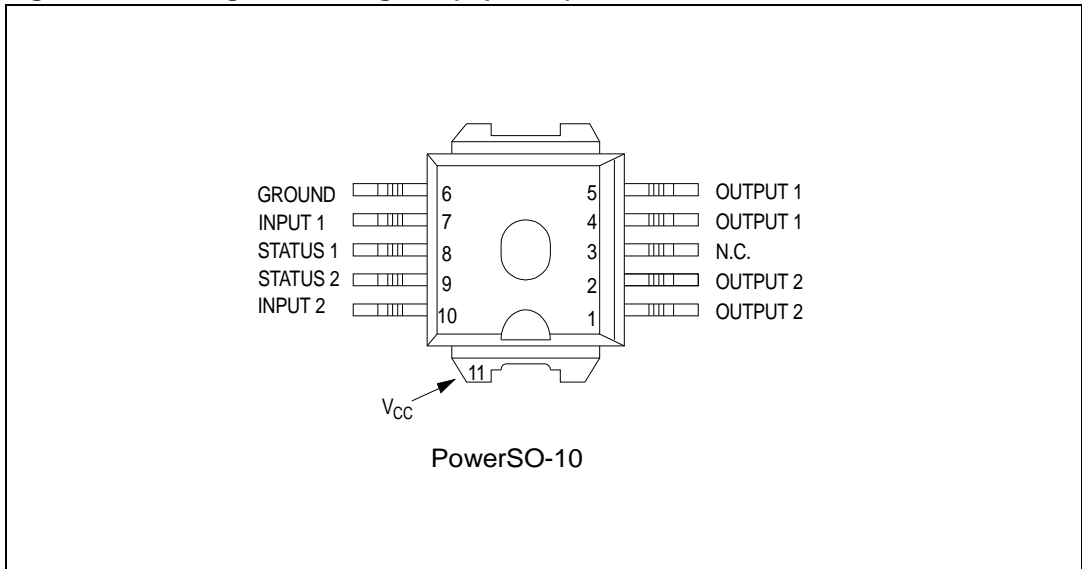
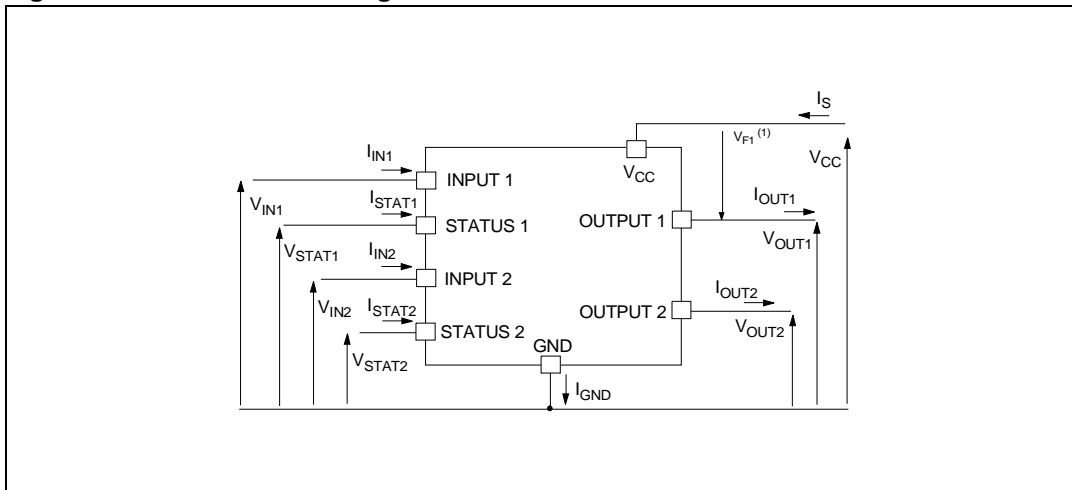


Table 2. Suggested connections for unused and not connected pins

Connection / pin	Status	N.C.	Output	Input
Floating	X	X	X	X
To ground		X		Through 10 KΩ resistor

2 Electrical specifications

Figure 3. Current and voltage conventions



1) $V_{F1} = V_{CCn} - V_{OUTn}$ during reverse battery condition.

2.1 Absolute maximum ratings

Stressing the device above the rating listed in [Table 3](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics sure program and other relevant quality document.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{CC}	DC supply voltage	41	V
-V _{CC}	Reverse DC supply voltage	-0.3	V
-I _{GND}	DC reverse ground pin current	-200	mA
I _{OUT}	DC output current	Internally Limited	A
-I _{OUT}	Reverse DC output current	-6	A
I _{IN}	DC input current	+/- 10	mA
I _{stat}	DC status current	+/- 10	mA
V _{ESD}	Electrostatic discharge (Human Body Model: R = 1.5 KΩ; C = 100 pF)		
	- INPUT	4000	V
	- STATUS	4000	V
	- OUTPUT	5000	V
	- V _{CC}	5000	V

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
E_{MAX}	Maximum switching energy ($L = 1.4 \text{ mH}$; $R_L = 0 \text{ } \Omega$; $V_{bat} = 13.5 \text{ V}$; $T_{jstart} = 150 \text{ } ^\circ\text{C}$; $I_L = 5 \text{ A}$)	24	mJ
P_{tot}	Power dissipation $T_C = 25 \text{ } ^\circ\text{C}$	52	W
T_j	Junction operating temperature	Internally Limited	$^\circ\text{C}$
T_C	Case operating temperature	-40 to 150	$^\circ\text{C}$
T_{stg}	Storage temperature	-55 to 150	$^\circ\text{C}$

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	2.4	$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	52.4 ⁽¹⁾ 37 ⁽²⁾	$^\circ\text{C/W}$

- When mounted on a standard single-sided FR-4 board with 0.5 cm² of Cu (at least 35 μm thick). Horizontal mounting and no artificial air flow.
- When mounted on a standard single-sided FR-4 board with 6 cm² of Cu (at least 35 μm thick). Horizontal mounting and no artificial air flow

2.3 Electrical characteristics

Values specified in this section are for $8 \text{ V} < V_{CC} < 36 \text{ V}$; $-40 \text{ } ^\circ\text{C} < T_j < 150 \text{ } ^\circ\text{C}$, unless otherwise stated.

(Per each channel)

Table 5. Power output

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CC}^{(1)}$	Operating supply voltage		5.5	13	36	V
$V_{USD}^{(1)}$	Undervoltage shutdown		3	4	5.5	V
$V_{OV}^{(1)}$	Overvoltage shutdown		36			V
R_{ON}	On-state resistance	$I_{OUT} = 1 \text{ A}$; $T_j = 25 \text{ } ^\circ\text{C}$ $I_{OUT} = 1 \text{ A}$; $V_{CC} > 8 \text{ V}$			160 320	m Ω m Ω
$I_S^{(1)}$	Supply current	Off-state; $V_{CC} = 13 \text{ V}$; $V_{IN} = V_{OUT} = 0 \text{ V}$ Off-state; $V_{CC} = 13 \text{ V}$; $V_{IN} = V_{OUT} = 0 \text{ V}$; $T_j = 25 \text{ } ^\circ\text{C}$ On-state; $V_{CC} = 13 \text{ V}$; $V_{IN} = 5 \text{ V}$; $I_{OUT} = 0 \text{ A}$		12 12 5	40 25 7	μA μA mA
$I_{L(off1)}$	Off-state output current	$V_{IN} = V_{OUT} = 0 \text{ V}$	0		50	μA

Table 5. Power output (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{L(off2)}$	Off-state output current	$V_{IN} = 0\text{ V}; V_{OUT} = 3.5\text{ V}$	-75		0	μA
$I_{L(off3)}$	Off-state output current	$V_{IN} = V_{OUT} = 0\text{ V}; V_{CC} = 13\text{ V}; T_j = 125\text{ }^\circ\text{C}$			5	μA
$I_{L(off4)}$	Off-state output current	$V_{IN} = V_{OUT} = 0\text{ V}; V_{CC} = 13\text{ V}; T_j = 25\text{ }^\circ\text{C}$			3	μA

1. Per device.

Table 6. Protection⁽¹⁾

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_{TSD}	Shutdown temperature		150	175	200	$^\circ\text{C}$
T_R	Reset temperature		135			$^\circ\text{C}$
T_{hyst}	Thermal hysteresis		7	15		$^\circ\text{C}$
t_{sdl}	Status delay in overload conditions	$T_j > T_{TSD}$			20	μs
I_{lim}	Current limitation	$V_{CC} = 13\text{ V}$ $5.5\text{ V} < V_{CC} < 36\text{ V}$	3.5	5	7.5 7.5	A A
V_{demag}	Turn-off output clamp voltage	$I_{OUT} = 1\text{ A}; L = 6\text{ mH}$	$V_{CC}-41$	$V_{CC}-48$	$V_{CC}-55$	V

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles

Table 7. V_{CC} output diode

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_F	Forward on voltage	$-I_{OUT} = 0.5\text{ A}; T_j = 150\text{ }^\circ\text{C}$	-	-	0.6	V

Table 8. Status pin

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{STAT}	Status low output voltage	$I_{STAT} = 1.6\text{ mA}$			0.5	V
I_{LSTAT}	Status leakage current	Normal operation; $V_{STAT} = 5\text{ V}$			10	μA
C_{STAT}	Status pin input capacitance	Normal operation; $V_{STAT} = 5\text{ V}$			100	pF
V_{SCL}	Status clamp voltage	$I_{STAT} = 1\text{ mA}$ $I_{STAT} = -1\text{ mA}$	6	6.8 -0.7	8	V V

Table 9. Switching ($V_{CC} = 13\text{ V}$)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on delay time	$R_L = 13\ \Omega$ from V_{IN} rising edge to $V_{OUT} = 1.3\text{ V}$	-	30	-	μs
$t_{d(off)}$	Turn-off delay time	$R_L = 13\ \Omega$ from V_{IN} falling edge to $V_{OUT} = 11.7\text{ V}$	-	30	-	μs
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	$R_L = 13\ \Omega$ from $V_{OUT} = 1.3\text{ V}$ to $V_{OUT} = 10.4\text{ V}$	-	See Table 21	-	$\text{V}/\mu\text{s}$
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	$R_L = 13\ \Omega$ from $V_{OUT} = 11.7\text{ V}$ to $V_{OUT} = 1.3\text{ V}$	-	See Table 22	-	$\text{V}/\mu\text{s}$

Table 10. Open-load detection

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
I_{OL}	Open-load on-state detection threshold	$V_{IN} = 5\text{ V}$	20	40	80	mA
$t_{DOL(on)}$	Open-load on-state detection delay	$I_{OUT} = 0\text{ A}$			200	μs
V_{OL}	Open-load off-state voltage detection threshold	$V_{IN} = 0\text{ V}$	1.5	2.5	3.5	V
$t_{DOL(off)}$	Open-load detection delay at turn-off				1000	μs

Table 11. Logic input

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{IL}	Input low level				1.25	V
I_{IL}	Low level input current	$V_{IN} = 1.25\text{ V}$	1			μA
V_{IH}	Input high level		3.25			V
I_{IH}	High level input current	$V_{IN} = 3.25\text{ V}$			10	μA
V_{hyst}	Input hysteresis voltage		0.5			V
V_{ICL}	Input clamp voltage	$I_{IN} = 1\text{ mA}$ $I_{IN} = -1\text{ mA}$	6	6.8 -0.7	8	V V

Figure 4. Status timing

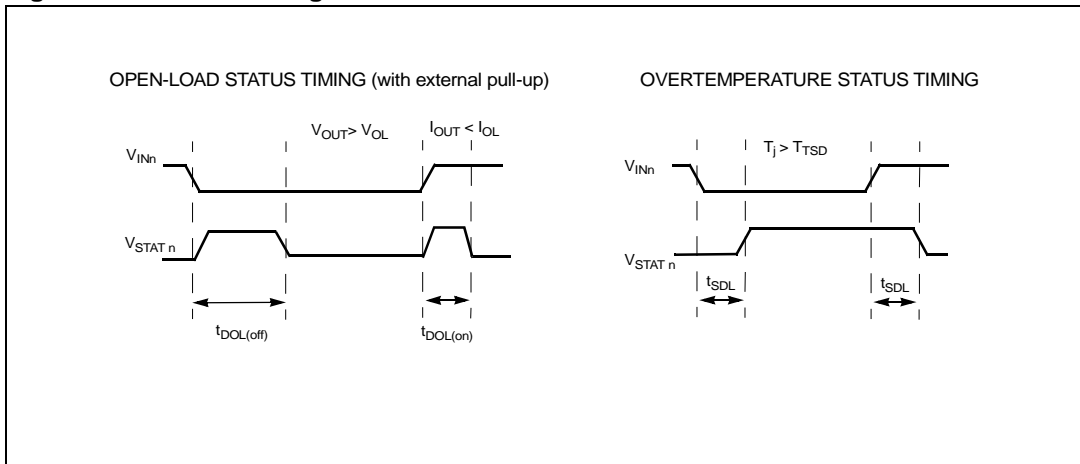


Figure 5. Switching time waveforms

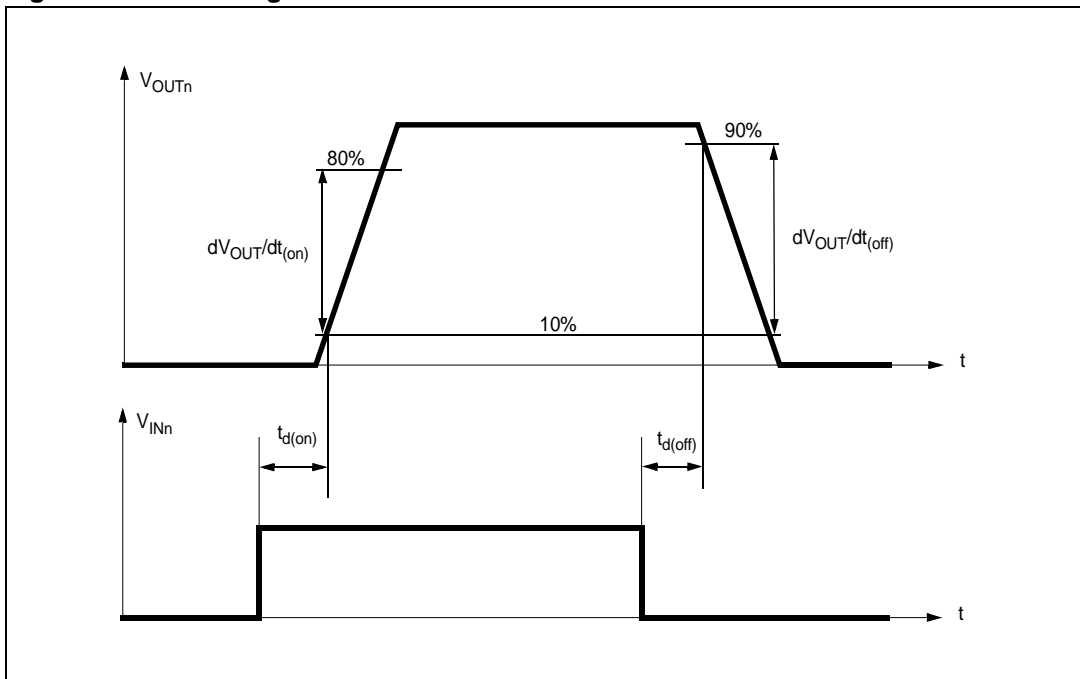


Table 12. Truth table

Conditions	Input	Output	Status
Normal operation	L	L	H
	H	H	H
Current limitation	L	L	H
	H	X	($T_j < T_{TSD}$) H
	H	X	($T_j > T_{TSD}$) L
Overtemperature	L	L	H
	H	L	L
Undervoltage	L	L	X
	H	L	X
Overvoltage	L	L	H
	H	L	H
Output voltage $> V_{OL}$	L	H	L
	H	H	H
Output current $< I_{OL}$	L	L	H
	H	H	L

Table 13. Electrical transient requirements on V_{CC} pin (part 1)

ISO T/R 7637/1 Test pulse	Test levels				Delays and impedance
	I	II	III	IV	
1	-25 V	-50 V	-75 V	-100 V	2 ms, 10 Ω
2	+25 V	+50 V	+75 V	+100 V	0.2 ms, 10 Ω
3a	-25 V	-50 V	-100 V	-150 V	0.1 μs, 50 Ω
3b	+25 V	+50 V	+75 V	+100 V	0.1 μs, 50 Ω
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 Ω
5	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400 ms, 2 Ω

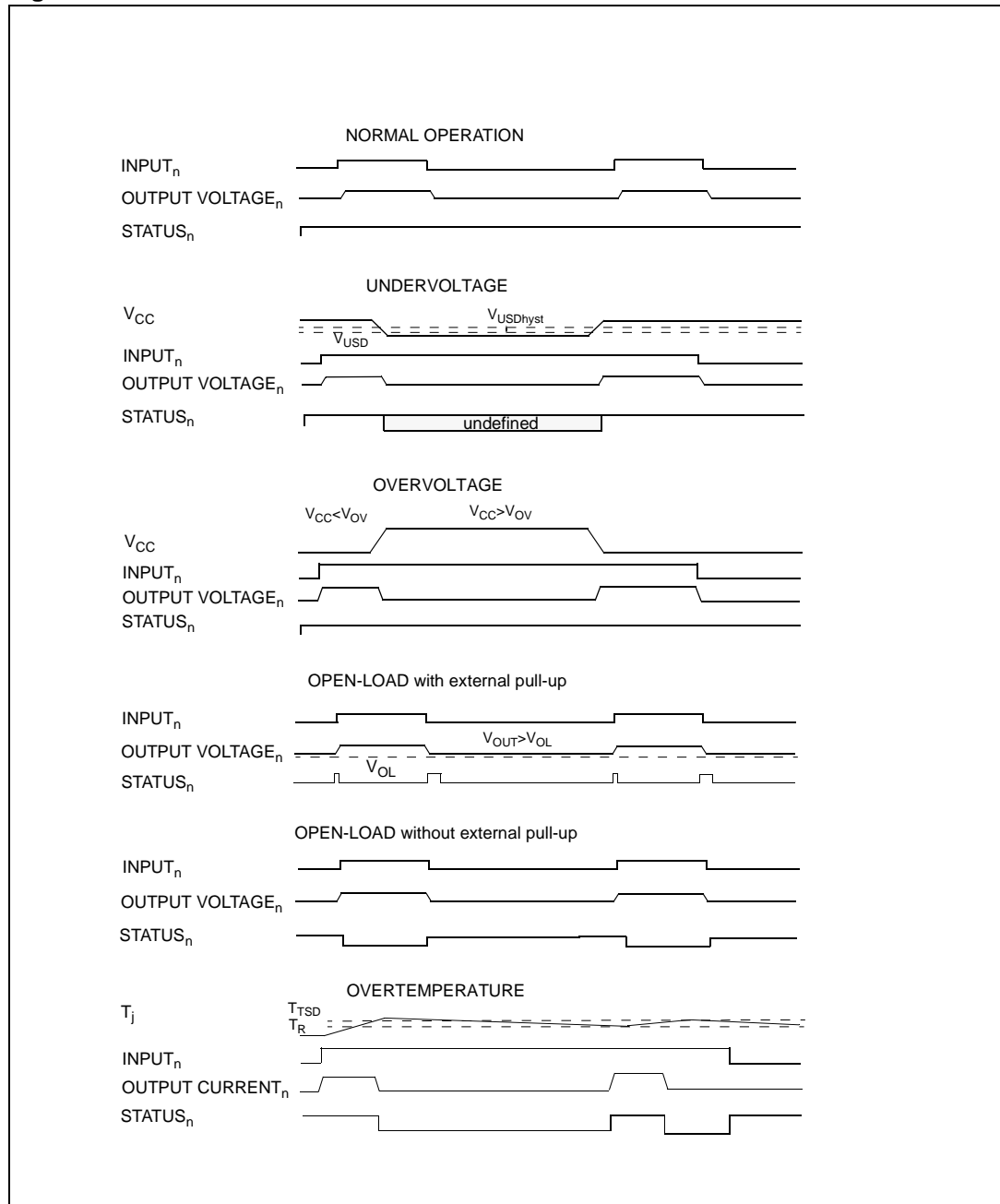
Table 14. Electrical transient requirements on V_{CC} pin (part 2)

ISO T/R 7637/1 Test pulse	Test levels			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

Table 15. Electrical transient requirements on V_{CC} pin (part 3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure and cannot be returned to proper operation without replacing the device.

Figure 6. Waveforms



2.4 Electrical characteristics curves

Figure 7. Off-state output current

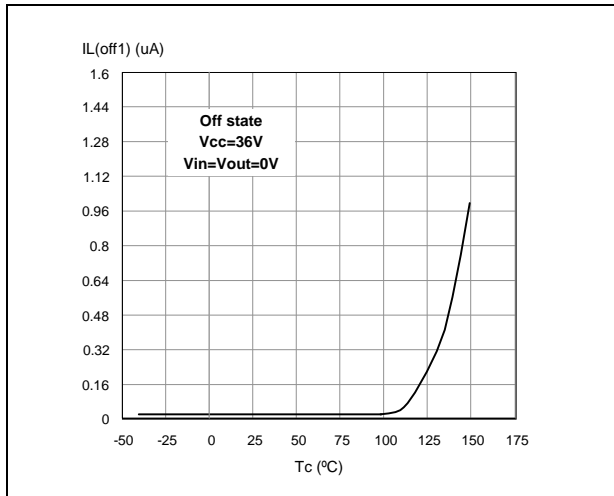


Figure 8. High level input current

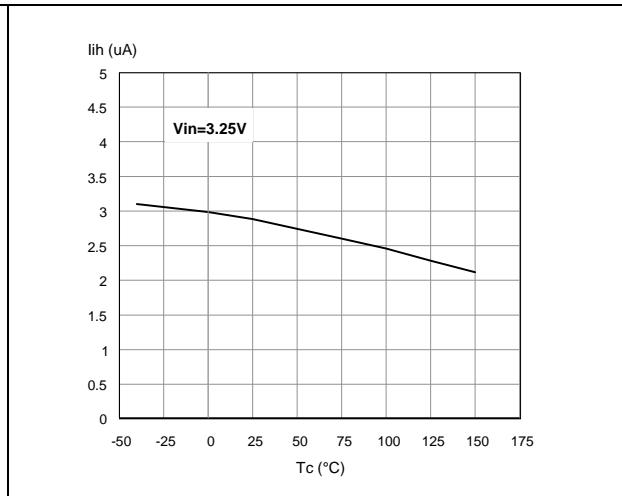


Figure 9. Input clamp voltage

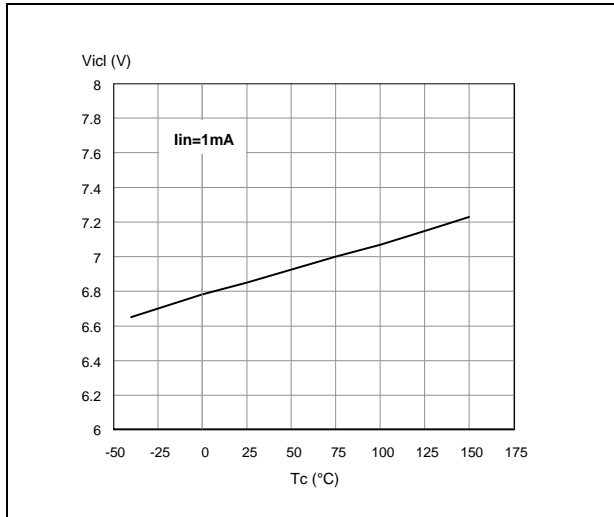


Figure 10. Status leakage current

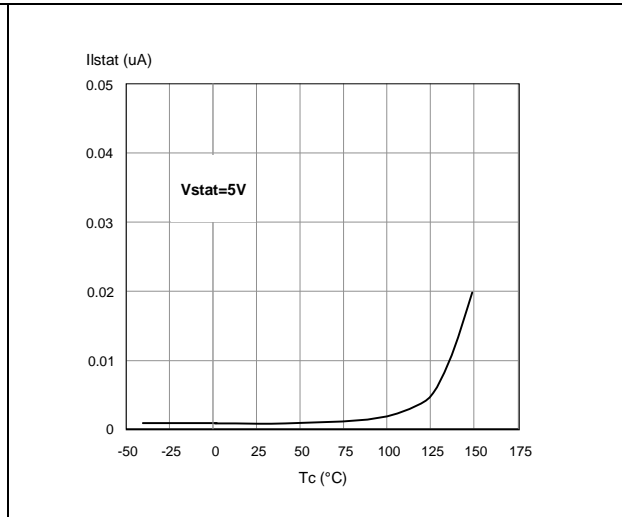


Figure 11. Status low output voltage

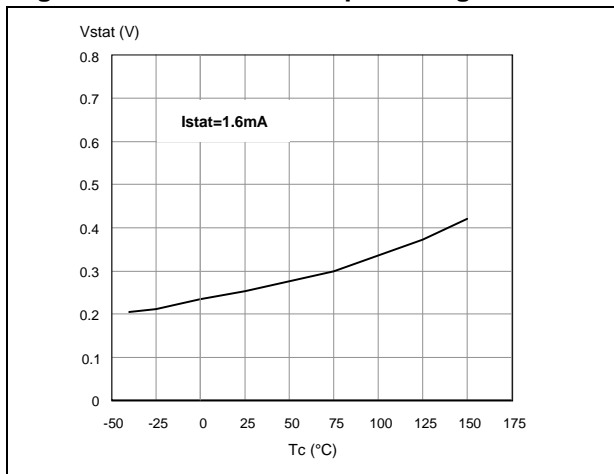


Figure 12. Status clamp voltage

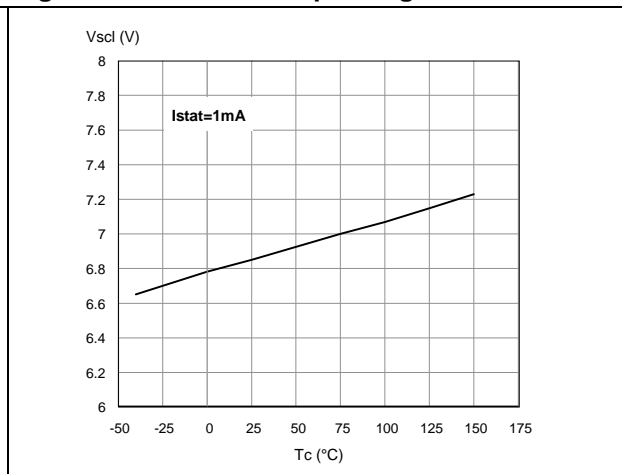


Figure 13. On-state resistance vs T_{case}

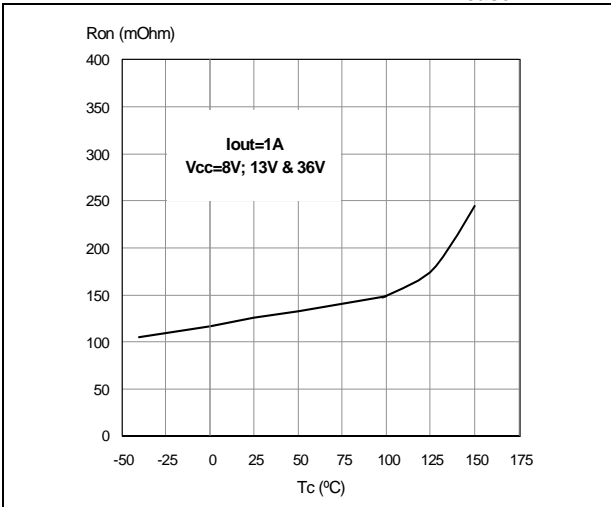


Figure 14. On-state resistance vs V_{CC}

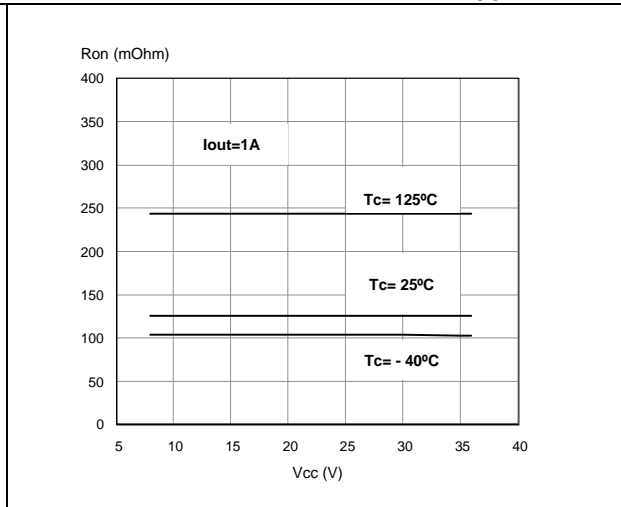


Figure 15. Open-load on-state detection threshold

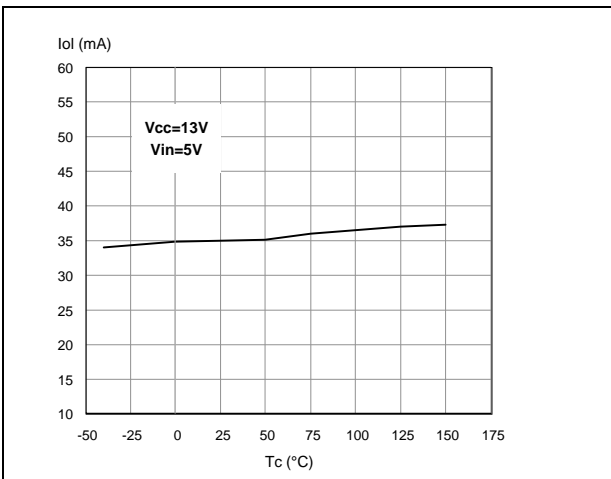


Figure 16. Open-load off-state detection threshold

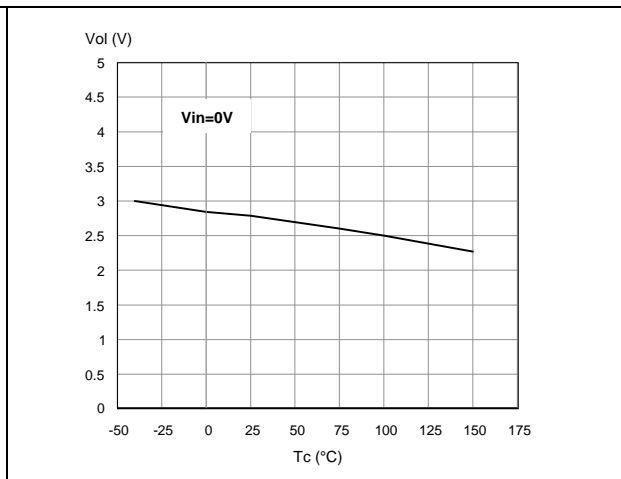


Figure 17. Input high level

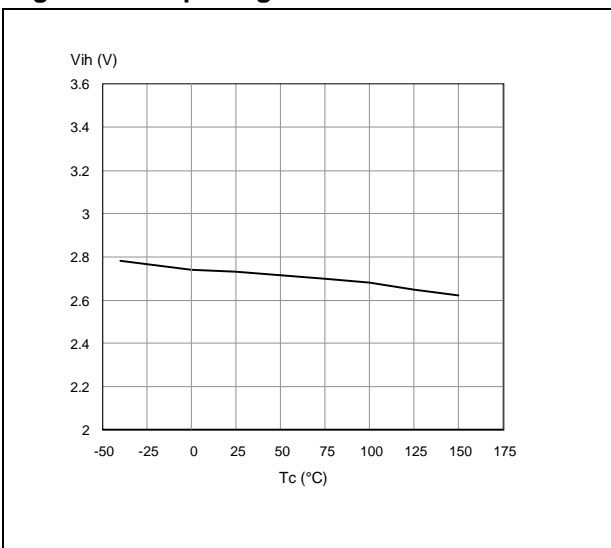


Figure 18. Input low level

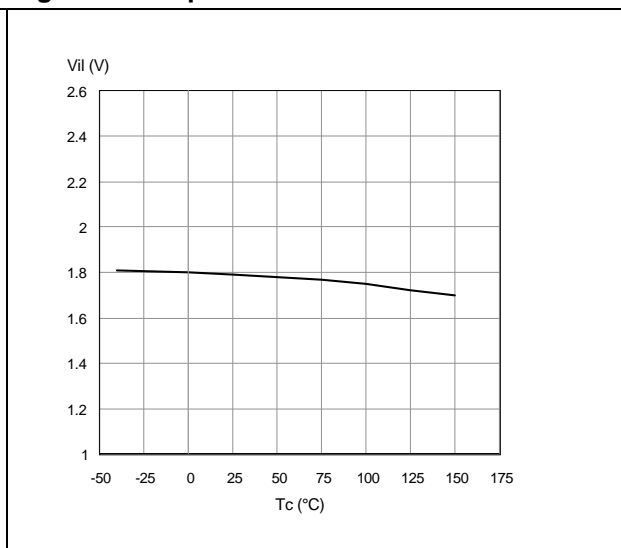


Figure 19. Input hysteresis voltage

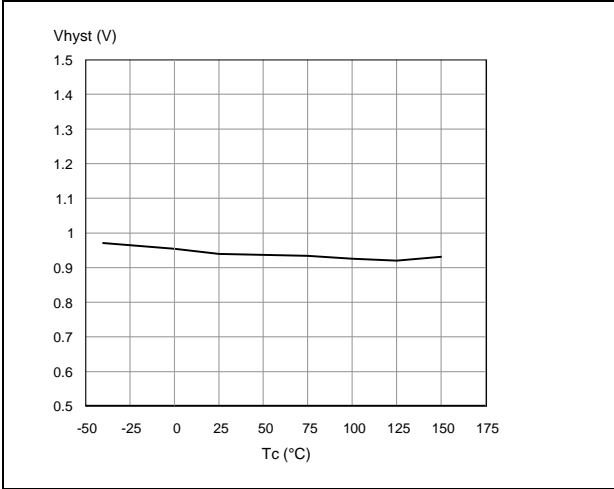


Figure 20. Overvoltage shutdown

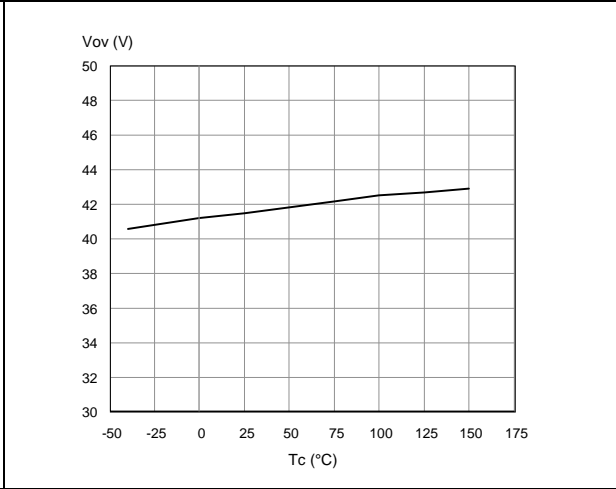


Figure 21. Turn-on voltage slope

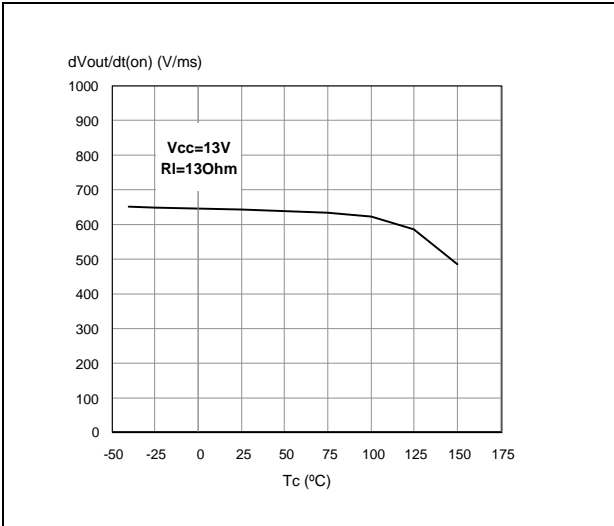


Figure 22. Turn-off voltage slope

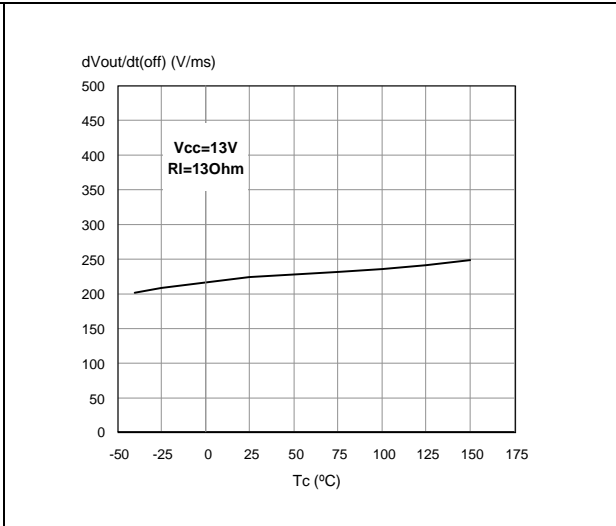
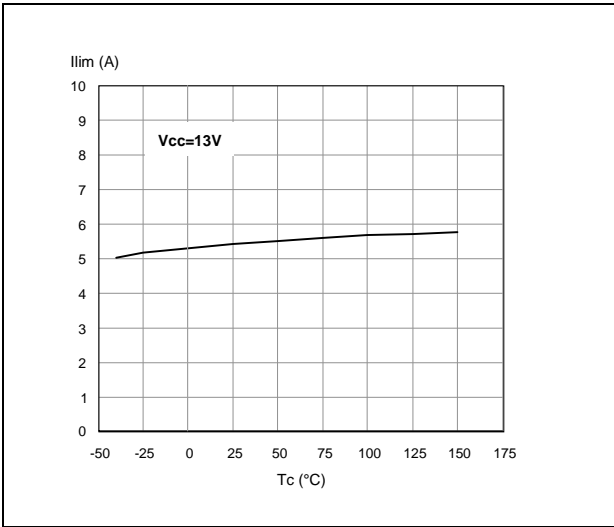
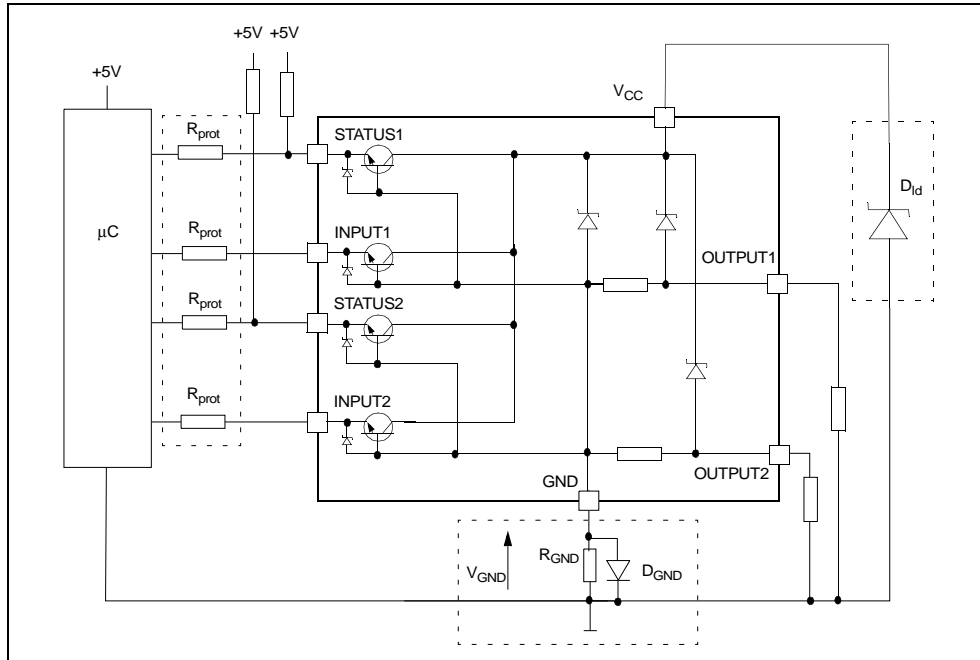


Figure 23. I_{LIM} vs T_{case}



3 Application information

Figure 24. Application schematic



3.1 GND protection network against reverse battery

This section provides two solutions for implementing a ground protection network against reverse battery.

3.1.1 Solution 1: a resistor in the ground line (R_{GND} only)

This can be used with any type of load.

The following shows how to dimension the R_{GND} resistor:

1. $R_{GND} \leq 600 \text{ mV} / I_{S(on)max}$
2. $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device's datasheet.

Power dissipation in R_{GND} (when $V_{CC} < 0$ during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that, if the microprocessor ground is not common with the device ground, then the R_{GND} produces a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift varies depending on how many devices are ON in the case of several high side drivers sharing the same R_{GND} .

If the calculated power dissipation requires the use of a large resistor, or several devices have to share the same resistor, then ST suggests using [Section 3.1.2](#) described below.

3.1.2 Solution 2: a diode (D_{GND}) in the ground line

A resistor ($R_{GND} = 1 \text{ k}\Omega$) should be inserted in parallel to D_{GND} if the device is driving an inductive load. This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network produce a shift ($\sim 600 \text{ mV}$) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift does not vary if more than one HSD shares the same diode/resistor network. Series resistor in INPUT and STATUS lines are also required to prevent that, during battery voltage transient, the current exceeds the absolute maximum rating. Safest configuration for unused INPUT and STATUS pin is to leave them unconnected.

3.1.3 Load dump protection

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds V_{CC} max DC rating. The same applies if the device is subjected to transients on the V_{CC} line that are greater than the ones shown in [Table 13](#).

3.2 MCU I/O protection

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins is pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the microcontroller I/O pins from latching up.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os:

$$-V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Example

For the following conditions:

$$V_{CCpeak} = -100 \text{ V}$$

$$I_{latchup} \geq 20 \text{ mA}$$

$$V_{OH\mu C} \geq 4.5 \text{ V}$$

$$5 \text{ k}\Omega \leq R_{prot} \leq 65 \text{ k}\Omega.$$

The recommended values are:

$$R_{prot} = 10 \text{ k}\Omega$$

3.2.1 Open-load detection in off-state

Off-state open-load detection requires an external pull-up resistor (R_{PU}) connected between OUTPUT pin and a positive supply voltage (V_{PU}) like the +5 V line used to supply the microprocessor.

The external resistor has to be selected according to the following requirements:

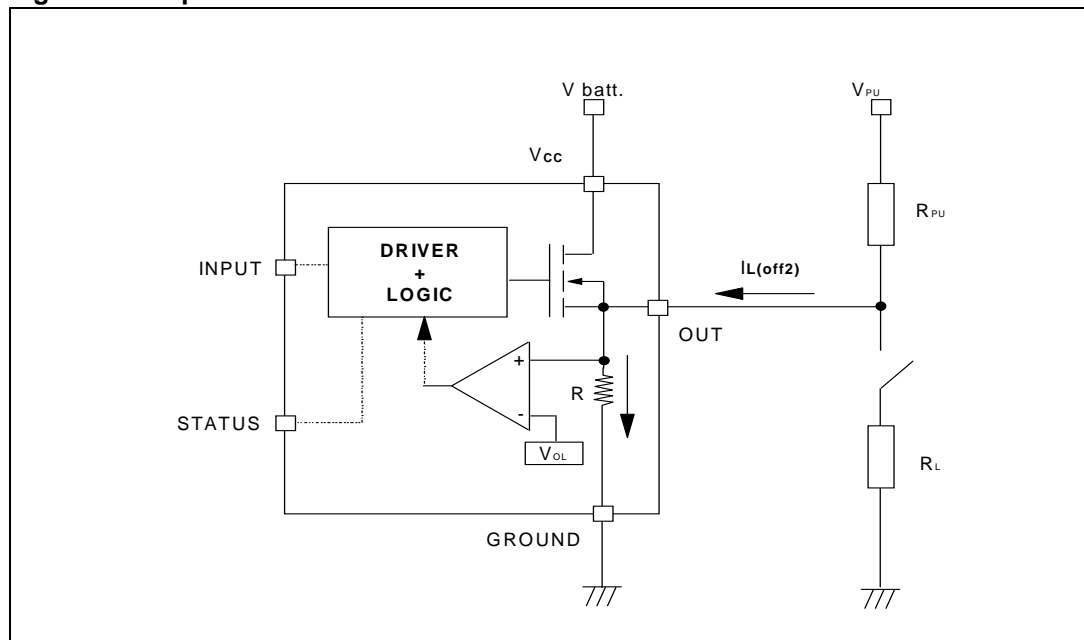
1. No false open-load indication when load is connected: in this case it needs to avoid V_{OUT} to be higher than V_{OLmin} ; this results in the following condition:

$$V_{OUT} = (V_{PU} / (R_L + R_{PU})) R_L < V_{OLmin}.$$
2. No misdetection when load is disconnected: in this case the V_{OUT} has to be higher than V_{OLmax} ; this results in the following condition $R_{PU} < (V_{PU} - V_{OLmax}) / I_{L(off2)}$.

Because $I_{s(OFF)}$ may significantly increase if V_{out} is pulled high (up to several mA), the pull-up resistor R_{PU} should be connected to a supply that is switched OFF when the module is in standby.

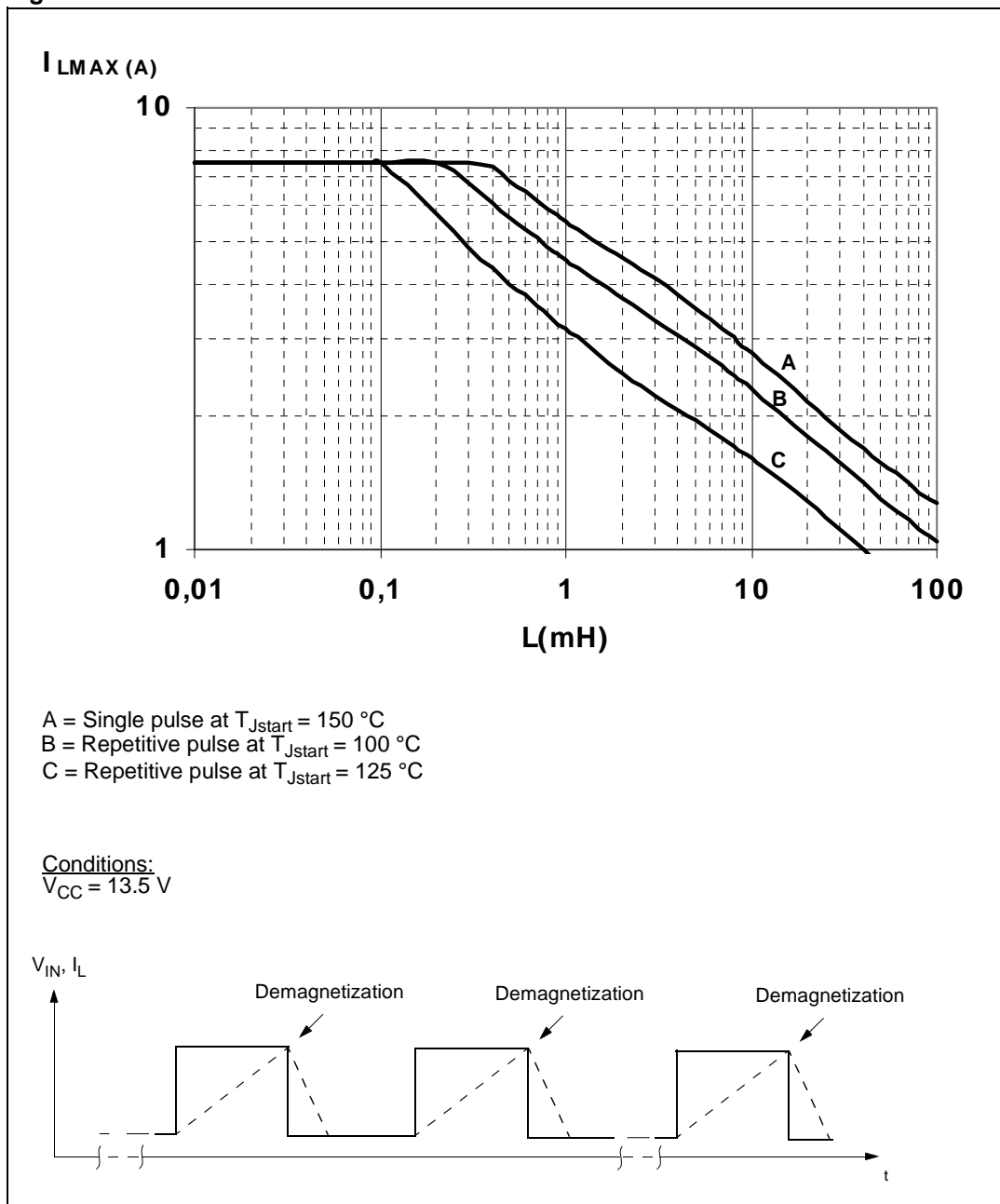
The values of V_{OLmin} , V_{OLmax} and $I_{L(off2)}$ are available in [Section 2.3](#).

Figure 25. Open-load detection in off-state



3.3 Maximum demagnetization energy

Figure 26. Maximum turn-off current versus load inductance

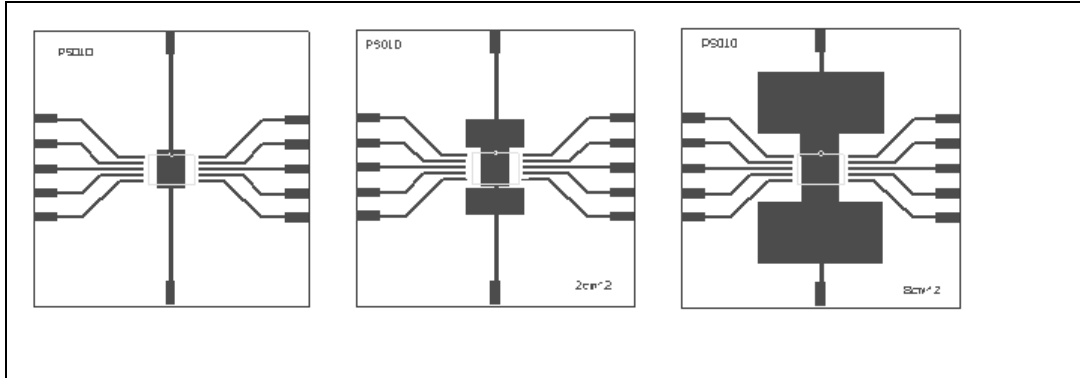


- Values are generated with $R_l = 0\ \Omega$. In case of repetitive pulses, T_{Jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

4 Package and PCB thermal data

4.1 PowerSO-10 thermal data

Figure 27. PowerSO-10 PC board



1. Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area= 58 mm x 58 mm, PCB thickness = 2 mm, Cu thickness = 35 μ m, Copper areas: from minimum pad lay-out to 8 cm²).

Figure 28. PowerSO-10 $R_{thj-amb}$ vs PCB copper area in open box free air condition

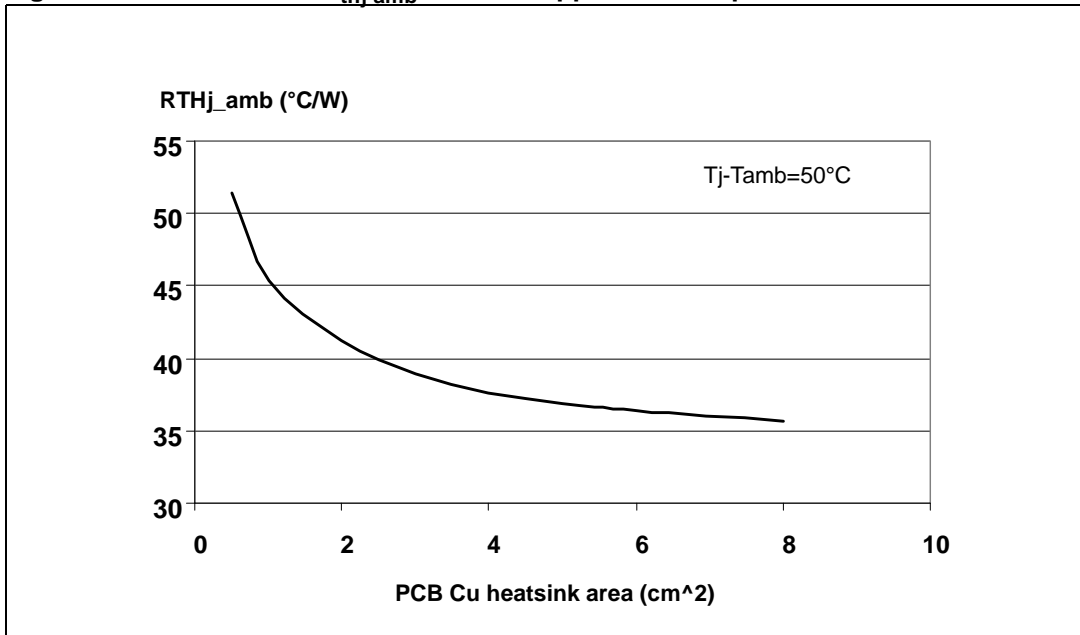


Figure 29. PowerSO-10 thermal impedance junction ambient single pulse

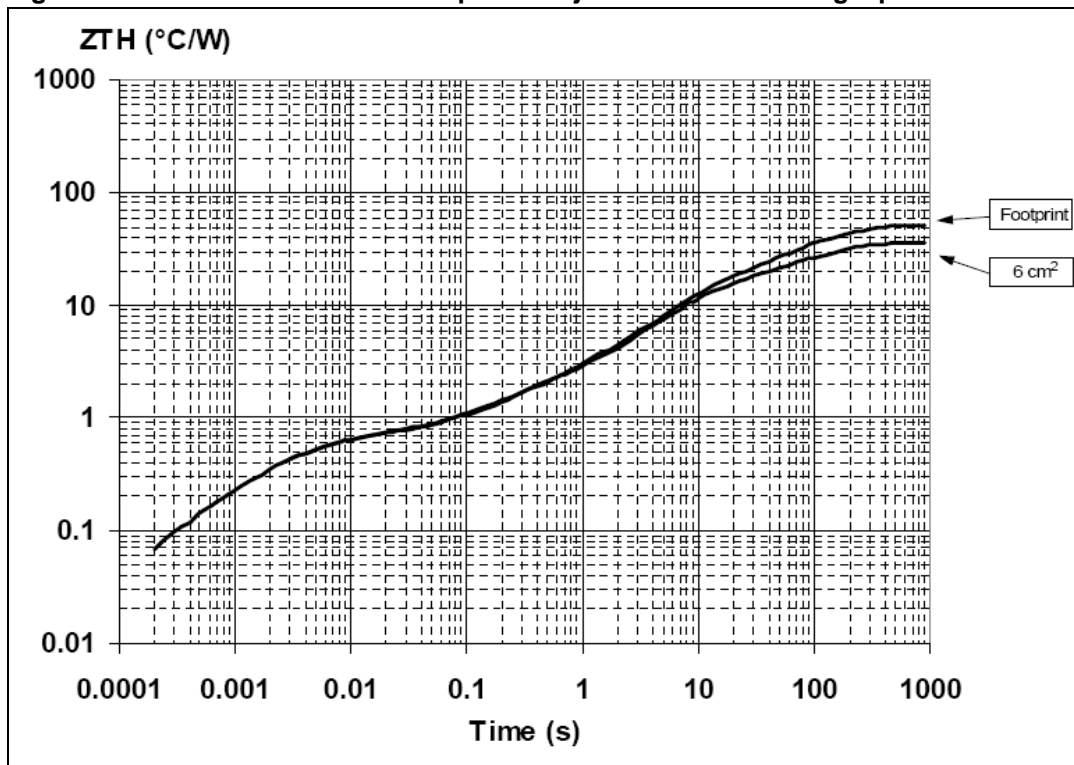
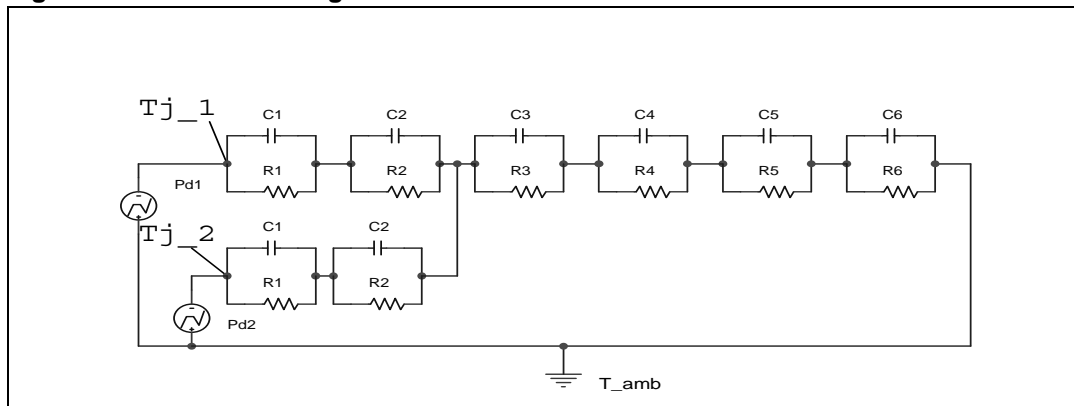


Figure 30. Thermal fitting model of a double channel HSD in PowerSO-10



Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Table 16. Thermal parameter

Area/island (cm ²)	Footprint	6
R1 (°C/W)	0.35	
R2 (°C/W)	1.8	
R3(°C/W)	1.1	
R4 (°C/W)	0.8	
R5 (°C/W)	12	
R6 (°C/W)	37	22
C1 (W.s/°C)	0.0001	
C2 (W.s/°C)	7E-04	
C3 (W.s/°C)	0.008	
C4 (W.s/°C)	0.3	
C5 (W.s/°C)	0.75	
C6 (W.s/°C)	3	5

5 Package and packing information

5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

5.2 PowerSO-10 mechanical data

Figure 31. PowerSO-10 package dimensions

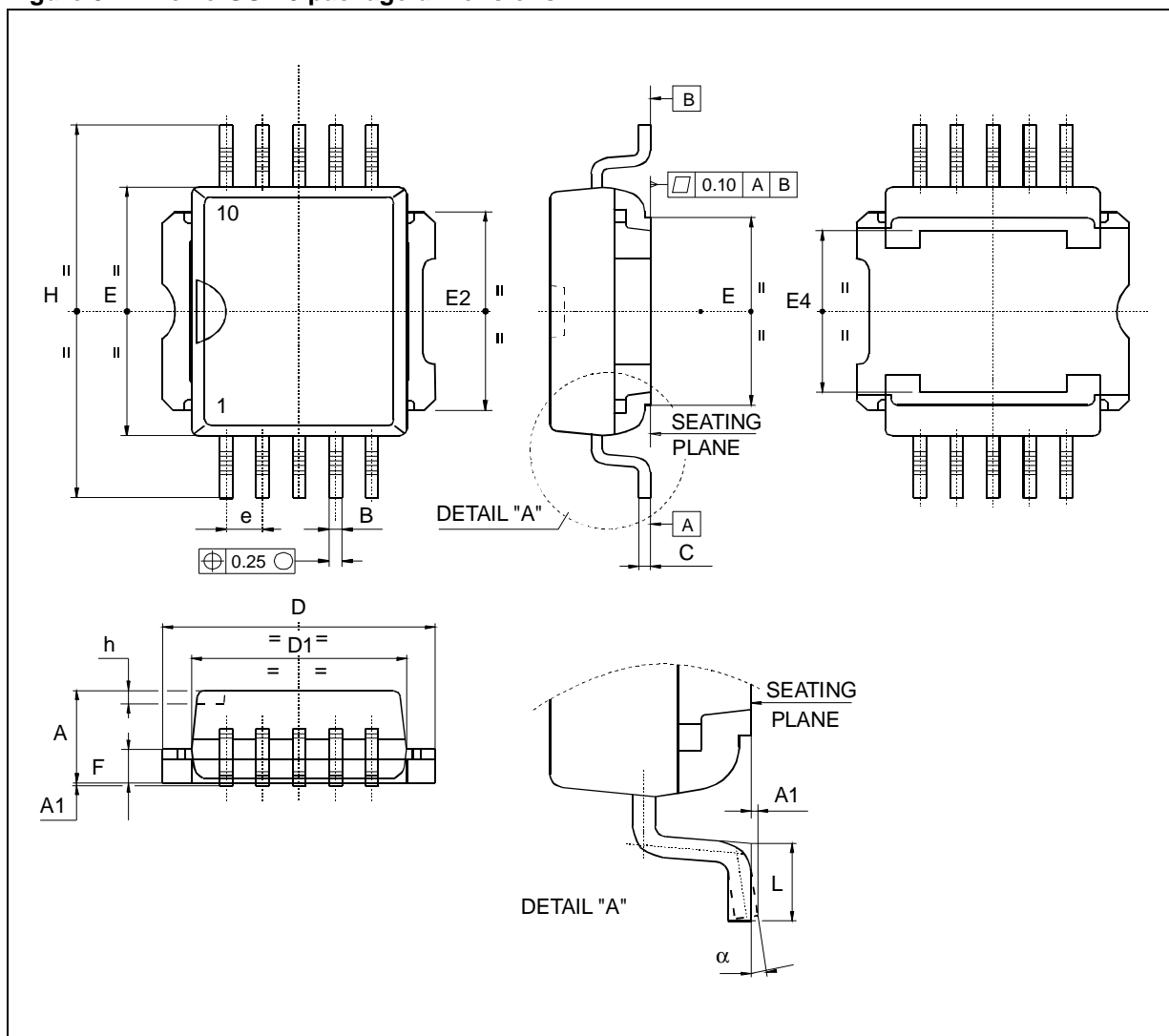


Table 17. PowerSO-10 mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	3.35		3.65
A ⁽¹⁾	3.4		3.6
A1	0.00		0.10
B	0.40		0.60
B ⁽¹⁾	0.37		0.53
C	0.35		0.55
C ⁽¹⁾	0.23		0.32
D	9.40		9.60
D1	7.40		7.60
E	9.30		9.50
E2	7.20		7.60
E2 ⁽¹⁾	7.30		7.50
E4	5.90		6.10
E4 ⁽¹⁾	5.90		6.30
e	1.27		
F	1.25		1.35
F ⁽¹⁾	1.20		1.40
H	13.80		14.40
H ⁽¹⁾	13.85		14.35
h	0.50		
L	1.20		1.80
L ⁽¹⁾	0.80		1.10
a	0°		8°
α ⁽¹⁾	2°		8°

1. Muar only POA P013P

5.3 PowerSO-10 packing information

Figure 32. PowerSO-10 suggested pad layout and tube shipment (no suffix)

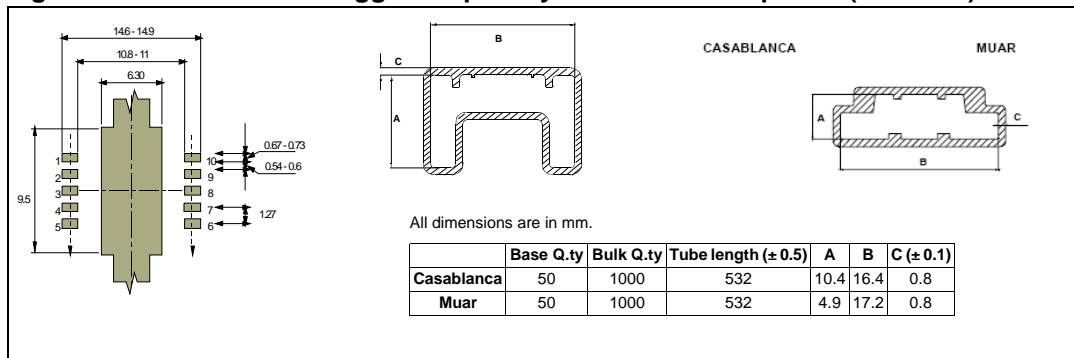
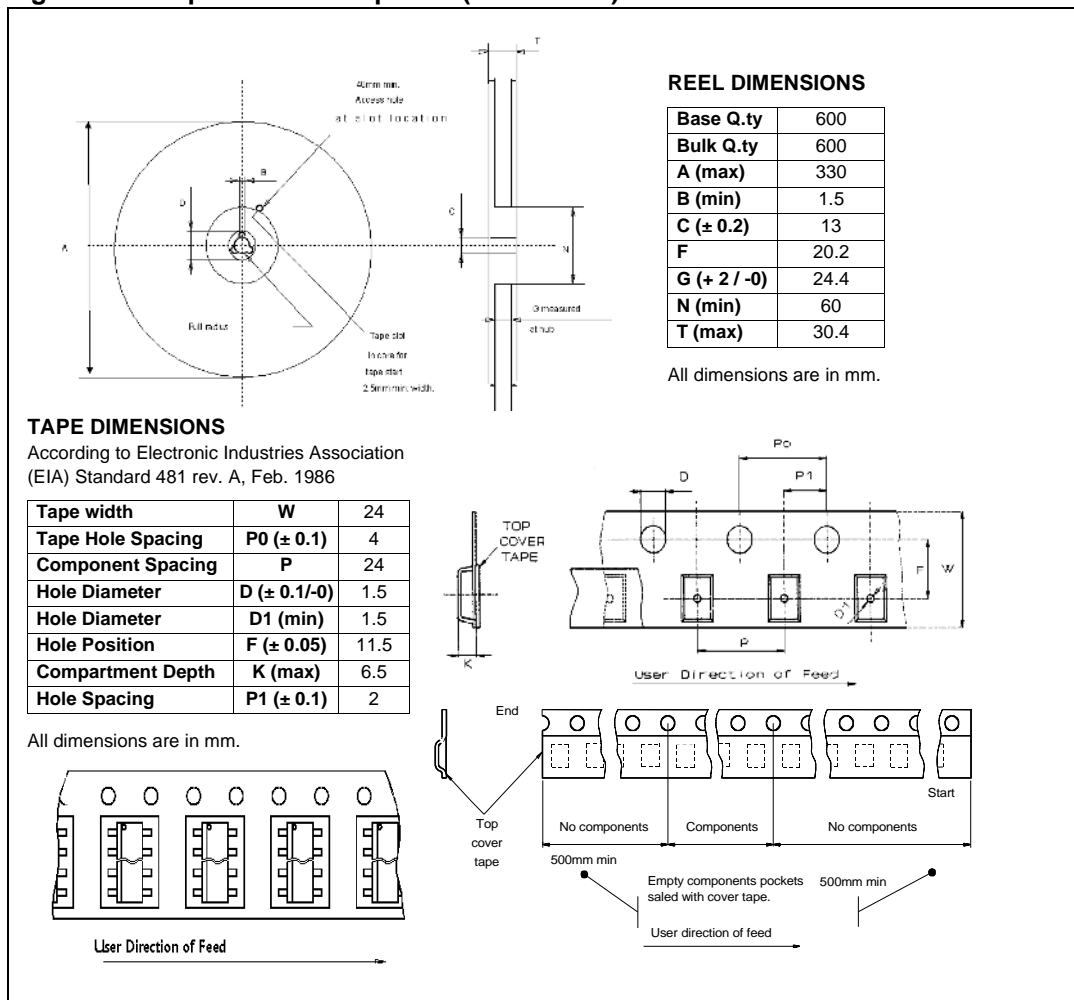


Figure 33. Tape and reel shipment (suffix “TR”)



6 Revision history

Table 18. Document revision history

Date	Revision	Changes
01-Oct-2004	1	Initial release.
25-May-2010	2	Changed document template. Reformatted entire document. Changed <i>Features</i> list.
08-Oct-2010	3	Updated following tables: – <i>Table 6: Protection</i> – <i>Table 12: Truth table</i> – <i>Table 17: PowerSO-10 mechanical data</i> Updated <i>Figure 26: Maximum turn-off current versus load inductance</i>
19-Sep-2013	4	Updated Disclaimer.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

ST PRODUCTS ARE NOT DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER'S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR "AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL" INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2013 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com