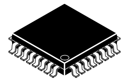


Actual Size
9mm Square

±3-A HIGH-EFFICIENCY PWM POWER DRIVER

Check for Samples: DRV593, DRV594

FEATURES

- **Operation Reduces Output Filter Size and Cost by 50% Compared to DRV591**
- **±3-A Maximum Output Current**
- **Low Supply Voltage Operation: 2.8 V to 5.5 V**
- **High Efficiency Generates Less Heat**
- **Overcurrent and Thermal Protection**
- **Fault Indicators for Overcurrent, Thermal and Undervoltage Conditions**
- **Two Selectable Switching Frequencies**
- **Internal or External Clock Sync**
- **PWM Scheme Optimized for EMI**
- **9×9 mm PowerPAD™ Quad Flatpack Package**

APPLICATIONS

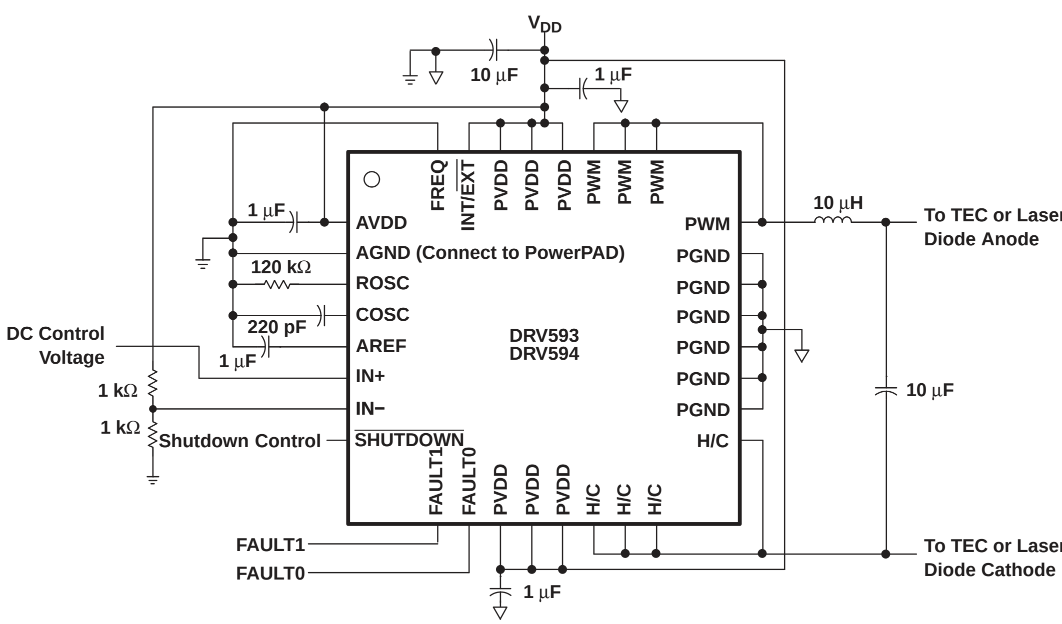
- **Thermoelectric Cooler (TEC) Driver**
- **Laser Diode Biasing**

DESCRIPTION

The DRV593 and DRV594 are high-efficiency, high-current power amplifiers ideal for driving a wide variety of thermoelectric cooler elements in systems powered from 2.8 V to 5.5 V. The operation of the device requires only one inductor and capacitor for the output filter, saving significant printed-circuit board area. Pulse-width modulation (PWM) operation and low output stage on-resistance significantly decrease power dissipation in the amplifier.

The DRV593 and DRV594 are internally protected against thermal and current overloads. Logic-level fault indicators signal when the junction temperature has reached approximately 128°C to allow for system-level shutdown before the amplifier's internal thermal shutdown circuitry activates. The fault indicators also signal when an overcurrent event has occurred. If the overcurrent circuitry is tripped, the devices automatically reset (see application information section for more details).

The PWM switching frequency may be set to 500 kHz or 100 kHz depending on system requirements. To eliminate external components, the gain is fixed at 2.3 V/V for the DRV593. For the DRV594, the gain is fixed at 14.5 V/V.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Table 1. ORDERING INFORMATION(1)

T_A	PowerPAD QUAD FLATPACK (VFP)
–40°C to 85°C	DRV593VFP(2)
	DRV594VFP(2)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com
(2) This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., DRV593VFPR or DRV594VFPR).

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		DRV593, DRV594
AVDD, PVDD	Supply voltage	–0.3 V to 5.5 V
V_I	Input voltage	–0.3 V to V_{DD} + 0.3 V
I_O (FAULT0, FAULT1)	Output current	1 mA
	Continuous total power dissipation	See Dissipation Rating Table
T_A	Operating free-air temperature range	–40°C to 85°C
T_J	Operating junction temperature range	–40°C to 150°C
T_{stg}	Storage temperature range	–65°C to 165°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
AVDD, PVDD	Supply voltage		2.8	5.5	V
V_{IH}	High-level input voltage	FREQ, INT/$\overline{\text{EXT}}$, $\overline{\text{SHUTDOWN}}$, COSC	2		V
V_{IL}	Low-level input voltage	FREQ, INT/$\overline{\text{EXT}}$, $\overline{\text{SHUTDOWN}}$, COSC		0.8	V
T_A	Operating free-air temperature		–40	85	°C

PACKAGE DISSIPATION RATINGS

PACKAGE	θ_{JA} (1) (°C/W)	θ_{JC} (°C/W)	T_A=25°C POWER RATING
VFP	29.4	1.2	4.1 W

(1) This data was taken using 2 oz trace and copper pad that is soldered directly to a JEDEC standard 4-layer 3 in × 3 in PCB.

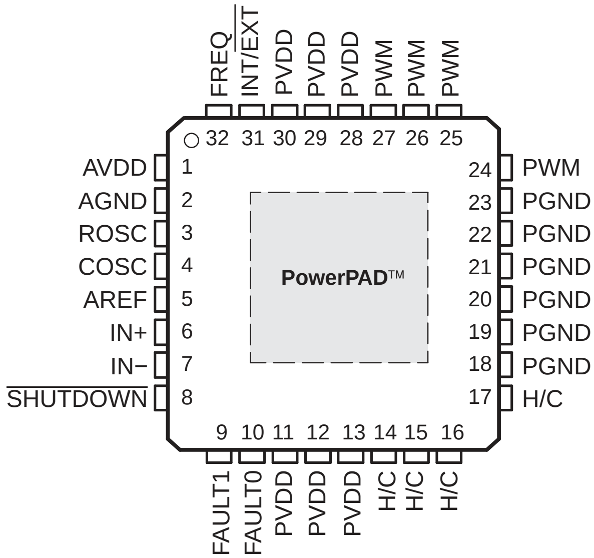
ELECTRICAL CHARACTERISTICS

over operating free-air temperature range unless otherwise noted

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\|V_{OO}\|$	Output offset voltage (measured differentially)	$V_I = V_{DD}/2$,	$I_O = 0$ A		14	100	mV
$\|I_{IH}\|$	High-level input current	$V_{DD} = 5.5$V,	$V_I = V_{DD}$			1	μA
$\|I_{IL}\|$	Low-level input current	$V_{DD} = 5.5$V,	$V_I = 0$ V			1	μA
V_n	Integrated output noise voltage	f = <1 Hz to 10 kHz			40		μV
V_{ICM}	Common-mode voltage range	$V_{DD} = 5$ V		1.2		3.8	V
		$V_{DD} = 3.3$ V		1.2		2.1	
A_v	Closed-loop voltage gain	DRV593		2.1	2.3	2.6	V/V
		DRV594		13.7	14.5	15.3	V/V
	Full power bandwidth				60		kHz
V_O	Voltage output (measured differentially)	$I_O = \pm1$ A, $r_{DS(on)} = 65$ mΩ, $V_{DD} = 5$ V			4.87		V
		$I_O = \pm3$ A, $r_{DS(on)} = 65$ mΩ, $V_{DD} = 5$ V			4.61		
$r_{DS(on)}$	Drain-source on-state resistance	$V_{DD} = 5$ V, $I_O = 4$ A, $T_A = 25°C$	High side	25	60	95	mΩ
			Low side	25	65	95	
		$V_{DD} = 3.3$ V, $I_O = 4$ A, $T_A = 25°C$	High side	25	80	140	mΩ
			Low side	25	90	140	
	Maximum continuous current output				3		A
	Status flag output pins (FAULT0, FAULT1) Fault active (open drain output)	Sinking 200 μA				0.1	V
	External clock frequency range	For 500 kHz operation		225	250	300	kHz
		For 100 kHz operation		45	50	55	
I_q	Quiescent current	$V_{DD} = 5$ V, No load or filter			4	12	mA
		$V_{DD} = 3.3$ V, No load or filter			2.5	8	
$I_{q(SD)}$	Quiescent current in shutdown mode	$V_{DD} = 5$ V, $\overline{SHUTDOWN} = 0.8$ V		0	40	80	μA
	Output resistance in shutdown	$\overline{SHUTDOWN} = 0.8$ V		1	2		kΩ
	Power-on threshold			1.7		2.8	V
	Power-off threshold			1.6		2.6	V
	Thermal trip point	FAULT0 active			128		°C
	Thermal shutdown	Power off			158		°C
Z_I	Input impedance (IN+, IN-)				100		kΩ

PIN ASSIGNMENTS

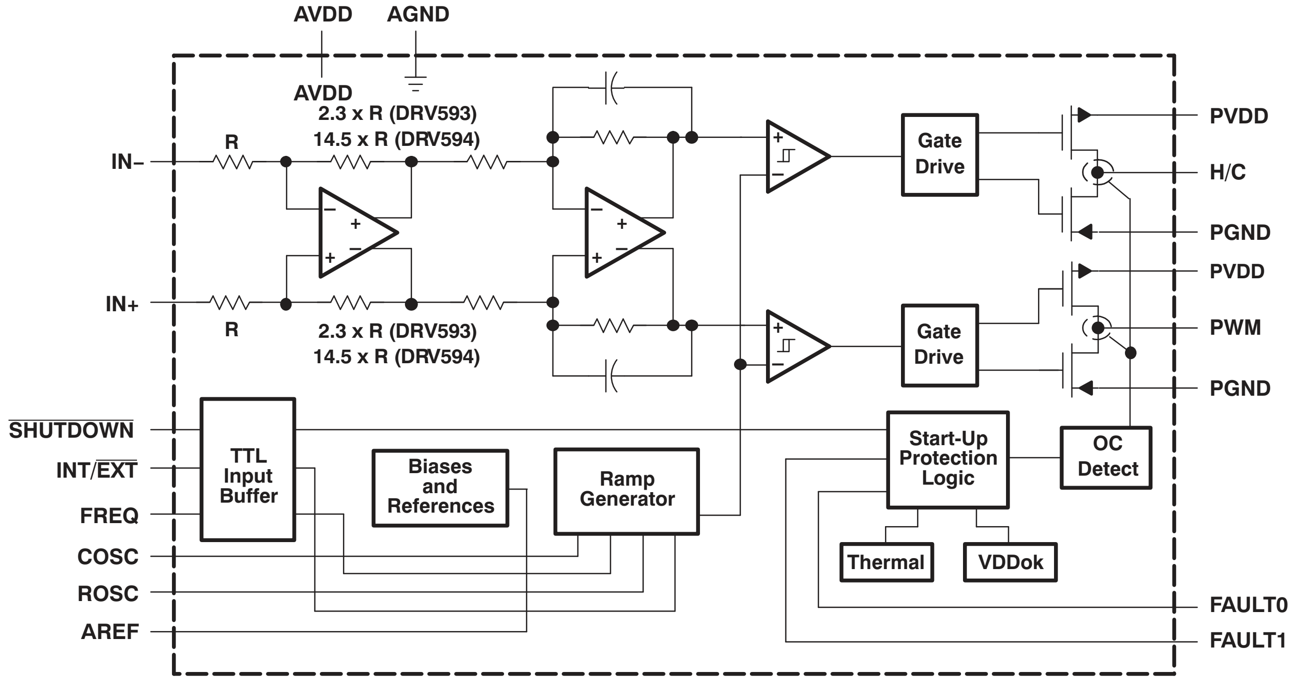
VFP PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	2		Analog ground
AREF	5	O	Connect 1 µF capacitor to ground for AREF voltage filtering
AVDD	1	I	Analog power supply
COSC	4	I	Connect capacitor to ground to set oscillation frequency (220 pF for 500 kHz, 1 nF for 100 kHz) when the internal oscillator is selected; connect clock signal when an external oscillator is used
FAULT0	10	O	Fault flag 0, low when active open drain output (see application information)
FAULT1	9	O	Fault flag 1, high when active open drain output (see application information)
FREQ	32	I	Selects 500 kHz switching frequency when a TTL logic low is applied to this terminal; selects 100 kHz switching frequency when a TTL logic high is applied
IN–	7	I	Negative differential input
IN+	6	I	Positive differential input
INT/EXT	31	I	Selects the internal oscillator when a TTL logic high is applied to this terminal; selects the use of an external oscillator when a TTL logic low is applied to this terminal
H/C	14, 15, 16, 17	O	Direction control output for heat and cool modes (4 pins)
PWM	24, 25, 26, 27	O	PWM output for voltage magnitude (4 pins)
PGND	18, 19, 20, 21, 22, 23		High-current ground (6 pins)
PVDD	11, 12, 13, 28, 29, 30	I	High-current power supply (6 pins)
ROSC	3	I	Connect 120-kΩ resistor to AGND to set oscillation frequency (either 500 kHz or 100 kHz). Not needed if an external clock is used.
SHUTDOWN	8	I	Places the amplifier in shutdown mode when a TTL logic low is applied to this terminal; places the amplifier in normal operation when a TTL logic high is applied

FUNCTIONAL BLOCK DIAGRAM



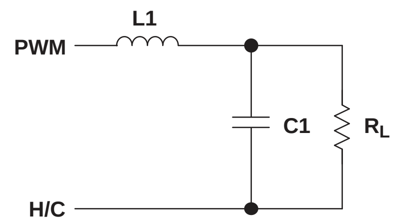
TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
	Efficiency	vs Load resistance	2, 3
$r_{DS(on)}$	Drain-source on-state resistance	vs Supply voltage	4
		vs Free-air temperature	5
		vs Free-air temperature	6
I_q	Supply current	vs Supply voltage	7
PSRR	Power supply rejection ratio	vs Frequency	8, 9
	Closed loop response		12, 13
I_O	Maximum output current	vs Output voltage	14
		vs Ambient temperature	15
V_{IO}	Input offset voltage	Common-mode input voltage	16, 17

TEST SETUP FOR GRAPHS

The LC output filter used in Figure 2, Figure 3, Figure 8, and Figure 9 is shown below.



L1 = 10 µH (part number: CDRH104R, manufacturer: Sumida)
C1 = 10 µF (part number: ECJ-4YB1C106K, manufacturer: Panasonic)

Figure 1. LC Output Filter

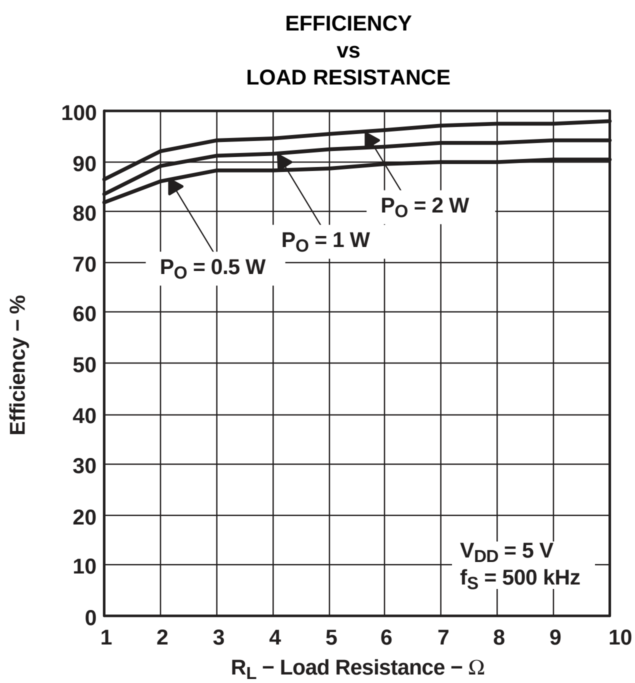


Figure 2.

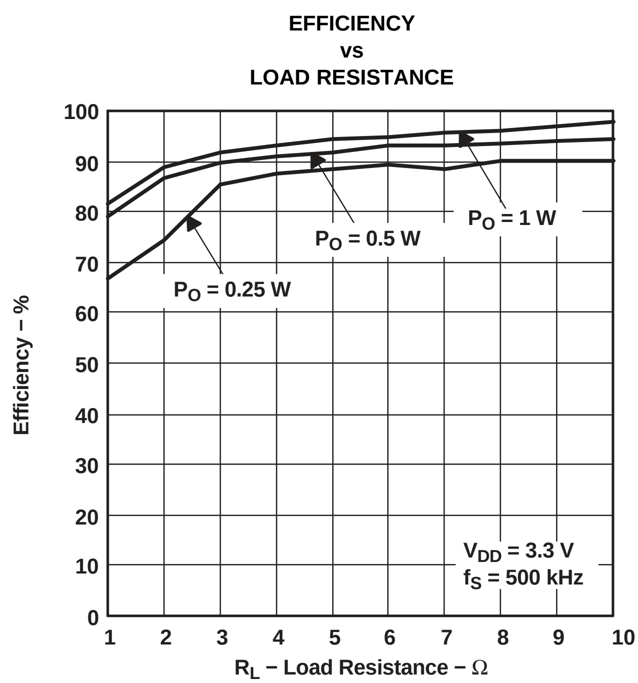


Figure 3.

DRAIN-SOURCE ON-STATE RESISTANCE
vs
SUPPLY VOLTAGE

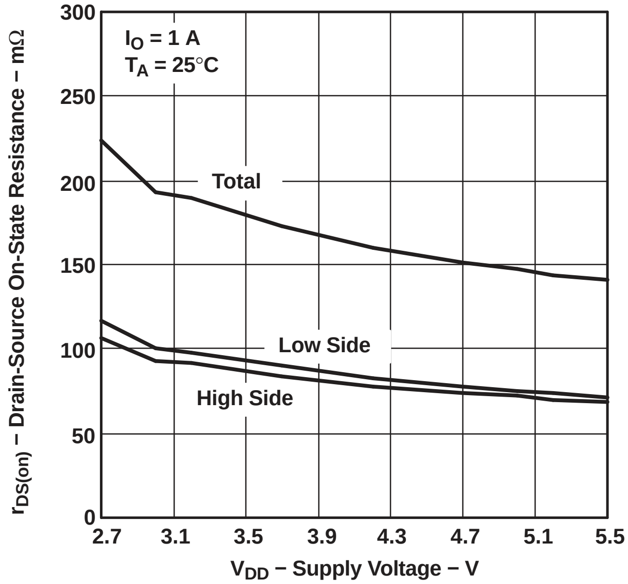


Figure 4.

DRAIN-SOURCE ON-STATE RESISTANCE
vs
FREE-AIR TEMPERATURE

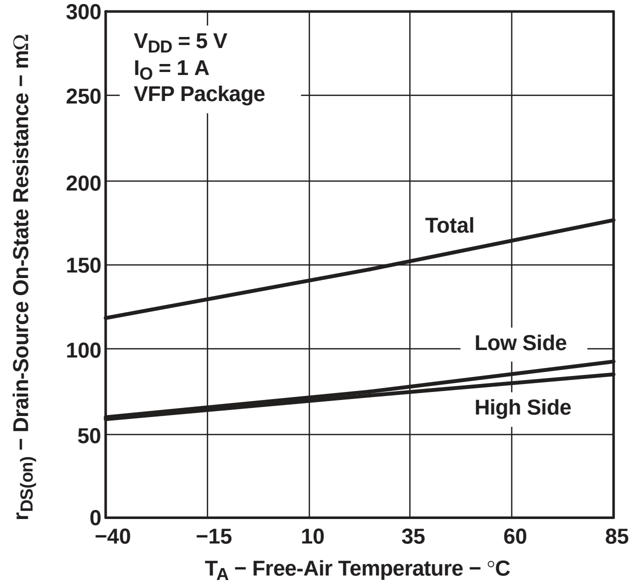


Figure 5.

DRAIN-SOURCE ON-STATE RESISTANCE
vs
FREE-AIR TEMPERATURE

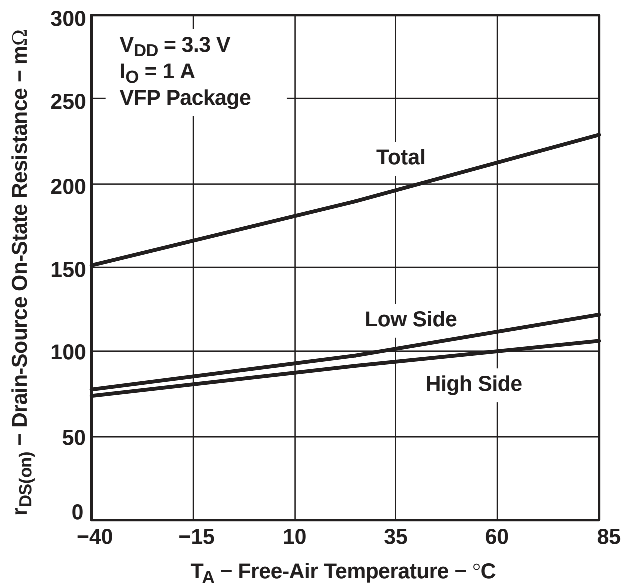


Figure 6.

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

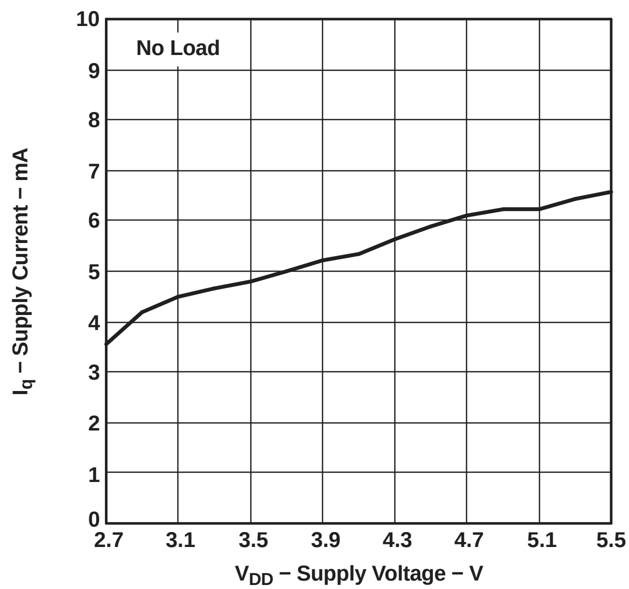


Figure 7.

POWER SUPPLY REJECTION RATIO
vs
FREQUENCY

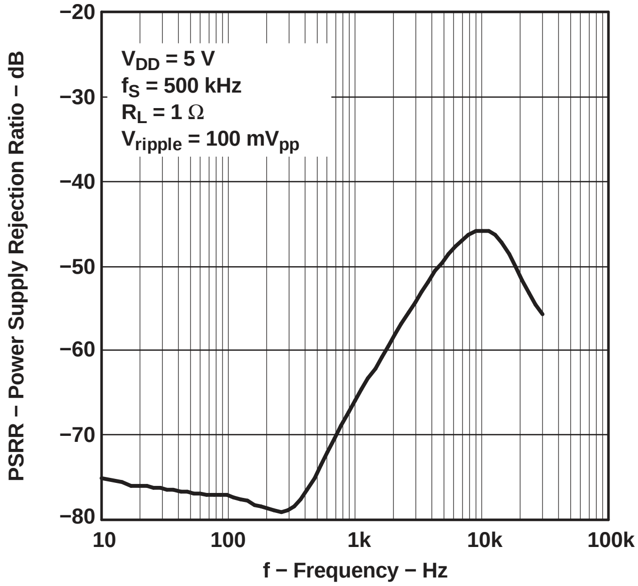


Figure 8.

POWER SUPPLY REJECTION RATIO
vs
FREQUENCY

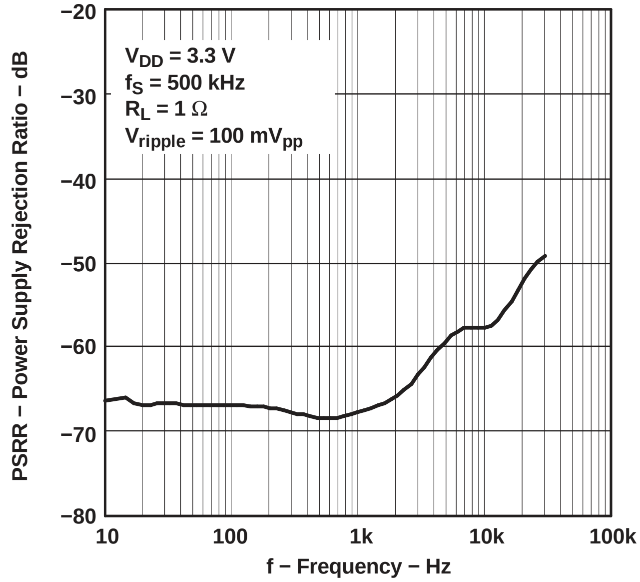


Figure 9.

DRV593
CLOSED LOOP RESPONSE

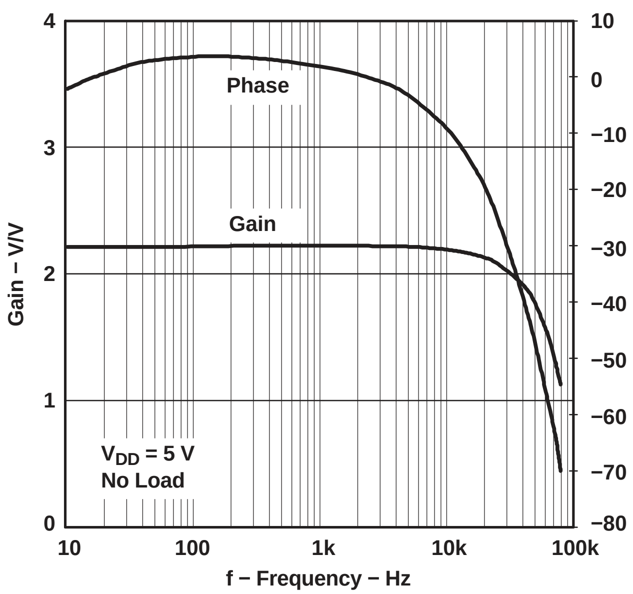


Figure 10.

DRV594
CLOSED LOOP RESPONSE

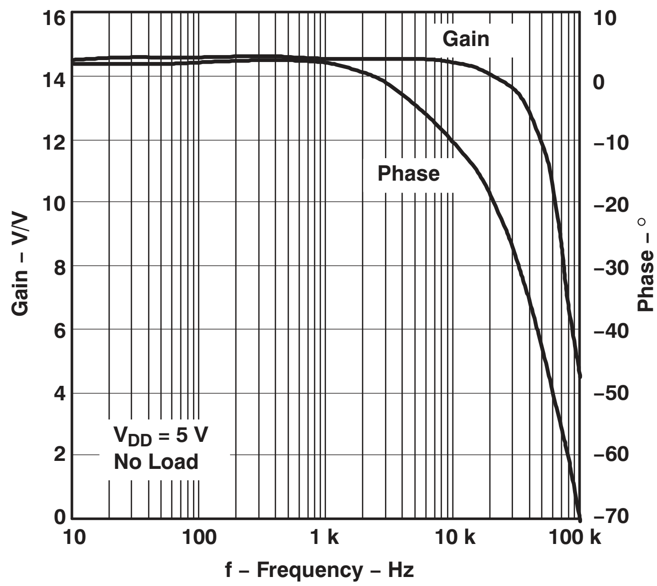


Figure 11.

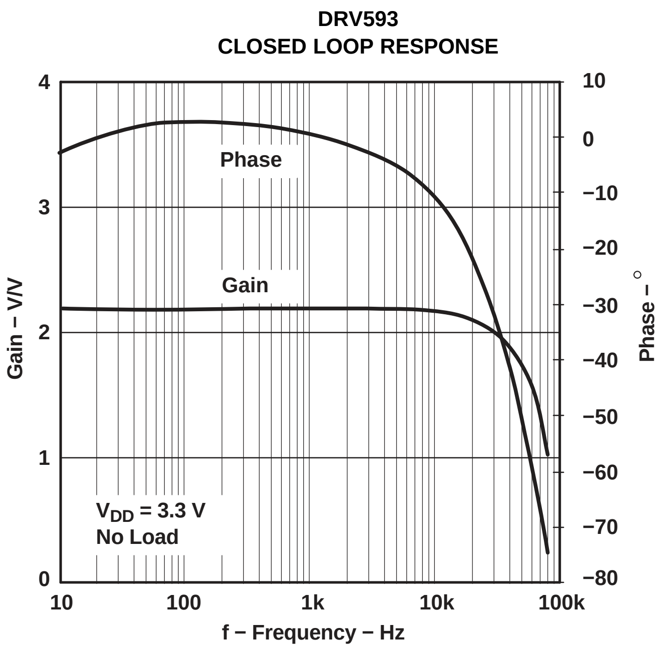


Figure 12.

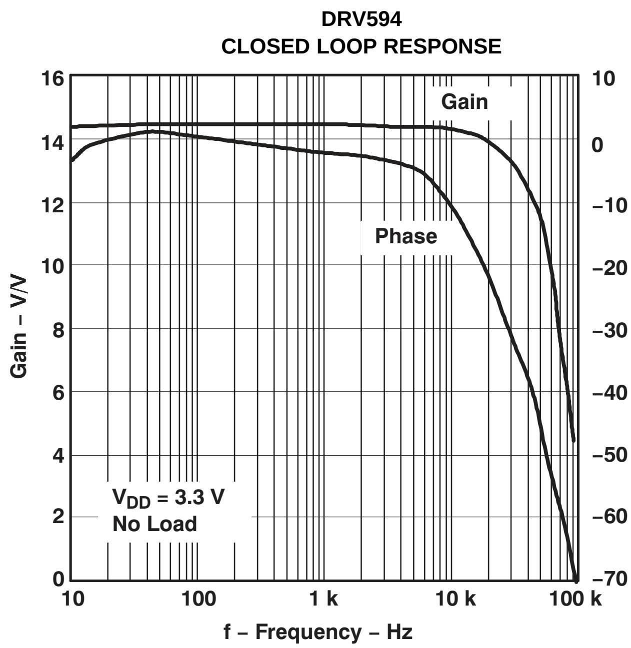


Figure 13.

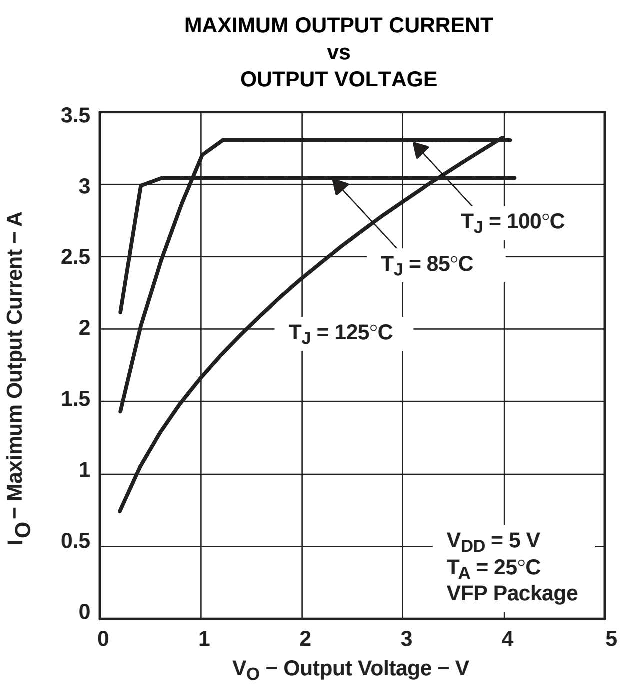


Figure 14.

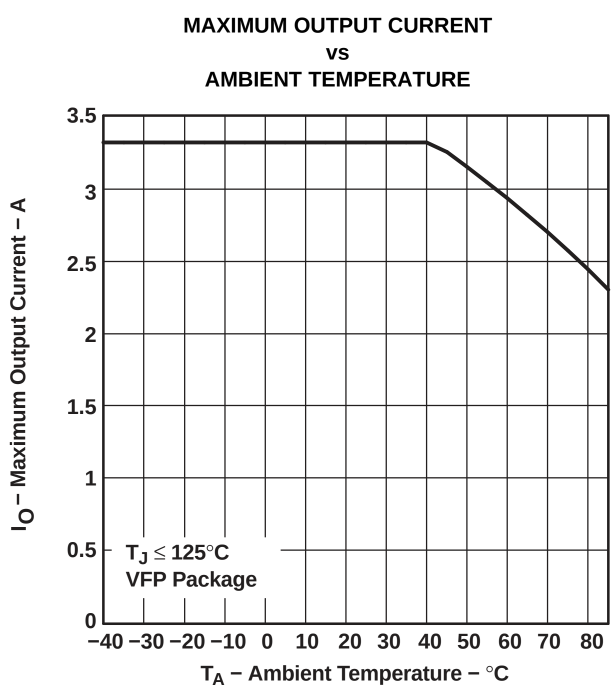


Figure 15.

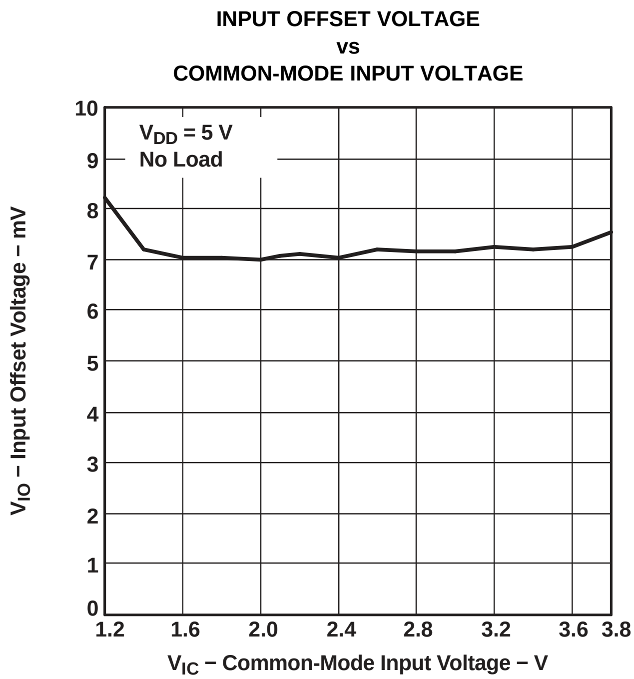


Figure 16.

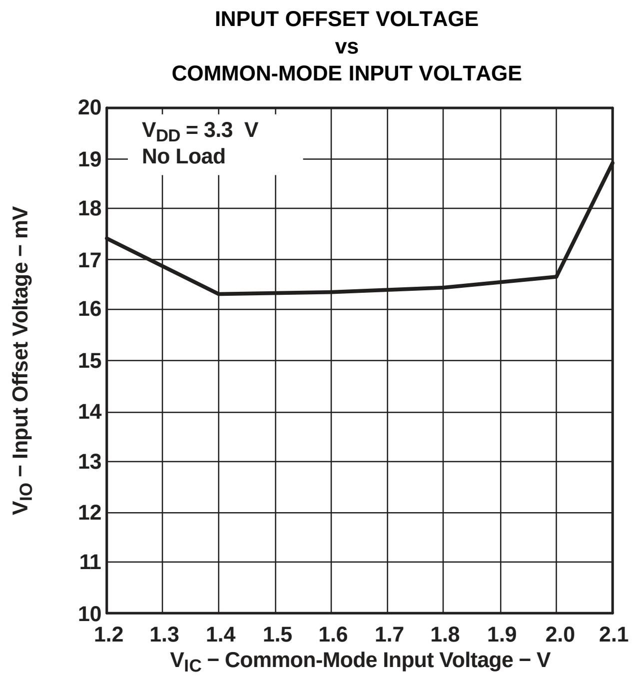


Figure 17.

APPLICATION INFORMATION

PULSE-WIDTH MODULATION SCHEME FOR DRV593 AND DRV594

The pulse-width modulation scheme implemented in the DRV593 and DRV594 eliminates one-half of the full output filter previously required for PWM drivers. The DRV593 and DRV594 require only one inductor and capacitor for the output filter. The H/C outputs determine the direction of the current and do not switch back and forth. The PWM outputs switch to produce a voltage across the load that is proportional to the input control voltage.

COOLING MODE

Figure 18 shows the DRV593 and DRV594 in cooling mode. The H/C outputs (pins 14-17) are at ground and the PWM outputs (pins 24-27) create a voltage across the load that is proportional to the input voltage.

The differential voltage across the load is determined using Equation 1 and the duty cycle using Equation 2. The differential voltage is defined as the voltage measured after the filter on the PWM output relative to the H/C output.

$$V_{Load} = D \times V_{DD} \quad (1)$$

$$D = \frac{A_V\left(V_{IN+} - V_{IN-}\right)}{V_{DD}} \quad (2)$$

where D duty cycle of the PWM signal A_v Gain of DRV593/594 (DRV593: 2.3 V/V, DRV594: 14.5 V/V) V_{IN+} Positive input terminal of the DRV593/594 V_{IN-} Negative input terminal of the DRV593/594 V_{DD} Power supply voltage

For example, a 50% duty cycle, shown in Figure 18, results in 2.5 V across the load for V_{DD} = 5 V.

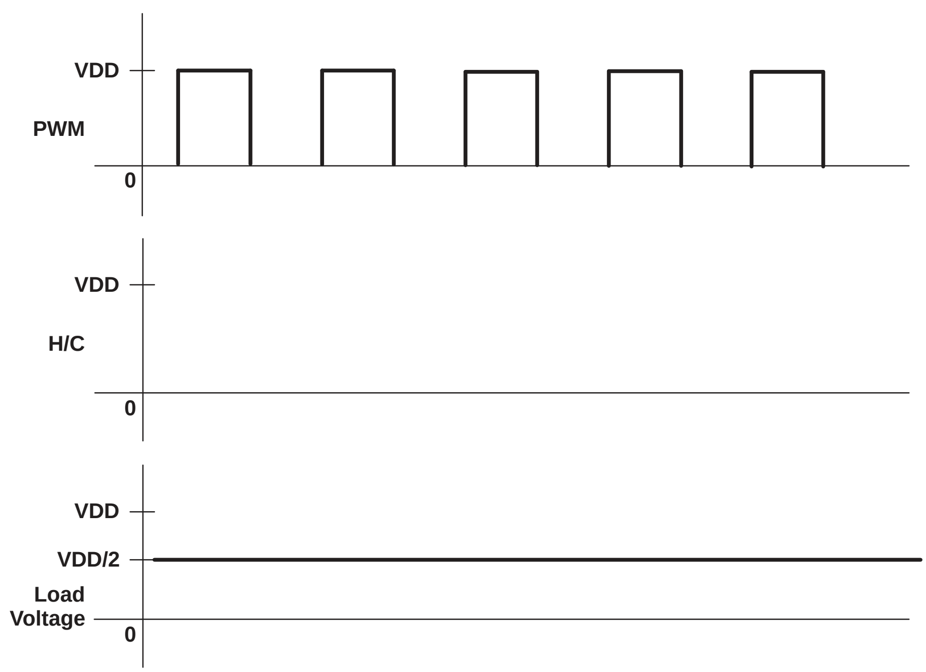


Figure 18. Cooling Mode

HEATING MODE

Figure 19 shows the DRV593 and DRV594 in heating mode. The H/C output is at VDD and the PWM output is proportional to the voltage across the load.

The differential voltage across the load is determined using Equation 3. The variables are the same as used previously for Equation 1 and Equation 2.

$$V_{Load} = -(1-D) \times V_{DD} \tag{3}$$

For example, a 50% duty cycle, shown in Figure 19, results in –2.5 V across the load for VDD = 5 V. The differential voltage across the load is defined as the voltage measured after the filter on the PWM output relative to the H/C output.

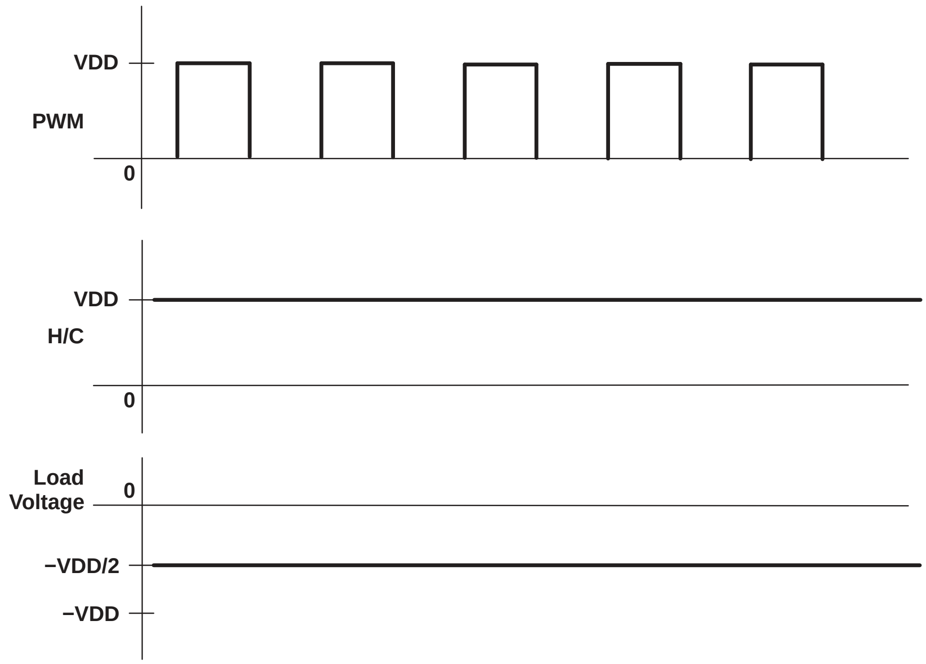


Figure 19. Heating Mode

HEAT/COOL TRANSITION

As the device transitions from cooling to heating, the duty cycle of the PWM outputs decrease to a small value and the H/C outputs remains at ground. When the device transitions to heating mode, the H/C outputs change from zero volts to VDD and the PWM outputs change to a high duty cycle. The direction of the current flow is reversed, but a low voltage is maintained across the load. The duty cycle decreases as the part is put further into heating mode to drive more current through the load. Figure 20 illustrates the transition from cooling to heating.

ZERO-CROSSING REGION

When the differential output voltage is near zero, the control logic in the DRV593 and DRV594 causes the outputs to change between heating and cooling modes. There are two possible states for the PWM and H/C outputs to obtain zero volts differentially: both outputs can be at VDD or both outputs can be at ground. Therefore, random noise causes the outputs to change between the two states when the two input voltages are equal. The outputs switch from zero to VDD, although not at a fixed frequency rate. Some of the pulses may be wider than others, but the two outputs (PWM and H/C) track each other to provide zero differential voltage. These uneven pulse widths can increase the switching noise during the zero-crossing condition.

To avoid this phenomenon, hysteresis should be implemented in the control loop to prevent the device from operating within this region. Although planning for operation during the zero-crossing is important, the normal operating points for the DRV593 and DRV594 are outside of this region. For laser temperature/wavelength regulation, the zero volts output condition is only a concern when the laser temperature or wavelength, relative to the ambient temperature, requires no heating or cooling from the TEC element.

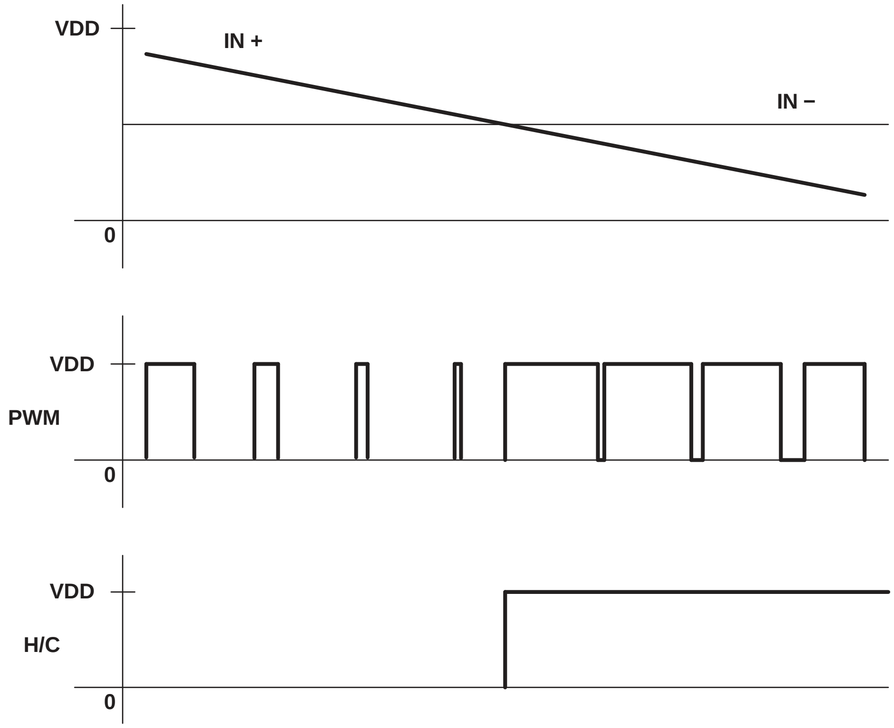


Figure 20. Transition From Cooling to Heating

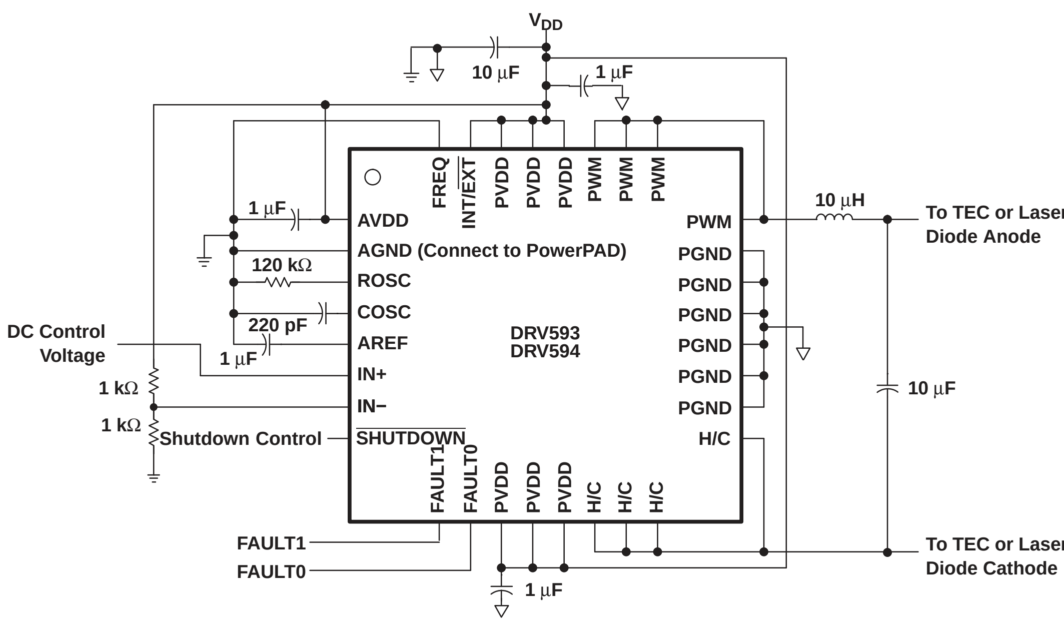


Figure 21. Typical Application Circuit

OUTPUT FILTER CONSIDERATIONS

TEC element manufacturers provide electrical specifications for maximum dc current and maximum output voltage for each particular element. The maximum ripple current, however, is typically only recommended to be less than 10% with no reference to the frequency components of the current. The maximum temperature differential across the element, which decreases as ripple current increases, may be calculated with the following equation:

$$\Delta T = \frac{1}{\left(1 + N^2\right)} \times \Delta T_{max} \quad (4)$$

where

ΔT = actual temperature differential

ΔT_{max} = maximum temperature differential (specified by manufacturer)

N = ratio of ripple current to dc current

According to this relationship, a 10% ripple current reduces the maximum temperature differential by 1%. An LC network may be used to filter the current flowing to the TEC to reduce the amount of ripple and, more importantly, protect the rest of the system from any electromagnetic interference (EMI).

FILTER COMPONENT SELECTION

The LC filter, which may be designed from two different perspectives, both described below, helps estimate the overall performance of the system. The filter should be designed for the worst-case conditions during operation, which is typically when the differential output is at 50% duty cycle. The following section serves as a starting point for the design, and any calculations should be confirmed with a prototype circuit in the lab.

Any filter should always be placed as close as possible to the DRV593 and DRV594 to reduce EMI.

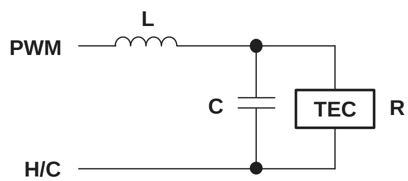


Figure 22. Output Filter

LC FILTER IN THE FREQUENCY DOMAIN

The transfer function for a second-order low-pass filter (Figure 22) is shown in Equation 5:

$$H_{LP}(j\omega) = \frac{1}{-\left(\frac{\omega}{\omega_0}\right)^2 + \frac{1}{Q}\frac{j\omega}{\omega_0} + 1}$$

$$\omega_0 = \frac{1}{\sqrt{LC}}$$

Q = quality factor

ω = DRV593 or DRV594 switching frequency (5)

For the DRV593 and DRV594, the differential output switching frequency is typically selected to be 500 kHz. The resonant frequency for the filter is typically chosen to be at least one order of magnitude lower than the switching frequency. Equation 5 may then be simplified to give the following magnitude Equation 6. These equations assume the use of the filter in Figure 22.

$$\left|H_{LP}\right|_{dB} = -40 \log\left(\frac{f_s}{f_o}\right)$$
$$f_o = \frac{1}{2\pi\sqrt{LC}}$$
$$f_s = 500 \text{ kHz (DRV593 or DRV594 switching frequency)} \tag{6}$$

If L=10 μH and C=10 μF, the cutoff frequency is 15.9 kHz, which corresponds to –60 dB of attenuation at the 500 kHz switching frequency. For VDD = 5 V, the amount of ripple voltage at the TEC element is approximately 5 mV.

The average TEC element has a resistance of 1.5 Ω, so the ripple current through the TEC is approximately 3.4 mA. At the 3-A maximum output current of the DRV593 and DRV594, this 5.4 mA corresponds to 0.11% ripple current, causing less than 0.0001% reduction of the maximum temperature differential of the TEC element (see Equation 4).

LC FILTER IN THE TIME DOMAIN

The ripple current of an inductor may be calculated using Equation 7:

$$\Delta I_L = \frac{\left(V_O - V_{TEC}\right) D T_s}{L}$$
$$D = \text{duty cycle (0.5 worst case)}$$
$$T_s = 1/f_s = 1/500 \text{ kHz} \tag{7}$$

For V_O = 5 V, V_{TEC} = 2.5 V, and L = 10 μH, the inductor ripple current is 250 mA. To calculate how much of that ripple current flows through the TEC element, however, the properties of the filter capacitor must be considered.

For relatively small capacitors (less than 22 μF) with very low equivalent series resistance (ESR, less than 10 mΩ, such as ceramic capacitors, the following Equation 8 may be used to estimate the ripple voltage on the capacitor due to the change in charge:

$$\Delta V_C = \frac{\pi^2}{2}(1-D)\left(\frac{f_o}{f_s}\right)^2 V_{TEC}$$
$$D = \text{duty cycle}$$
$$f_s = 500 \text{ kHz}$$
$$f_o = \frac{1}{2\pi\sqrt{LC}} \tag{8}$$

For L = 10 μH and C = 10 μF, the cutoff frequency, f_o, is 15.9 kHz. For worst case duty cycle of 0.5 and V_{TEC}=2.5 V, the ripple voltage on the capacitors is 6.2 mV. The ripple current may be calculated by dividing the ripple voltage by the TEC resistance of 1.5Ω, resulting in a ripple current through the TEC element of 4.1 mA. Note that this is similar to the value calculated using the frequency domain approach.

For larger capacitors (greater than 22 μF) with relatively high ESR (greater than 100 mΩ), such as electrolytic capacitors, the ESR dominates over the charging/discharging of the capacitor. The following simple Equation 9 may be used to estimate the ripple voltage:

$$\Delta V_C = \Delta I_L \times R_{ESR}$$
$$\Delta I_L = \text{inductor ripple current}$$
$$R_{ESR} = \text{filter capacitor ESR} \tag{9}$$

For a 100 µF electrolytic capacitor, an ESR of 0.1 Ω is common. If the 10 µH inductor is used, delivering 250 mA of ripple current to the capacitor (as calculated above), then the ripple voltage is 25 mV. This is over ten times that of the 10 µF ceramic capacitor, as ceramic capacitors typically have negligible ESR.

SWITCHING FREQUENCY CONFIGURATION: OSCILLATOR COMPONENTS R_{OSC} and C_{OSC} AND FREQ OPERATION

The onboard ramp generator requires an external resistor and capacitor to set the oscillation frequency. The frequency may be either 500 kHz or 100 kHz by selecting the proper capacitor value and by holding the FREQ pin either low (500 kHz) or high (100 kHz). Table 2 shows the values required and FREQ pin configuration for each switching frequency.

Table 2. Frequency Configuration Options

SWITCHING FREQUENCY	R_{OSC}	C_{OSC}	FREQ
500 kHz	120 kΩ	220 pF	LOW (GND)
100 kHz	120 kΩ	1 nF	HIGH (VDD)

For proper operation, the resistor R_{OSC} should have 1% tolerance while capacitor C_{OSC} should be a ceramic type with 10% tolerance. Both components should be grounded to AGND, which should be connected to PGND at a single point, typically where power and ground are physically connected to the printed-circuit board.

EXTERNAL CLOCKING OPERATION

To synchronize the switching to an external clock signal, pull the INT/$\overline{\text{EXT}}$ terminal low, and drive the clock signal into the COSC terminal. This clock signal must be from 10% to 90% duty cycle and meet the voltage requirements specified in the electrical specifications table. Since the DRV593 and DRV594 include an internal frequency doubler, the external clock signal must be approximately 250 kHz. Deviations from the 250 kHz clock frequency are allowed and are specified in the electrical characteristic table. The resistor connected from ROSC to ground may be omitted from the circuit in this mode of operation—the source is disconnected internally.

INPUT CONFIGURATION: DIFFERENTIAL AND SINGLE-ENDED

If a differential input is used, it should be biased around the midrail of the DRV593 or DRV594 and must not exceed the common-mode input range of the input stage (see the operating characteristics at the beginning of the data sheet).

The most common configuration employs a single-ended input. The unused input should be tied to $V_{DD}/2$, which may be simply accomplished with a resistive voltage divider. For the best performance, the resistor values chosen should be at least 100 times lower than the input resistance of the DRV593 or DRV594. This prevents the bias voltage at the unused input from shifting when the signal input is applied. A small ceramic capacitor should also be placed from the input to ground to filter noise and keep the voltage stable. An op amp configured as a buffer may also be used to set the voltage at the unused input.

FIXED INTERNAL GAIN

The differential output voltage may be calculated using Equation 10:

$$V_O = V_{OUT+} - V_{OUT-} = A_V\left(V_{IN+} - V_{IN-}\right) \quad (10)$$

A_V is the voltage gain, which is fixed internally at 2.3 V/V for DRV593 and 14.5 V/V for DRV594. The maximum and minimum ratings are provided in the electrical specification table at the beginning of the data sheet.

POWER SUPPLY DECOUPLING

To reduce the effects of high-frequency transients or spikes, a small ceramic capacitor, typically 0.1 µF to 1 µF, should be placed as close to each set of PVDD pins of the DRV593 and DRV594 as possible. For bulk decoupling, a 10 µF to 100 µF tantalum or aluminum electrolytic capacitor should be placed relatively close to the DRV593 and DRV594.

AREF CAPACITOR

The AREF terminal is the output of an internal mid-rail voltage regulator used for the onboard oscillator and ramp generator. The regulator may not be used to provide power to any additional circuitry. A 1 μF ceramic capacitor must be connected from AREF to AGND for stability (see oscillator components above for AGND connection information).

SHUTDOWN OPERATION

The DRV593 and DRV594 include a shutdown mode that disables the outputs and places the device in a low supply current state. The SHUTDOWN pin may be controlled with a TTL logic signal. When SHUTDOWN is held high, the device operates normally. When SHUTDOWN is held low, the device is placed in shutdown. The SHUTDOWN pin must not be left floating. If the shutdown feature is unused, the pin may be connected to VDD.

FAULT REPORTING

The DRV593 and DRV594 include circuitry to sense three faults:

- Overcurrent
- Undervoltage
- Overtemperature

These three fault conditions are decoded via the FAULT1 and FAULT0 terminals. Internally, these are open-drain outputs, so an external pullup resistor of 5 kΩ or greater is required.

Table 3. Fault Indicators

FAULT1	FAULT0	
0	0	Overcurrent
1	0	Undervoltage
0	1	Overtemperature
1	1	Normal operation

The overcurrent fault is reported when the output current exceeds four amps. As soon as the condition is sensed, the overcurrent fault is set and the outputs go into a high-impedance state for approximately 3 μs to 5 μs (500 kHz operation). After 3 μs to 5 μs, the outputs are re-enabled. If the overcurrent condition has ended, the fault is cleared and the device resumes normal operation. If the overcurrent condition still exists, the above sequence repeats.

The undervoltage fault is reported when the operating voltage is reduced below 2.8 V. This fault is not latched, so as soon as the power supply recovers, the fault is cleared and normal operation resumes. During the undervoltage condition, the outputs go into a high-impedance state to prevent overdissipation due to increased $r_{DS(on)}$.

The overtemperature fault is reported when the junction temperature exceeds 128°C. The device continues operating normally until the junction temperature reaches 158°C, at which point the IC is disabled to prevent permanent damage from occurring. The system's controller must reduce the power demanded from the DRV593 or DRV594 once the overtemperature flag is set, or else the device switches off when it reaches 158°C. This fault is not latched; once the junction temperature drops below 128°C, the fault is cleared, and normal operation resumes.

POWER DISSIPATION AND MAXIMUM AMBIENT TEMPERATURE

Though the DRV593 and DRV594 are much more efficient than traditional linear solutions, the power drop across the on-resistance of the output transistors does generate some heat in the package, which may be calculated as shown in Equation 11:

$$P_{DISS} = \left(I_{OUT}\right)^2 \times r_{DS(on),\ total} \quad (11)$$

For example, at the maximum output current of 3 A through a total on-resistance of 130 mΩ (at T_J = 25°C), the power dissipated in the package is 1.17 W.

Calculate the maximum ambient temperature using Equation 12:

$$T_A = T_J - \left(\theta_{JA} \times P_{DISS}\right) \tag{12}$$

PRINTED-CIRCUIT BOARD (PCB) LAYOUT CONSIDERATIONS

Since the DRV593 and DRV594 are high-current switching devices, a few guidelines for the layout of the printed-circuit board (PCB) must be considered:

1. **Grounding.** Analog ground (AGND) and power ground (PGND) must be kept separated, ideally back to where the power supply physically connects to the PCB, minimally back to the bulk decoupling capacitor (10 µF ceramic minimum). Furthermore, the PowerPAD ground connection should be made to AGND, not PGND. Ground planes are not recommended for AGND or PGND, traces should be used to route the currents. Wide traces (100 mils) should be used for PGND while narrow traces (15 mils) should be used for AGND.
2. **Power supply decoupling.** A small 0.1 µF to 1 µF ceramic capacitor should be placed as close to each set of PVDD pins as possible, connecting from PVDD to PGND. A 0.1 µF to 1 µF ceramic capacitor should also be placed close to the AVDD pin, connecting from AVDD to AGND. A bulk decoupling capacitor of at least 10 µF, preferably ceramic, should be placed close to the DRV593 or DRV594, from PVDD to PGND. If power supply lines are long, additional decoupling may be required.
3. **Power and output traces.** The power and output traces should be sized to handle the desired maximum output current. The output traces should be kept as short as possible to reduce EMI, i.e., the output filter should be placed as close to the DRV593 or DRV594 outputs as possible.
4. **PowerPAD.** The DRV593 and DRV594 in the Quad Flatpack package use TI's PowerPAD technology to enhance the thermal performance. The PowerPAD is physically connected to the substrate of the DRV593 and DRV594 silicon, which is connected to AGND. The PowerPAD ground connection should therefore be kept separate from PGND as described above. The pad underneath the AGND pin may be connected underneath the device to the PowerPAD ground connection for ease of routing. For additional information on PowerPAD PCB layout, refer to the *PowerPAD Thermally Enhanced Package* application note, (SLMA002).
5. **Thermal performance.** For proper thermal performance, the PowerPAD must be soldered down to a thermal land, as described in the *PowerPAD Thermally Enhanced Package* application note, (SLMA002). In addition, at high current levels (greater than 2 A) or high ambient temperatures (greater than 25°C), an internal plane may be used for heat sinking. The vias under the PowerPAD should make a solid connection, and the plane should not be tied to ground except through the PowerPAD connection, as described above.

Changes from Revision A (October 2002) to Revision B **Page**

- Changed Thermal trip point from 115°C to 128°C 3
- Changed Thermal shtudown point from 128°C to 158°C 3

Changes from Revision B (November 2008) to Revision C **Page**

- Changed figure cross reference from "Figure 17 and Figure 18" to "Figure 22" in the "LC FILTER......." section. 14

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV593VFP	ACTIVE	HLQFP	VFP	32	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DRV593	Samples
DRV593VFPR	ACTIVE	HLQFP	VFP	32	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DRV593	Samples
DRV594VFP	ACTIVE	HLQFP	VFP	32	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DRV594	Samples
DRV594VFPR	ACTIVE	HLQFP	VFP	32	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DRV594	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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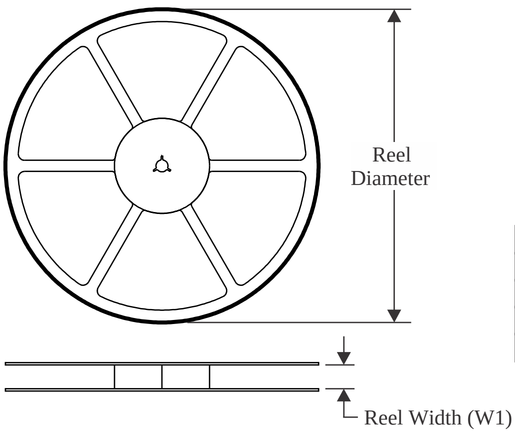
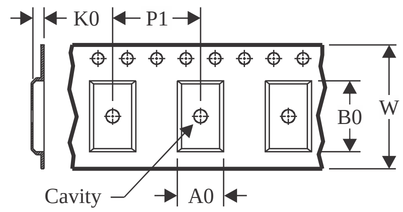
TAPE AND REEL INFORMATION

REEL DIMENSIONS

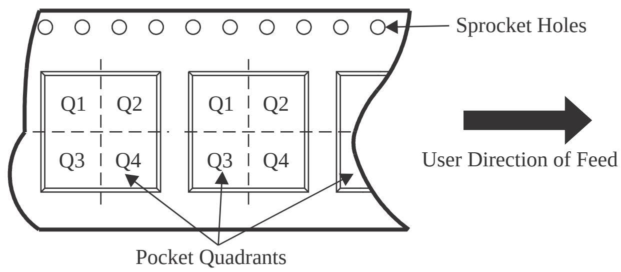


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

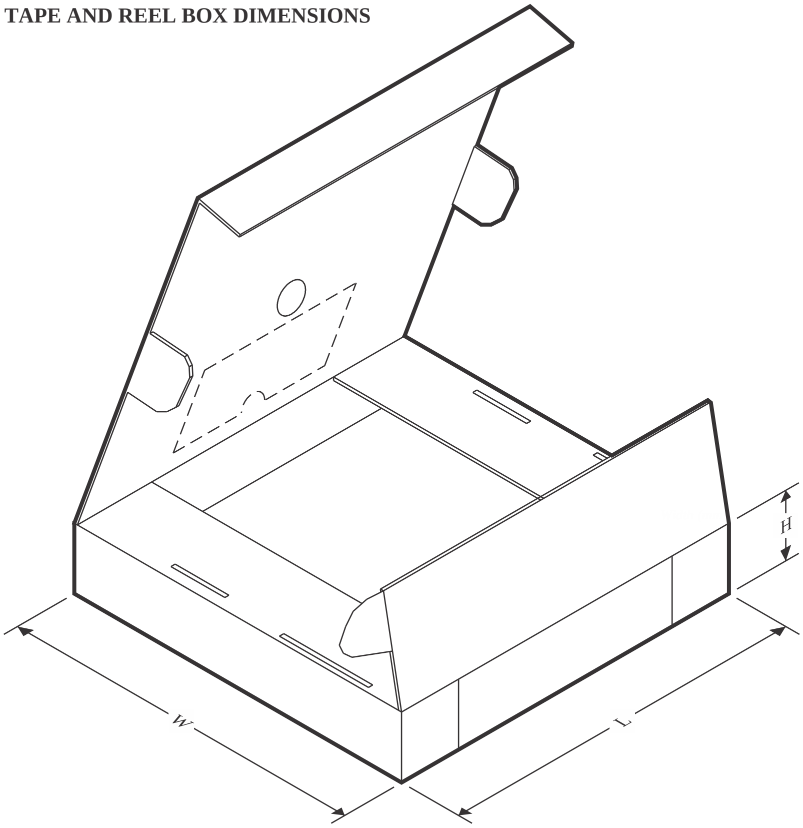
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV593VFPR	HLQFP	VFP	32	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
DRV594VFPR	HLQFP	VFP	32	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2

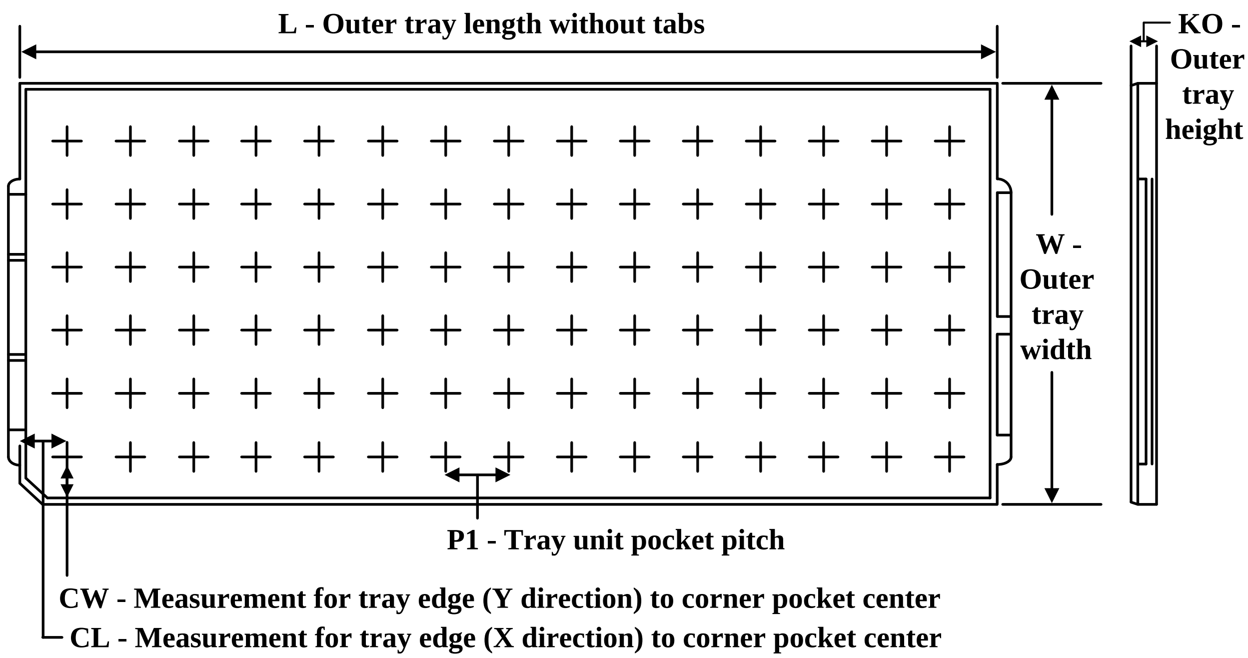
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV593VFPR	HLQFP	VFP	32	1000	350.0	350.0	43.0
DRV594VFPR	HLQFP	VFP	32	1000	350.0	350.0	43.0

TRAY



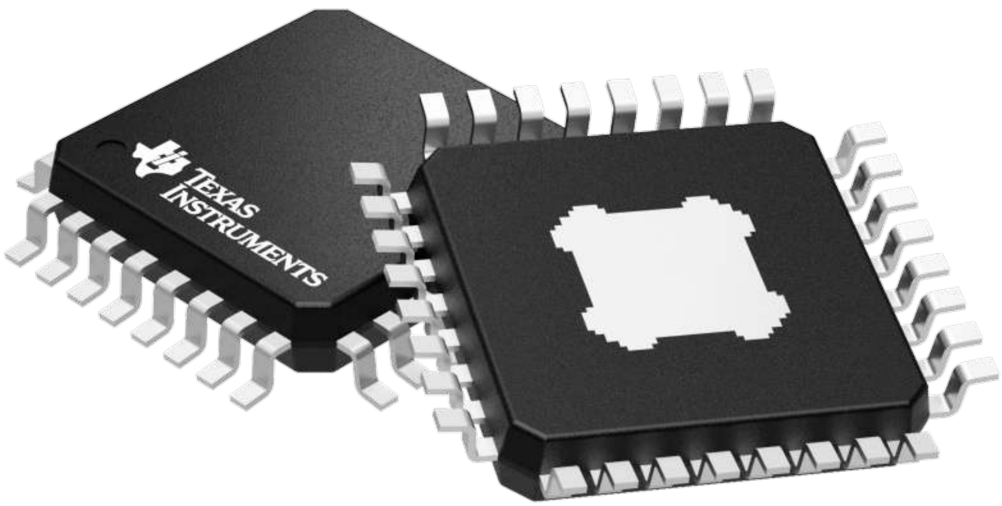
Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
DRV593VFP	VFP	HLQFP	32	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
DRV594VFP	VFP	HLQFP	32	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25

VFP 32 PowerPAD™ LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4200791/D

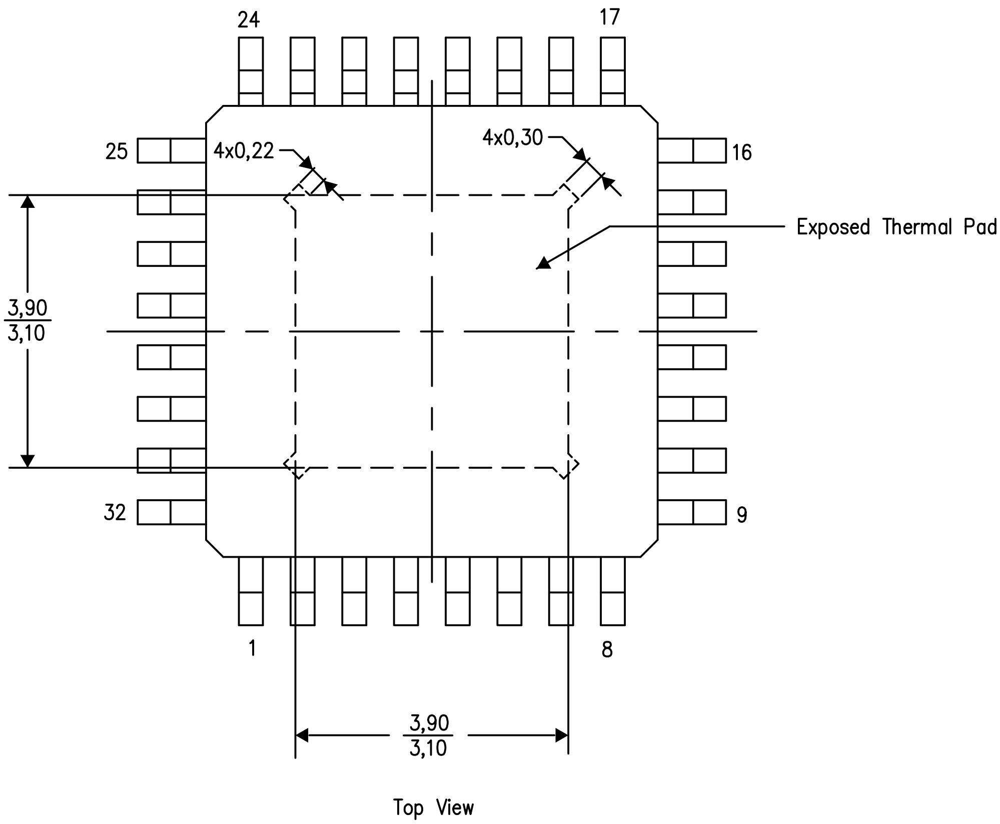
VFP (S-PQFP-G32) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

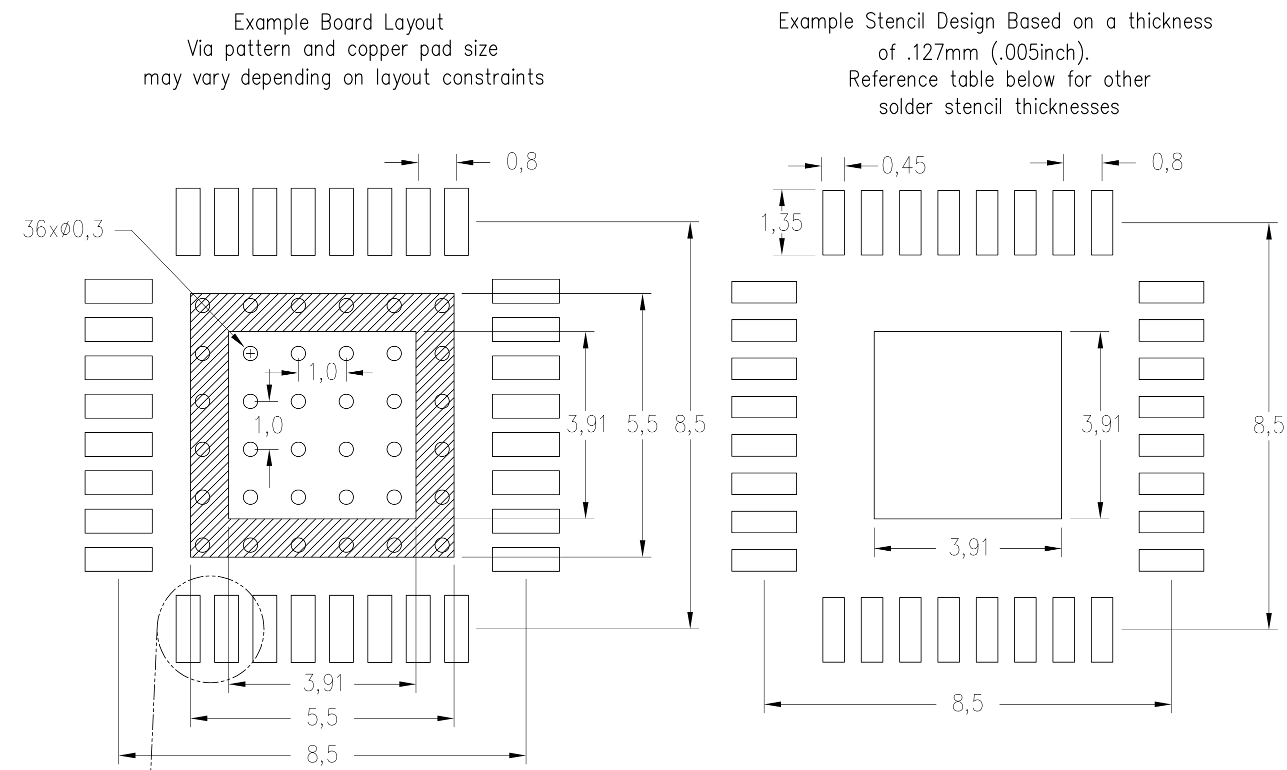


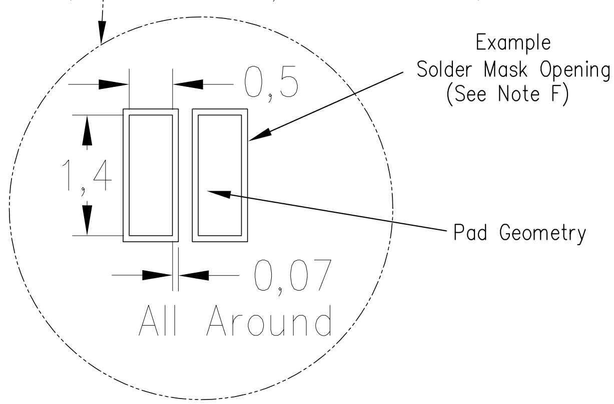
Exposed Thermal Pad Dimensions

4206318-2/E 06/13

NOTE: All linear dimensions are in millimeters

VFP (S–PQFP–G32) PowerPAD™





CENTER POWER PAD SOLDER STENCIL OPENING		
STENCIL THICKNESS	X	Y
0.1mm	4.20	4.20
0.127mm	3.91	3.91
0.152mm	3.70	3.70
0.178mm	3.40	3.40

4209361–3/A 03/08

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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