A comprehensive methodology to qualify the reliability of GaN products

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TI is designing a comprehensive quality program based on GaN fundamentals and application-relevant testing to provide reliable GaN solutions.

The material properties of gallium-nitride (GaN) enable an exciting and disruptive new power switch – the power GaN high-electron mobility transistor (HEMT). This HEMT is a field-effect transistor (FET) with much lower on-resistance. It can switch faster than an equivalently-sized silicon power transistor. These benefits are making power conversion more energy and space efficient. GaN can be grown on silicon substrates, which allows the use of silicon manufacturing capability and lower cost. As with new technologies, however, reliability needs to be proven. GaN device qualification is the subject of this whitepaper.

Introduction

The industry takes the reliability of silicon power transistors for granted due to over thirty years of experience and continuous improvement. This longstanding experience has resulted in a mature qualification methodology, whereby reliability and quality are certified by running standardized tests. These tests originated from detailed work on the understanding of failure modes, their activation energies and acceleration factors, and the development of a statistical and mathematical framework to extrapolate lifetimes, failure rates and defectivity. This qualification methodology has been proven out now that several generations of silicon parts have been run for their true lifetimes under actual-use conditions.

GaN transistors, however, are a more recent development. RF GaN HEMTs on more expensive silicon carbide substrates have become widely used in wireless base stations with proven reliability [1]. The power GaN HEMT, although based on similar fundamentals, has added features to enable higher voltage handling. It is grown on a silicon substrate and uses silicon fabrication-compatible

materials to lower cost. Additionally, it needs to be an enhancement-mode (e-mode), or normally-off device, for fail-safe reasons.

There are three leading architectures: 1) depletion-mode (d-mode) insulated gate GaN HEMT cascoded with an e-mode Si FET; 2) e-mode insulated gate GaN HEMT; and 3) p-doped, e-mode junction-gate GaN HEMT. These have different failure modes from each other, and from silicon FETs, which brings up the question of how to qualify them. The standard silicon-based qualification recipe is a worthy quality and reliability milestone, but it is not clear what it means for GaN transistors in terms of device lifetime, failure rates and application-relevance.

Texas Instruments is an industry leader in semiconductor technology with longtime experience in bringing reliable semiconductor products to market, including non-silicon technologies like ferroelectric random access memory (FRAM). We are well-suited to bring reliable GaN products to market through GaN-relevant qualification methodology and application-relevant testing.

Standard qualification methodology

There are two standards bodies whose qualification methodologies are in widespread use for qualifying silicon power devices: Joint Electron Device Engineering Council (JEDEC); and Automotive Electronics Council (AEC) [2, 3, 4, 5]. These standards specify many tests which may be classified into three categories: electrostatic discharge (ESD), package, and device.

Electrostatic discharge requirements are imposed by handling, so the ESD qualification is not expected to change. Packaging tests are expected to be similar to those done for silicon, with failures being driven to root cause to highlight unexpected failure mechanisms. The similarity arises because the issues of package stress, bonding surface interactions, and so on, are common since the back-end processing used historically with silicon is also used with GaN. The device category, however, is new and consequently of particular importance. The following paragraphs examine the standard silicon qualification methodology and describe how it may be adapted to GaN.

For silicon qualification the standard stress is run for 1000h, at a junction temperature of at least 125ºC. An activation energy of 0.7 eV is assumed, giving a temperature acceleration factor of 78.6 [2]. This makes a 1000h stress at a junction temperature (Tj) of 125ºC equivalent to nine years of use at Tj=55ºC. Devices are qualified at their maximum operating voltage. For discrete power FETs, this is usually chosen to be 80 percent of the minimum breakdown voltage specification. This means that there is no voltage acceleration built into the qualification test condition and acceleration is achieved by temperature alone. This has important implications for power devices, since Tj is higher than 55ºC, typically above 75ºC.

The standard also specifies that three lots, each with 77 parts, be stressed with no failures. A criteria of zero failures out of 231 means that the lot-tolerant percent defective (LTPD) value is one [2]. This means that you can state with 90 percent confidence that less than one percent of the parts in a lot are defective under the extrapolated stress condition. In other words, nine years of use at Tj=55ºC, biased at the maximum operating voltage. The initial maximum failure in time (FIT) rate of about 50 FITs at Tj=55ºC is also established from the result of zero fails out of 231 units using the activation energy of 0.7 eV [6].

There is a dynamic test in addition to the static tests, however. It is very loosely defined as "the devices may be operated in a dynamic operating mode" [3]. It is left to the manufacturer to define the testing. The absence of prescribed testing is due to the difficulty of specifying a test that corresponds to the wide range of ever-evolving applications and technology. A prescribed stress test may not correlate appropriately to the actual-use environment and may either produce false failures or fail to accelerate valid failure mechanisms [7].

For silicon FETs, credibility in the qualification methodology has been established by many years of actual usage. In contrast for new technologies like GaN, it falls to the device manufacturer to establish that their dynamic testing is predictive of actual use. Therefore, it is important to develop application-relevant stress testing where reliability can be validated under actual-use conditions.

Finally, there is concern that GaN is not avalanche robust. That is to say, devices will get damaged if driven into breakdown. This issue needs to be addressed, particularly for high-voltage applications like power factor correction (PFC) circuits where devices are subject to possible overvoltage events, for example, from lightning spikes on power lines.

Adaptation of standard qualification methodology

Both JEDEC and AEC standards are based on sound fundamentals, but lag technology introduction. While passing silicon qualification is a worthy milestone, the customer needs a product that will last for the desired lifetime, such as 10 years at a low-failure rate under actual-use conditions. As a result, companies introducing new technologies, for example, FRAM, scaled CMOS, GaN and so on, need to understand the fundamentals from which the standards arose.

In the JEDEC qualification methodology, the main accelerant is temperature. The acceleration factor (AF) is calculated per eq. (1), where E_A is the activation energy, and k is the Boltzmann constant.

$$AF = \exp\left\{ \left(\frac{E_A}{k} \right) \left[\left(\frac{1}{T_{USE}} \right) - \left(\frac{1}{T_{STRESS}} \right) \right] \right\} \tag{1}$$

If eq (1) is used with a stress temperature of Tj=125°C, a use temperature of Tj=55°C, and an activation energy of about 0.7 eV, it gives an acceleration factor of 78.6. This is why a 1000h stress at Tj=125°C is roughly equivalent to 10 years of use at Tj=55°C. Published literature shows activation energies for GaN [8] varying between 1.05 to 2.5 eV. The wide range of values is indicative of variation in devices, processes and materials at different laboratories and companies around the world. This range can give a wide variation in acceleration factors, say from 687 at E_A=1.05 eV to over 5 million at E_A=2.5 eV. Therefore, it is necessary to determine the activation energy on a process and device architecture representative of the final product.

It is also important to consider the junction temperature under actual operation. Due to its wide bandgap, GaN can operate at higher temperatures than silicon. This is important for power electronics products. In qualifying devices, several factors need to be considered. Table 1 contrasts a standard 1000h silicon qualification stress at 125°C with several other scenarios. It shows that if a junction operating temperature (Tj) of 105°C is desired, the nonaccelerated time decreases from about nine years to 0.3 years for the assumed activation energy of 0.7 eV. The time may be increased to 1.1 years by increasing the stress temperature to 150°C, which is a practical limit for a standard package. In this case, the stress test does not meet the field-equivalent lifetime, or resolve the maximum FIT rate condition of about 50 FITs. It does, however, serve as a reliability and quality milestone

A 1000h stress representing 10 years of use needs an acceleration factor of 87.6 and is achieved for an activation energy of 1.37. Lower activation energy, for example, a low value of 1.05 eV from ref [8] will need either voltage acceleration of 2.84 times or duration-extension from about six to 17 weeks. Excessive voltage acceleration can cause non-representative failure modes, and the duration extension lengthens the new product development cycle. Depending upon the failure modes and the available acceleration in package, qualification tests representing the required field-equivalent lifetime may not be possible. The lifetime requirement would be assured by wafer-level reliability testing [2] and validated by conducting extended-duration stress testing of packaged parts.

	Material	Silicon	Silicon	Silicon	E_A=1.05 eV	E_A=1.05 eV	E_A=1.37 eV
Scenario	Junction operating T (C)	55	105	105	105	105	105
	Voltage acceleration	No	No	No	Yes	No	No
	Stress time (h)	1000	1000	1000	1000	2846	1000
Inputs	Burn-in temperature (C)	125	125	150	150	150	150
	Activation energy (eV)	0.7	0.7	0.7	1.05	1.05	1.37
	Fails/sample size	0/231	0/231	0/231	0/231	0/231	0/231
	Voltage acceleration	1	1	1	2.84	1	1
Outputs	Non-accelerated time (yrs)	8.9	0.3	1.1	10.0	10.0	10.0
	Maximum FIT rate	50.8	1345.0	402.6	45.2	45.1	45.1
	The FIT rate calculation is to a confidence level of 60%						

Table 1: The effect of different stress parameters on reliability and quality extrapolations.

It is important to base the failure criteria upon the specific failure modes of GaN. A particular failure is that of dynamic Rds-on increase, also known as current-collapse. This is caused by negative charge trapping in both the buffer and topside layers [9,10]. Charge can be trapped when high-voltage is applied, and may not dissipate instantaneously when the device is turned on.

The trapped negative charge repels electrons from the channel layer, and Rds-on increases because the number of electrons in the channel layer is reduced (**Figure 1**). Subsequently, Rds-on recovers as the trapped charge dissipates. This effect decreases efficiency and can cause the device to excessively self-heat and fail prematurely.
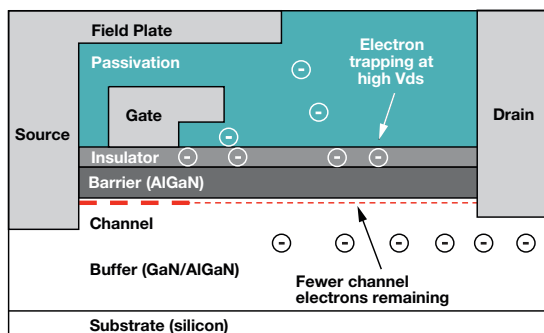
Figure 1: Schematic cross-section of a GaN device shows how trapped electrons can increase Rds-on by reducing the number of electrons in the channel layer.

Furthermore, the trap density can increase as the device ages, making the dynamic Rds-on effect worse. We have specialized hardware to monitor dynamic Rds-on during stress testing, which allows us to release product without this issue.

Application-relevant testing

Although the DC tests are relatively straightforward to carry out for a large quantity of parts, they may not predict whether GaN will have 10 years of lifetime in the actual application. Hard-switching stress is different from a DC stress. Hard-switched power converters have inductive switching transitions, during which the device is simultaneously subjected to high currents and voltages. The turn-on transition is the most stressful because the FET channel needs to sink the full inductor current before the drain voltage, Vds, drops, as well as discharge any reverse recovery from other devices at that node. It also needs to carry the extra current from discharging the device output and switched-node capacitances as Vds drops. Turn-off is less stressful because the FET channel is turned off when Vds is low, and the inductor current goes towards charging the respective capacitances.

Device stress is illustrated using a boost converter with the topology shown in **Figure 2**. Simulation results of the hard-switching turn-on transition on the primary switch (FET1) are shown in **Figure 3**. The input voltage is 200V and the inductor current is 5A (load current is about 2.5A). In this case, when FET1 is off, its drain voltage is clamped at about 400V due to the conduction of the clamp FET (FET2). As a result, when FET1 turns on, it needs to sink the full inductor current before Vds starts dropping (region A).
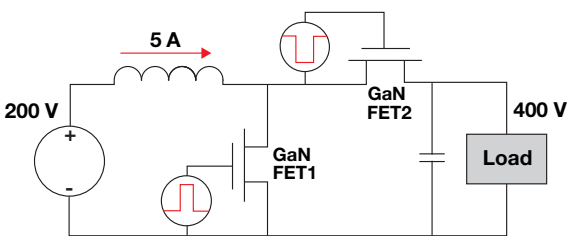
Figure 2: A simple boost converter topology.
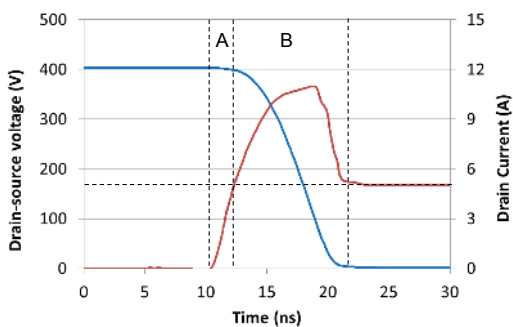
Figure 3: Turn-on transition for a hard-switched transition.

As the drain voltage drops (region B), the FET needs to discharge the capacitance at the switched node. This arises from the clamp FET, the board trace and other connected components. There is no reverse recovery current from this clamp, since a GaN FET is used. The V-I locus (**Figure 4**) shows considerable drain current at high Vds. In this case, it is about 6A above the value of the inductor current. The actual FET channel current is higher, since the drain capacitance of the FET discharges through the channel. For example, 50 pF of drain capacitance with a 60 V/ns slew rate adds another 3A.
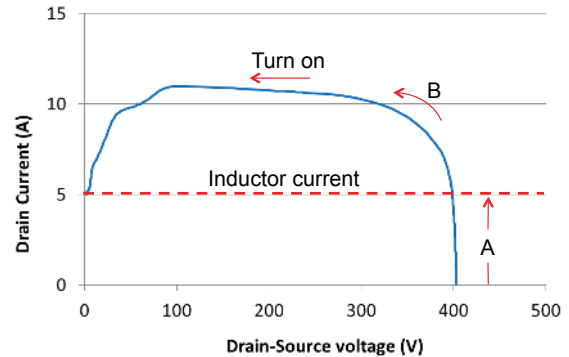
Figure 4: V-I locus of an inductive switching transition shows considerable current flow at high drain bias. The discharge of the FET drain capacitance adds additional channel current, for example, 50 pF at 60 V/ns adds 3A.

During hard-switching, the substantial FET channel current flow at high Vds results in significant hot-carrier generation, for which the device needs to be robust. Further still, large device arrays can experience non-uniform switching, which could crowd the device current into the portion of the array that turns on first and exceed the local rating. High dv/dt switching also can introduce capacitive current into unwanted regions of the device, such as terminations. Reliability testing needs to be done, especially to ensure that devices are robust for hard-switching applications, and that the reliable switching safe operating area (SOA) bounds the customer-use conditions for the device.

TI has developed an inductive switching cell based upon a simple boost converter in order to validate hard-switching robustness (**Figure 5**). The selection is based upon the JEDEC recommendation [7] stating, "Dependent on the failure modes and mechanisms of concern, a test vehicle may be preferable since the actual product complexity may mask intrinsic failure mechanisms".
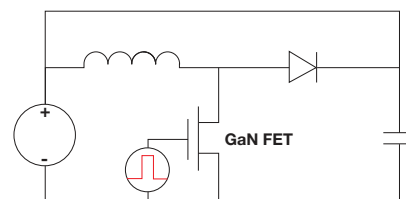
Figure 5: Test vehicle for inductive switching application test.

When the GaN FET is off, the inductor current is recirculated to the input through a diode, which eliminates the need for a load resistor and allows energy-saving. The cell is run with the inductor in continuous-current-mode. Since the objective is the switching transition, energy may be saved by using short duty cycles. The cell has the ability to vary the applied voltage, current, frequency and temperature applied to the device. Additional drain current (**Figure 4**) is provided by the diode capacitance.

Extra capacitance can be added as needed. This cell also has hardware to measure the dynamic on-resistance (dRds-on) of the device one microsecond after the switching transition. This in-situ monitoring capability is needed since dRds-on can get worse with stress, resulting in higher conduction loss and lower efficiency. In a product, the increasing dRds-on will cause excessive device self-heating and result in thermal failure. It is not possible to get this data during a "pull point" by stopping the stress, because the Rds-on degradation recovers. The ability to monitor this critical GaN failure parameter allows us to release product without this issue.

In addition to inductive-switch testing, the GaN multi-chip module needs to be evaluated in the system and run under actual product-use conditions. This validates the interactions with other system components and exposes unknown failure mechanisms. Even though the components may individually be reliable, they may interact in unanticipated ways. For example, in a cascoded GaN device, charge coupling through the drain-source capacitance of the GaN device can cause the silicon cascode device to avalanche during the turn-off transition [11]. The device is also run under load, thereby validating operation under demanding thermal conditions.

The issue of avalanche robustness deserves special mention. At present, GaN HEMTs have not shown avalanche capability. This may improve with technology maturity, since GaN itself is avalanche-capable [12] In the meantime, we are engineering TI products with enough margin to address the overvoltage conditions encountered. For example, in the case of the PFC application, the voltage seen by the FETs could momentarily rise to as high as 700V, if lightning strikes the power line. For this application, a GaN device would be built to withstand spikes of up to at least 750V.

Conclusion

At Texas Instruments, we have longstanding expertise with the qualification of silicon products, which we are bringing to bear on qualifying GaN. This involves going back to the fundamentals to understand the origins of the silicon qualification procedures, and creating tests based upon GaN-specific failures, activation energies and acceleration factors. It also involves qualifying GaN for application-relevant use, by stress-testing in a special inductive-switching test-vehicle and also by running parts in actual product configurations.

To learn more about TI's GaN solutions, please visit **www.ti.com/GaN**.

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